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Versatile Dual-Mode Class-AB Four-Quadrant Analog Multiplier

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***Abstract*—**Versatile dual-mode class-AB CMOS four-quadrant analog multiplier circuit is presented. The dual translinear loops and current mirrors are the basic building blocks in realization scheme. This technique provides; wide dynamic range, wide-bandwidth response and low power consumption. The major advantages of this approach are; its has single ended inputs; since its input is dual translinear loop operate in class-AB mode which make this multiplier configuration interesting for low-power applications; current multiplying, voltage multiplying, or current and voltage multiplying can be obtainable with balanced input. The simulation results of versatile analog multiplier demonstrate a linearity error of 1.2 %, a -3dB bandwidth of about 19MHz, a maximum power consumption of 0.46mW, and temperature compensated. Operation of versatile analog multiplier was also confirmed through an experiment using CMOS transistor array.

***Keywords*—**Class-AB, dual-mode CMOS analog multiplier, CMOS analog integrated circuit, CMOS translinear integrated circuit.

I. Introduction

ANALOG multiplier are important nonlinear analog signal processing function finding application of a wide variety in adaptive filtering, modulation, frequency translation, automatic gain controlling, neural network, etc. At present, the power consumption is a key parameter in the designing of high performance mixed-signal integrated circuit. As CMOS technology is widely recognized as the most desirable technology for integrated circuits implementation [1]. Therefore, some of CMOS multipliers [2]-[6] are not very optimal low-voltage low-power applications. Several techniques of reducing power consumption, CMOS analog multiplier circuit, have recently been described. They are the usable floating-gate MOS [7]-[9], bulk driven MOS [10], [11], subthreshold mode [11]-[13], or class-AB mode [14], [15]. However, these analog multiplier circuits have been proposed with multiplying either in voltage or current form.

In this paper, we present a versatile dual-mode analog multiplier circuit using dual translinear loops. The resulting input signal of the analog multiplier circuit can be voltage and/or current. Namely, it properly combines a voltage multiplier, a current multiplier, a current and a voltage multiplier into a circuit (we called the versatile analog multiplier circuit [16], [17]). The class-AB technique will be chosen to reduce the power consumption circuit in a standard CMOS technology. The advantages of this technique are;

1) special processing and calibration steps associated with floating gate devices are avoided;
2) the input transistor pair gain reduction and input impedance reduction associated with a bulk driven avoided;
3) high frequency response reduction associated with device operate in subthreshold mode are avoided;
4) standard CMOS technology can be used.

In addition, based on the dual translinear loop allows the design of analog multiplier circuit that exhibit wide bandwidth, high dynamic range and high speed [18], [19]. The proposed analog multiplier has single ended input, which no requires additional hardware and consequently more silicon area. Thus, it can be more easily in a large system. PSPICE simulation and experimental results are confirmed to characterize the performance of the proposed circuit.

II. Circuit Descriptions

A. Class-AB CMOS Squaring Circuit

An MOS version of the dual translinear loop for realizing the proposed versatile dual-mode analog multiplier circuit is shown in Fig. 1. The circuit consists of a dual translinear loop (M1-M4) and a current mirror (M5-M6). Generally the drain current I_D of an MOS transistor operated in saturation by neglecting the second order effect such as mobility reduction and channel-length modulation can be expressed as

$$I_D = K(V_{GS} - V_T)^2 \tag{1.1}$$

or

$$V_{GS} = V_T + \sqrt{\frac{I_D}{K}} \tag{1.2}$$

where $K=0.5\mu_O C_{OX}(W/L)$ is transconductance parameter of transistor, μ_O is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio, V_{GS} is the gate-to-source voltages and V_T is threshold voltage of the MOS transistor, respectively.

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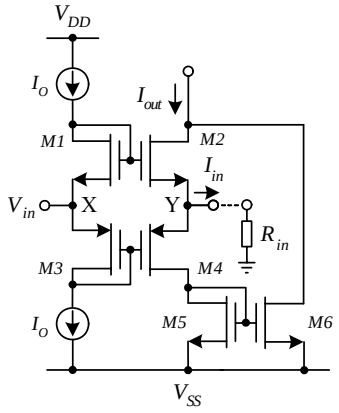

Fig. 1 Basic building block

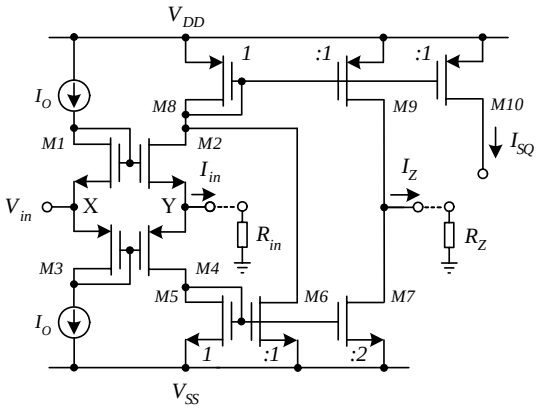

Fig. 2 Squaring and copy current into a single circuit

Consider a loop of MOS transistor M1 to M4, summing the gate-source voltages around the loop gives [20]:

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \tag{2}$$

Assuming that MOS transistors M1 to M4 from a dual translinear loop in Fig. 1 are biased in the saturation region and all transistors are well matched and having the same value of the transconductance parameter, that is $K_N=K_P$, then using (1)-(2), the relationship of the current I_O, I_{D2} and I_{D4} in the loop can be described as

$$2\sqrt{I_O} = \sqrt{I_{D2}} + \sqrt{I_{D4}} \tag{3}$$

The drain current I_{D1} and I_{D3} are equal constant current source I_O, thus from the class-AB principle [14] and [15], it can be shown that the current I_{D2} and I_{D4} are equal;

$$I_{D2} = I_O - \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_O} \tag{4}$$

and

$$I_{D4} = I_O + \frac{I_{in}}{2} + \frac{I_{in}^2}{16I_O} \tag{5}$$

The V_{in} and I_{in} are the input voltage at port Y and the input current at port X, respectively, R_X is conversions resistance. Assume the current mirror (M5, M6) has a perfect unity current gain. The current I_{D2} adds to the current I_{D2}, the output current I_{out} of the circuit in Fig. 1 can be written as

$$I_{out} = 2I_O + \frac{I_{in}^2}{8I_O} \tag{6}$$

It can see from (6) this results is the current squarer of input signal, a basic building block of the class-AB CMOS analog multiplier. It should be noted that, in a voltage input mode, the input voltage will be applied at the port Y. Since the dual translinear loop is also working as a voltage-to-current converter where $V_{in}=V_X=V_Y$ [20] and R_X is the conversion resistance, the output current I_{out} in this case can be given by

$$I_{out} = 2I_O + \frac{V_{in}^2}{8R_{in}^2 I_O} \tag{7}$$

From (6) and (7), we see that the input signal can be voltage or current. The circuit is shown in Fig. 1, it is modified to combine a squarer and a copier into a single circuit while maintaining the class-AB operates, which can be shown in Fig. 2. Assume it is well matched current mirror (M8, M10), therefore it can be given as

$$I_{SQ} = 2I_O + \frac{I_{in}^2}{8I_O} \tag{8}$$

By setting the aspect ratio (W/L) of the M5 twice of M7, therefore, the current I_Z is rewritten as

$$I_Z = I_{in} \tag{9}$$

The circuit as shown in Fig. 2 is a circuit having both a squarer and a copier into a single circuit that is used for key building block of the proposed class-AB CMOS analog multiplier.

B. The Proposed Analog Multiplier Circuit

The basic principle of operation of the proposed multiplier is based on the square-difference identity: $(X+Y)^2-X^2-Y^2=2XY$. The proposed analog multiplier circuit is shown in Fig. 3. It is based on the class-AB squaring circuit of the Fig. 2 and three dual translinear loops was used. First loop (M1 to M4) provides a X input function (I_X or V_X) to squarer function X^2, second loop (M4 to M6) provides a Y input function (I_Y or V_Y) to be squarer function Y^2 and providing a squarer function $(X+Y)^2$ for the third loop.

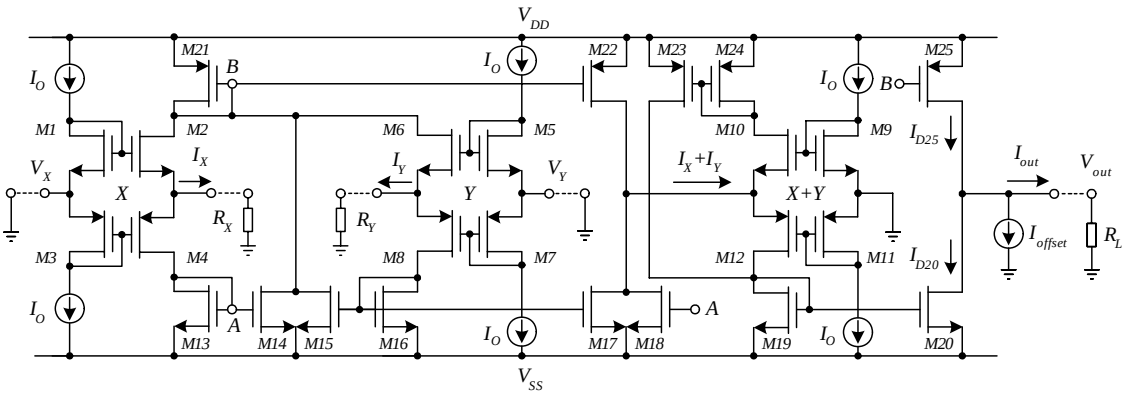

Fig. 3 Proposed versatile dual-mode class-AB analog CMOS multiplier

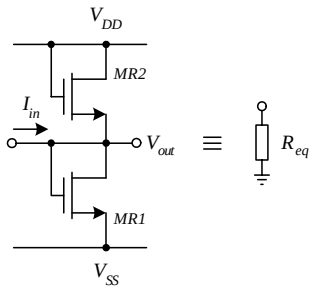

Fig. 4 Linear MOS transistor

Assuming current mirrors, M21-M25 and M19-M20 has a perfect unity current gain, thus

$$I_{D20} = 2I_O + \frac{(I_X + I_Y)^2}{8I_O} \tag{10}$$

and

$$I_{D25} = 4I_O + \frac{I_X^2 + I_Y^2}{8I_O} \tag{11}$$

From Kirchhoff's current law, it is written that

$$I_{out} = I_{D20} - I_{D25} + I_{off} \tag{12}$$

Substitute (10), (11) into (12), results the output current of the analog multiplier can be defined and expressed as

$$I_{out} = \frac{I_X I_Y}{4I_O} - 2I_O + I_{off} \tag{13}$$

To compensate the bias current $2I_O$ with constant current I_{off} ($I_{off}=2I_O$), the current I_{out} can be rewritten as

$$I_{out} = \frac{I_X I_Y}{4I_O} \tag{14}$$

It is clearly seen that the current I_{out} is in the form of a multiplier value as required. Consider (14), the multiplier has function as the current multiplier when $V_X=V_Y=0$ or connecting voltage input to ground.

By using (7) and setting $R_X=R_Y=R_L$, give I_X and I_Y is connected to grounded resistor R_X and R_Y, respectively, the multiplier has function as the voltage multiplier.

$$V_{out} = \frac{V_X V_Y}{4I_O} \tag{15}$$

If V_X is attached to ground, I_Y is connected to grounded resistor or V_X is attached to ground, I_X is connected to grounded resistor, the multiplier has function as the current and voltage multiplier.

$$V_{out} = \frac{I_X V_Y}{4I_O} \tag{16}$$

and

$$V_{out} = \frac{V_X I_Y}{4I_O} \tag{17}$$

From the multi-function of the multiplier, the proposed multiplier called the versatile analog multiplier as same in [16], [17]. It should be noted from the equations (14)-(17) that, since no terms of thansconductance parameters and threshold voltages of MOS transistors that cause of temperature effect are included in the output current I_{out} function and output voltage V_{out} function. It means that the output current and voltage are less sensitive than temperature.

For the input case is voltage form, an analog multiplier is re-quired to grounded resistors for V-I conversion. The MOS implementation of resistors which is used instead of their resistors (R_X, R_Y), can be obtained using only two MOS transistor, is shown in Fig. 4 [21]. The resistance values can be given as:

$$R_{eq} = \frac{1}{4K(V_{DD} - V_{TN})} \tag{18}$$

TABLE I
FUNCTIONS FOR VERSATILE ANALOG MULTIPLIER

Function	Condition
$I_{out}=\frac{I_X I_Y}{2I_O}$	$V_X=V_Y=GND$
$V_{out}=\frac{V_X V_Y}{2I_O}$	$I_X=I_Y=R$
$V_{out}=\frac{I_X V_Y}{2I_O}$	$V_X=GND, I_Y=R$
$V_{out}=\frac{V_X I_Y}{2I_O}$	$I_X=R, V_Y=GND$

when assume that MOS transistor MR1 and MR2 are matched, operated in saturation region, and have the same characteristic; $K=\mu_O C_{OX} W/L$, $V_{DD}=-V_{SS}$ and V_{TN}.

It can be seen from equations (14) and (17) that for an analog multiplier circuit the voltage or current can be applied. Addition, the output signal can be product of any of current and voltage form which shown in (16) and (17). All functions are listed in Table I. Finally, the circuit is suitable for IC implementation when resistors can be used instead of MOS resistors that shown in Fig. 4.

III. PERFORMANCE ANALYSIS

In this section, the characteristics of analog multiplier will be analyzed in Fig. 3. Input range, input and output impedance, mismatched and second-order effects, and frequency responses are discussed.

A. Mismatch and Second-Order Effects

In this section, the contribution consideration of the component mismatches on the distortion of the analog multiplier circuit. The transconductance and threshold voltage mismatch and second-order effect will be discussed.

The mismatching between the transconductance parameters, K_N and K_P, of the n-channel and p-channel MOS transistors of the class-AB configuration of Fig. 1 is, therefore, it is considered as the major contributor to the errors from the ideal per-formance [12]. Under this assumption, (3) becomes;

$$\sqrt{\frac{I_O}{K}}+\sqrt{\frac{I_O}{K+\Delta K}}=\sqrt{\frac{I_{D2}}{K}}+\sqrt{\frac{I_{D4}}{K+\Delta K}} \tag{19}$$

with $K_N=K$, $K_P=K+\Delta K$, using the approximation $(1+I_{in})^{-1/2}\approx 1-(1/2)I_{in}$ if $I_{in}\ll 1$, ignoring terms containing Δ^2. Assume that $4(1-\Delta)I_{in}\gg(\Delta/2)I_{in}$, it can be rewritten the (4) and (5) as follows;

$$I_{D2}\approx I_O-\left(\frac{1}{2}-\frac{1}{\Delta}\right)\frac{I_{in}}{2}+\left(1-\frac{4}{\Delta}\right)\frac{I_{in}^2}{16I_O} \tag{20}$$

and

$$I_{D4}\approx I_O+\left(\frac{1}{2}-\frac{1}{\Delta}\right)\frac{I_{in}}{2}+\left(1-\frac{4}{\Delta}\right)\frac{I_{in}^2}{16I_O} \tag{21}$$

Therefore, the output current I_{out} of the circuit in Fig. 1 can be rewritten as;

$$I_{out}\approx 2I_O+\frac{I_{in}^2}{8I_O}+\frac{I_{in}}{\Delta}-\frac{I_{in}^2}{4\Delta I_O} \tag{22}$$

From (24) implies to the first order, transconductance mismatch will affect to slope and the offset in DC squaring characteristic.

For the proposed analog multiplier that shown in Fig. 3, using (20) and (21), (10) and (11) can be rewritten as follows;

$$I_{D20}\approx 2I_O+\frac{(I_X+I_Y)^2}{8I_O}+\frac{I_X+I_Y}{\Delta}-\frac{(I_X+I_Y)^2}{\Delta 4I_O} \tag{23}$$

and

$$I_{D25}\approx 4I_O+\frac{I_X^2+I_Y^2}{8I_O}+\frac{I_X+I_Y}{\Delta}-\frac{I_X^2+I_Y^2}{\Delta 4I_O} \tag{24}$$

Therefore, the output current I_{out} of the analog multiplier circuit can be rewritten as follows:

$$I_{out}\approx\frac{I_X I_Y}{4I_O}-\frac{I_X I_Y}{\Delta 4I_O} \tag{25}$$

and

$$V_{out}\approx\frac{V_X V_Y}{4I_O}-\frac{V_X V_Y}{\Delta 4I_O} \tag{26}$$

From (27) and (28) imply that the transconductance mismatch will dominate in first order harmonic distortion.

The second order effects such as body effect, mobility reduction, and channel-length modulation are considered next. The second source of nonlinear is mobility degradation. The mobility variation is reduced by maximizing the gate-source voltage of the class-AB MOS transistors. Channel length modulation is another source of nonlinear. To reduce this effect, it is necessary to stabilize the drain-source voltage of the class-AB transistors by some effect, such as using a sufficiently large channel length throughout the circuit or cascading this also improves the current mirroring accuracy. The body effect can be reduced by connecting source and bulk of MOS transistor.

B. Input Range and Input/Output Resistance

The voltage input range of the multiplier is restricted by dual translinear loop, M1-M4 and M5-M8, and MOS transistors M13, M16, M21, operate in the saturation region. If we assume that the V_{DS} of each MOS transistors are high enough to satisfy the saturation condition. From the class-AB principle, the MOS transistor M2 and M4 alternating operate (M1-off, M3-on or M2-on, M4-off). Therefore, the voltage input range of input V_X can be written as

$$V_{SS}+2\sqrt{\frac{I_O}{K_{13}}}-\sqrt{\frac{I_O}{K_3}}+V_{T13}\le V_X\le V_{DD}+2\sqrt{\frac{I_O}{K_{21}}}-\sqrt{\frac{I_O}{K_1}}+V_{T21} \tag{27}$$

$$\frac{I_{out}}{V_X}=\frac{\left(\frac{g_{m2}\left(R_X\left(C_{gs1}+C_{gs2}\right)s+1\right)}{1+R_X g_{m2}}\right)}{\left(\frac{(C_{gs1}+C_{gs2})s}{g_{m2}}-1\right)\left(\frac{(C_{gs19}+C_{gs20})s}{g_{m20}}-1\right)\left(\frac{(C_{gs21}+C_{gs22})s}{g_{m22}}-1\right)\left(\frac{R_X C_{gs2}s}{1+R_X g_{m2}}+1\right)} \quad (34)$$

whereas, the input V_Y restricts the MOS transistor M5 and M6 is alternating operates (M6-off, M8-on or M5-on, M7-off). Thus, input voltage range of input V_Y can be written as

$$V_{SS}+2\sqrt{\frac{I_O}{K_{16}}}-\sqrt{\frac{I_O}{K_7}}+V_{T16}\le V_Y\le V_{DD}+2\sqrt{\frac{I_O}{K_{21}}}-\sqrt{\frac{I_O}{K_5}}+V_{T21} \quad (28)$$

Again, the value of input currents, I_X and I_Y, is restricted by the saturation condition of an MOS transistor of the dual trans-linear loop (M1 toM8). Therefore the input current range of proposed multiplier should be given by

$$\left|I_X\right|=\left|I_Y\right|\le 2I_O \quad (29)$$

The analog multiplier in Fig. 3 can fine the input and output impedance by take it into the small-small circuit. Assume that; $r_{Io}\ll 1/g_{m1}$, $1/g_{m5}\ll 1/g_{m3}$ and $1/g_{m7}$, where r_{Io} is inner resistance of current source I_O, r_{dj} and g_{mj} are drain-source resistances and transconductances, respectively, of MOS transistor Mj,. Therefore, the input impedances at port V_X and V_Y can be given as;

$$r_{V_X}=r_{V_Y}\cong\frac{r_{I_O}}{2} \quad (30)$$

The input impedance at port I_X and I_Y can be derived as;

$$r_{I_X}=\frac{1}{\left(g_{m2}+g_{m4}\right)+\left(\frac{g_{m4}g_{m14}g_{d2}}{g_{m21}g_{d13}}\right)} \quad (31)$$

and

$$r_{I_Y}=\frac{1}{\left(g_{m6}+g_{m8}\right)+\left(\frac{g_{m8}g_{m15}g_{d6}}{g_{m21}g_{d16}}\right)} \quad (32)$$

The output impedance r_{out} can be calculated from M20, M25 as follows;

$$r_{out}=r_{d20}\,//\,r_{d25} \quad (33)$$

From (33), r_{V_X}, r_{V_Y} depend on inner resistance of current source I_O. Typically, the inner resistance of the current source is very high. Thus, as indicated by (33), the input resistances V_X, V_Y of proposed circuit is very high.

For example, the CMOS with V_{TN}=0.62V, V_{TP}=-0.58V, $\mu_O C_{OX}=53\times10^{-7}AV^{-2}$. Let $V_{DD}=-V_{SS}$=1.5V and I_O=10μA, then the input range V_X,V_Y and I_X, I_Y of multiplier is approximately equal to |20μA| and |400mV|, respectively.

C. Frequency Response

From the analog multiplier in Fig. 3, the input voltage has considered under condition operation in class-AB. Therefore, MOS transistor M1, M2, M17, M18, M23, and M24 is the pass of signal that chosen for calculation. For high-frequency, the major high frequency limitation of the proposed circuit results for the bandwidth of three current mirrors M1-M2, M21-M22 and M19-M20, the transfer function of the multiplier circuit can be expressed as equation (32), where g_{mi}, g_{di} denote the transconductances and output conductance and C_{gsi} denotes the gate-to-source capacitances, respectively, of the MOS transistor Mi. Based on (34), assume $g_{m1}\approx g_{m5}$ and $g_{m2}\approx g_{m6}$, the transfer function of I_{out}/V_Y can be given as $I_{out}/V_Y\approx I_{out}/V_X$. From equation (34), the cutoff frequency can be approximately given by $1/(2\pi R_X(C_{gs1}+C_{gs2}))$.

The input current is considered next. The major high frequency limitation results from the bandwidth of negative current mirror M21-M22 and positive current mirror M19-M20. It means the input current of circuit can be operated wider bandwidth than input voltage. The dominant poles of the two current mirrors is approximately given by $1/(1+s(C_{gs21}/g_{m21}))$, $1/(1+s(C_{gs19}/g_{m19}))$.

IV. Simulation and Experimental Results

A. Simulation Results

The performance of the analog multiplier circuit as shown in Fig. 3 are simulated using PSPICE with level 3 model of 0.5μm CMOS parameter of MIETEC as shown in Table II. The transistors aspect ratios as given in Table III and the supply voltage are $V_{DD}=-V_{SS}$=1.5V, I_O is set to 10μA and $R_L=R_X=R_Y$ =10kΩ.

Fig. 5 shows the DC transfer characteristics of the proposed analog multiplier when input are currents. The output current swings between -20μA to +20μA for the input current range of ±20μA, while the V_X and V_Y are connected to ground.

Fig. 6 shows the DC transfer characteristic of multiplier under condition by varying V_X from -300mV to 300mV against varying V_Y from -300mV to 300mV at 100mV per step, while the input I_X and I_Y are connected to $R_X=R_Y$=10kΩ. The input and output swing can be increased by using large input and output resistors.

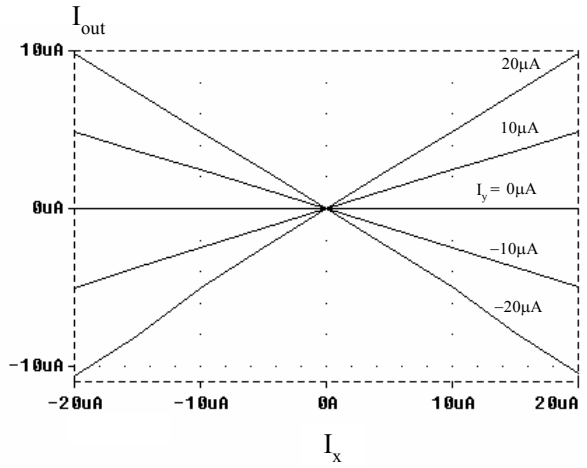

Fig. 5 Simulated DC transfer characteristics for inputs are currents

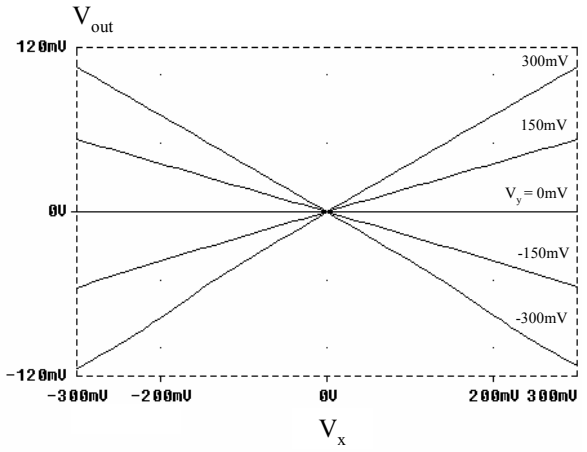

Fig. 6 Simulated DC transfer characteristics for inputs are voltages

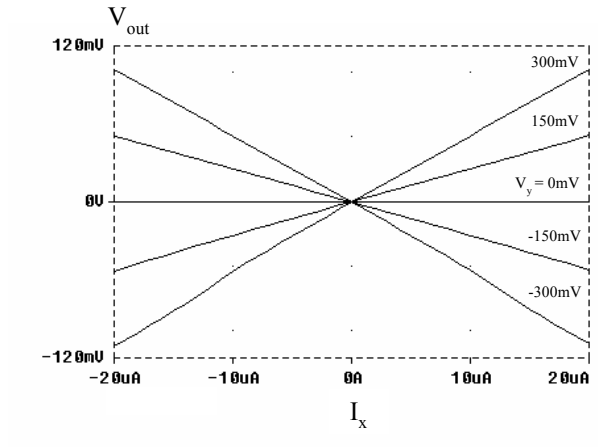

Fig. 7 Simulated DC transfer characteristics for inputs are voltage and current

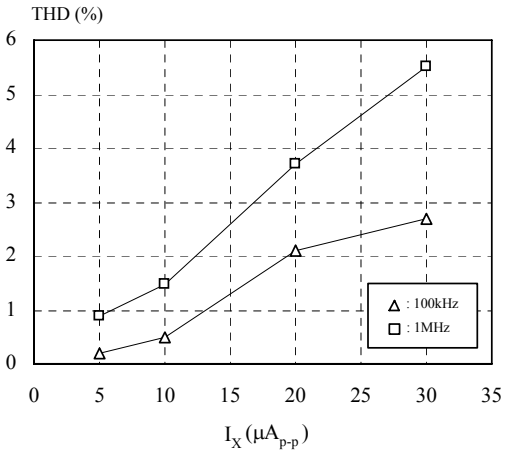

Fig. 8 Total harmonic distortion versus input current

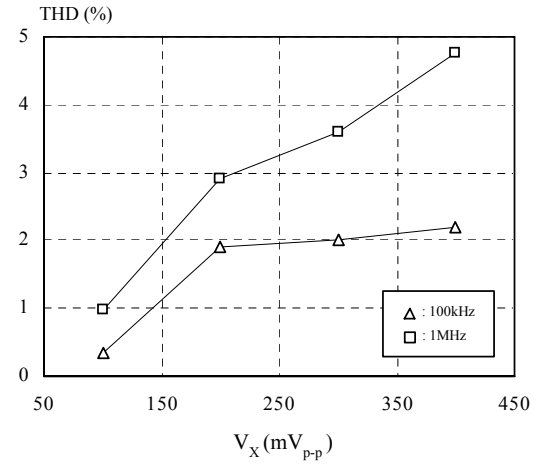

Fig. 9 Total harmonic distortion versus input voltage

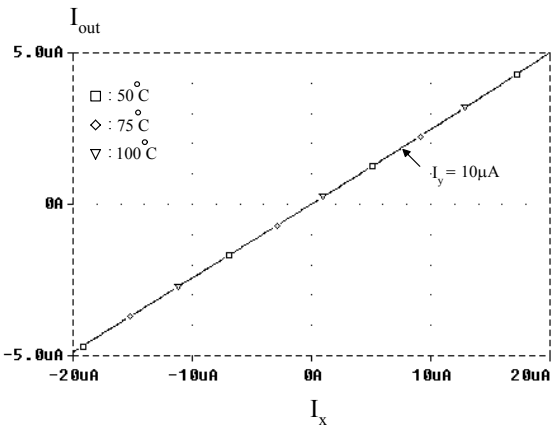

Fig. 10 Simulated DC transfer characteristic for I_Y = 10μA and temperatures = 50°C, 75°C and 100°C

TABLE II
MOS MODEL USED IN THE SIMULATION

.MODEL NM NMOS LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1 VTO=0.62 JS=1.08E-6 XJ=0.15U RSH=2.73 LD=0.04U VMAX=130E3 NSUB=1.71E17 PB=0.761 ETA=00 THETA=0.129 PHI=0.905 GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357 CJSW=5.68E-10 MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=3.07E-28 AF=1 WD=+0.11U DELTA=+0.42 NFS=1.2E11 DELL=0U LIS=2 ISTMP=10 TT=0.1E-9

.MODEL PM PMOS LEVEL=3 UO=100 TOX=1.0E-8 TPG=1 VTO=-0.58 JS=0.38E-6 XJ=0.10U RSH=1.81 LD=0.03U VMAX=113E3 NSUB=2.08E17 PB=0.911 ETA=00 THETA=0.120 PHI=0.905 GAMMA=0.76 KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10 MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10 CGBO=3.45E-10 KF=1.08E-29 AF=1 WD=0.14U DELTA=0.81 NFS=0.52E11 DELL=0U LIS=2 ISTMP=10 TT=0.1E-9

TABLE III
MOS TRANSISTOR SIZES

Transistor	W/L (μm/μm)
M1, M2, M5, M6, M9, M10, M13, M14, M15, M16, M19, M20	20/4
M3, M4, M7, M8, M11, M12, M21, M22, M23, M24, M25	93/4
M17, M18	40/4

From PSPICE simulations, the linearity error was 1.2%. The total harmonic distortion (THD) versus input current signal at 100kHz and 1MHz is shown in Fig. 8, and versus input voltage is shown in Fig 9. The dependence of the output current on temperature was studied and shown in Fig. 10. The simulation results for the variation of the output current, I_{out}, due to the change of temperature are plotted for the operating tempera- tures = 50°C, 75°C and 100°C. Let the input signal current I_Y=10μA and I_X varied from -20μA to 20μA. This simulation results demonstrated the realization, the temperature depen- dence of the transconductances and the threshold voltages of MOS transistors can be compensated.

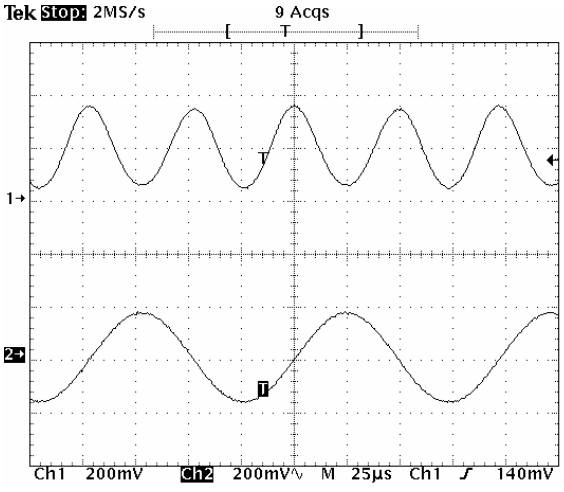

Fig. 11 Measured frequency doubler with a 10kHz sine wave inputs. Lower track: 400mV$_{P-P}$ sinusoidal signal of 20kHz (200mV/div), Upper track: output waveform (200mV/div), horizontal scale is 25μs/div

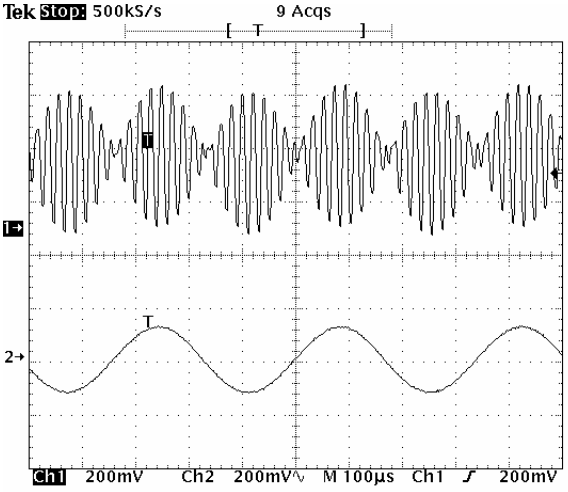

Fig. 12 Measured output waveform of a 50kHz sinusoid and a 3kHz triangular wave. Lower track: 400mV$_{P-P}$ sine signal of 3kHz (200mV/div), Upper track: output waveform (200mV/div), Horizontal scale is 100μs/div

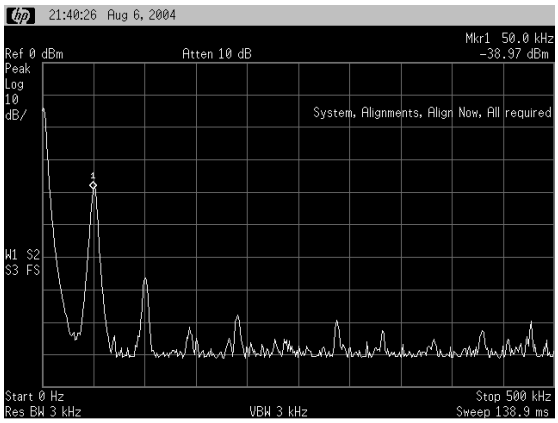

Fig. 13 Measured output spectrum of multiplier, for the case in which a 400mV$_{P-P}$ sinusoidal signal of 50kHz and a 400mV DC voltage are applied to V_X and V_Y, respectively [horizontal scale is 100μs/div; vertical scale is 10dBm]

B. Experimental Results

The circuit of Fig. 3 is prototyped the form of complementtary MOS transistor pair (MC14007). In this experiment, V_{DD}=-V_{SS}=3V and R_L=1kΩ where they are used for the multiplier. The input I_X and I_Y are connected with R_X=R_Y=10kΩ and the input V_X and V_Y are used. Fig. 11 shows the performance of the multiplier as a frequency doubler, the input signals are two in-phase 10kHz sine wave 400mV$_{P-P}$ (Lower trace 200mV/div) that applied to V_X and V_Y, respectively. The output is a sine wave of twice the input signal frequency and has a magnitude of 320mV$_{P-P}$ (Upper trace 200mV/div). Fig. 12 shows the multiplier being used for amplitude modulation, when inputs, a 3kHz sinusoidal signal (Lower trace, 200mV/div) and a 50kHz 400mV$_{P-P}$ sinusoidal signal are applied to V_X and V_Y, respectively. Fig. 13 shows the

multiplier output on spectrum analyzer when a 400mV$_{P-P}$ sinusoidal signal of 50kHz and a 0.4V DC voltage are applied to V_X and V_Y, respectively. In Fig. 13 the measured THD is –59dB with the second and third harmonics as main contribution to distortion.

V. Conclusion

The class-AB CMOS four-quadrant multiplier was presented. The proposed circuit has distinguished in used class AB mode, and its combine a voltage multiplier, a current multiplier, a current and a voltage multiplier into single ended circuit. The advantages of the proposed analog multiplier circuit over previous circuit are; (i) versatile analog multiplier since the input can be voltage, current or both voltage and current, (ii) high dynamic range and high speed, since input operated in class-AB, (iii) high bandwidth and high temperature stability, since the circuit realizing based on dual translinear loop [18], [19]. The multiplier can be used in analog VLSI cell for low power high dynamic range and high speed application, such as IF variable gain amplifier and adaptive filters. The experimental results have been shown to confirm the operation. The PSPICE simulation results of this analog multiplier are summarized in Table IV.

TABLE IV
Simulated Performance of Proposed Multiplier

Parameter	Values
Technology	0.5μm CMOS
Supply voltage	±1.5V
Bias current	10μA
Input voltage range @R_X=R_Y=10kΩ	±300mV
Input current range	±20μA
Bandwidth (-3dB)	19MHz
Nonlinear error for I_X@I_Y=20μA Nonlinear error for V_X@V_Y=300mV	1.2% 1.2%
THD for @I_X=20μA$_{P-P}$,100kHz; I_Y=20μA$_{DC}$ THD for @V_X=300mV$_{P-P}$,100kHz; V_Y=300mV$_{DC}$	2% 1.9%
Power consumption (Max.)	0.46mW

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