Trap Assisted Tunneling Model for Gate Current in Nano Scale MOSFET with High-K Gate Dielectrics

Ashwani K. Rana, Narottam Chand and Vinod Kapoor

Abstract—This paper presents a new compact analytical model of the gate leakage current in high-k based nano scale MOSFET by assuming a two-step inelastic trap-assisted tunneling (ITAT) process as the conduction mechanism. This model is based on an inelastic trap-assisted tunneling (ITAT) mechanism combined with a semi-empirical gate leakage current formulation in the BSIM 4 model. The gate tunneling currents have been calculated as a function of gate voltage for different gate dielectrics structures such as HfO_2, Al_2O_3 and Si_3N_4 with EOT (equivalent oxide thickness) of 1.0 nm. The proposed model is compared and contrasted with santaurus simulation results to verify the accuracy of the model and excellent agreement is found between the analytical and simulated data. It is observed that proposed analytical model is suitable for different high-k gate dielectrics simply by adjusting two fitting parameters. It was also shown that gate leakages reduced with the introduction of high-k gate dielectric in place of SiO_2.

Keywords—Analytical model, High-k gate dielectrics, inelastic trap assisted tunneling, metal–oxide–semiconductor (MOS) devices.

I. INTRODUCTION

OVER the last few decades, a dramatic increase in the performance of VLSI ICs has been achieved as a result of continued scaling of MOS transistor. However, as a result of aggressing scaling to obtain high current drive and good control on short channel effect, gate oxide thickness approaches its manufacturing and physically limiting value of less than 2 nm [1]. For example, devices with oxides thinner than ~ 4-5 nm exhibit large off-state leakage currents (1 to 10 A/cm) since carriers can easily tunnel directly between the substrate and gate electrode [2]-[3]. Consequently, gate leakage (tunneling) current has emerged as the most prominent form of leakage due to use of ever lower thickness of SiO_2 layer in nano-CMOS devices, particularly in the 65 nm and below regime. This is a big concern for satellite systems and ground-based mobile electronics where power conservation is important.

To reconcile the need for reduced off-state leakage currents in highly scaled devices, the replacement of SiO_2 as gate dielectric with alternate high-k dielectric material is considered as a method to contain/reduce the gate leakage current, thus constructing a type of non-classical nano-MOS transistor [2]-[6]. The use of high-κ gate dielectrics to replace SiO_2 serves the dual purpose of reducing the gate leakage as well as scaling of future devices. The main advantage of alternative high-κ dielectrics is that they can have higher dielectric constants which make it possible to manufacture a gate insulator that is physically thicker than SiO_2, but which maintains electrostatically similar performance to ultrathin SiO_2 layers. The increased physical thickness significantly reduces the probability of charge tunneling across the insulator and therefore reduces the amount of off-state leakage current [5]-[6].

Research on high-k dielectrics quickly converged on the Al_2O_3, HfO_2, and ZrO_2 family, which has a band gap larger than 5.0 eV [7], [8]-[12]. However, HfO_2 and ZrO_2 received most attention in the late 1990s, based on their better thermal stability with Si [13]-[14].

Many high-κ gate dielectrics have shown encouraging electrical characteristics as described above; however, other concerns for high-κ dielectrics include several orders of magnitude more traps found in the bulk or interface [3],[6],[13]-[15]. The traps generation is believed due to high voltage stressing across the high-k gate dielectrics which lead to trap assisted tunneling [16]. These traps greatly influence the gate leakage component of the devices [17]. Therefore, trap-assisted tunneling, also supported by A. Palma et al in [18], is the main mechanism of carrier tunneling through high-k based nano scale MOSFETs when modeling the gate current for nanoscale MOS devices in modern simulators.

In the past, research has been carried out to model the gate tunneling currents through various high-k dielectrics [19]-[21]. In [19]-[21], numerical models are utilized, which neglects the trap assisted tunneling through high-k dielectrics. In addition, numerical modeling approach is time consuming and difficult to use in practice.

Huixian Wu et al [22] proposed a semi-empirical gate tunnel model based on WKB approximation which neglects the trap assisted tunneling through high-k dielectrics. In a

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recent paper [23], A. Bouazra et al established an approach to model the trap assisted tunneling through HfO$_2$/SiO$_2$ multi stacks by solving a set of coupled Schrödinger-Poisson equation. The problem was treated numerically using the finite differential method.

In this work, a simplified analytical model of gate tunnel current through high-k dielectrics is presented which accounts trap assisted tunneling mechanism. This model is based on an inelastic trap-assisted tunneling mechanism combined with semi-empirical gate leakage current model of BSIM 4.

The rest of the paper is organized as follows. In Section II, theoretical modeling of trap assisted gate tunneling current is established. The high-k gate dielectric device structure and design used for simulation set up is presented in Section III. The results obtained are discussed in Section IV. Finally, concluding remarks are offered in Section V.

II. INELASTIC TRAP ASSISTED TUNNELING (ITAT) MODEL

The schematic energy band diagram shown in Fig. 1 illustrate our model in more detail showing the conditions which lead to inelastic trap assisted tunneling. The Fig. 1 illustrate the energetic situation for a p-type Si substrate and a n$^+$- doped poly Si gate electrode.
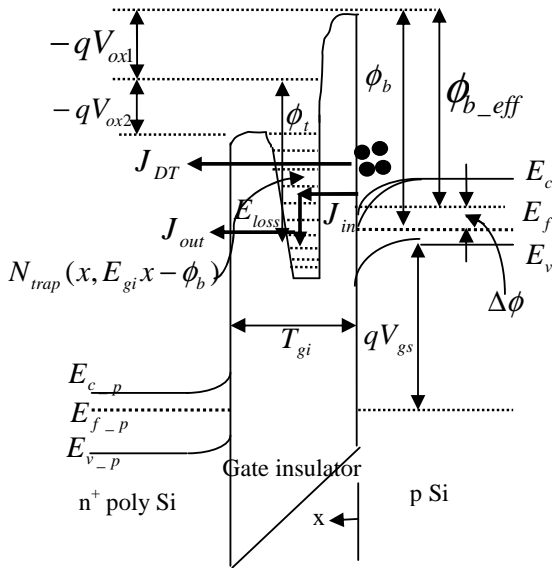

Fig. 1 Schematic energy band diagram of two-step inelastic trap-assisted tunneling through high-k gate insulator of a nano scale MOSFET Mapping nonlinear data to a higher dimensional feature space

It is observed that electrons injected from the High-k/Si interface will first tunnel to the nearer trap, then to the farther trap, and finally out of the gate insulator.

Assumptions:

i. inelastic trap assisted tunneling is a two step process for simplicity

ii. Firstly, electrons tunnel into deep lying trap state, become released from the trap state and subsequently tunnel to gate under the influence of the applied electric field.

In this process, tunneling-in current from inversion layer to the traps and tunneling-out current from the traps to the gate are calculated by modifying the formulation of direct tunneling in the BSIM 4 model [24]-[25]. Assuming that x is the distance from the Si–high-k interface, $N_{trap}(x, E)$ is the sheet trap density in cm^2 at a distance x and having the energy level with respect to the conduction band edge of gate dielectric, $O_t(x, E)$ is the electron occupancy of the traps at a distance of x and the energy of E, σ_t is the capture cross section of the traps and A_g is the gate tunneling area. The tunnel-in current density (J_{in}) into the traps and the tunnel-out current (J_{out}) density from the traps are then expressed as

$$J_{in} = \frac{q}{A_g} \sigma_t N_{trap}\left(x, qE_{gi}x - \phi_{b\_eff}\right) \times$$
$$\left[1 - O_t\left(x, qE_{gi1}x - \phi_{b\_eff}\right)\right] J_1\left(\phi_{b\_eff}, x, E_{gi1}\right) \quad (1)$$

$$J_{out} = \frac{q}{A_g} \sigma_t N_{trap}\left(x, qE_{gi1}x - \phi_{b\_eff}\right) \times$$
$$O_t\left(x, qE_{gi1}x - \phi_{b\_eff}\right) J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right) \quad (2)$$

$$\phi_t = \phi_{b\_eff} - qE_{gi1}x + E_{LOSS} \quad (3)$$

where Φ_t is the barrier height of the gate insulator trap states, E_{gi} is the electric field in the gate insulator, E_{gi1} is the electric field over a distance x of the trap relative to the interface in the gate insulator and E_{gi2} is the electric field over a distance t_{gi}-x relative to the interface in the gate insulator, E_{Loss} is the energy loss accompanied with the injection of electrons into the neutral trap sites and σ_t is assumed to be constant irrespective of the position and energy level of the traps. J_1 and J_2 are the uniform current density and are calculated by modifying the formulation of direct tunneling in the BSIM model. Φ_b is the actual barrier height of gate insulator i.e. gate dielectric and ϕ_{b_eff} is the effective barrier height, given as below,

$$\phi_{b\_eff} = \phi_b - \Delta\phi \quad (4)$$

$$\Delta\phi = \sqrt{\frac{qE_{gi}}{4\pi\varepsilon_{gi}}} = \sqrt{\frac{qV_{gi}}{4\pi\varepsilon_{gi}T_{gi}}} = \left(\frac{2q^3 N_{eff}\phi_{b\_eff}}{16\pi^2\varepsilon_{gi}^3}\right)^{1/4} \quad (5)$$

The $\Delta\phi$ is the reduction in the barrier height at the high-k/Si interface [26] from Φ_b so that barrier height becomes ϕ_{b_eff}.

This reduction in barrier height is due to image charges across the interface. This barrier reduction is of great interest since it modulates the gate tunneling current.

The resulting tunneling current J_{ITAT} of this trap-assisted tunneling process is given by a detailed balance of J_{in} and J_{out}. Consequently, inelastic trap assisted tunneling current can be expressed as

$$J_{ITAT} =$$
$$\frac{q}{A_g} \sigma_t N_{trap}\left(x, qE_{gi}x - \phi_{b\_eff}\right) P_{ITAT}\left(x, E, E_{gi}\right) \quad (6)$$

where P_{ITAT} can be expressed as

$$P_{ITAT} = \frac{J_1(\phi_{b\_eff}, x, E_{gi1}) J_2(\phi_t, t_{gi} - x, E_{gi2})}{J_1(\phi_{b\_eff}, x, E_{gi1}) + J_2(\phi_t, t_{gi} - x, E_{gi2})} \quad (7)$$

Using Gauss's law and considering MOS capacitor equivalent circuit, the local electrical fields E_{gi1} and E_{gi2} of both the tunneling regions finally become

$$E_{gi1} = E_{gi} + \frac{t_{gi} - x}{t_{gi}} \cdot \frac{q N_{trap}}{\varepsilon_{gi}} \quad (8)$$

$$E_{gi2} = E_{gi} + \frac{x}{t_{gi}} \cdot \frac{q N_{trap}}{\varepsilon_{gi}} \quad (9)$$

The modified uniform current density J_1 and J_2 as obtained from BSIM 4 are expressed as

$$J_1(\phi_{b\_eff}, x, E_{gi1}) = A_t \frac{C(\phi_{b\_eff}, x, E_{gi1})}{\phi_{b\_eff}} \cdot \times$$

$$\exp\left[-\frac{8\pi\sqrt{2m_{gi}}}{3hq} \cdot \frac{\phi_{b\_eff}^{3/2}}{E_{gi1}} \beta(\phi_{b\_eff}, x, E_{gi1}) \right] \quad (10)$$

$$J_2(\phi_{b\_eff}, x, E_{gi1}) = A_t \frac{C(\phi_t, t_{gi} - x, E_{gi2})}{\phi_t} \times$$

$$\exp\left[-\frac{8\pi\sqrt{2m_{gi}}}{3hq} \cdot \frac{\phi_t^{3/2}}{E_{gi2}} \beta(\phi_t, t_{gi} - x, E_{gi2}) \right] \quad (11)$$

$$\text{where } A_t = \frac{q^3}{8\pi\phi_{b\_eff}\varepsilon_{gi}}$$

$$c_{(ch,ov)}(\phi_{b\_eff}, x, E_{gi1}) =$$

$$\exp\left[\frac{20}{\phi_{b\_eff}} \left(\frac{x|E_{gi1(ch,ov)}| - \phi_{b\_eff\_}}{\phi_{b\_eff}} + 1 \right)^{\alpha(ch,ov)} \cdot \left(1 - \frac{x|E_{gi1(ch,ov)}|}{\phi_{b\_eff}} \right) \right].$$

$$\times (E_{gi1}) N_{DTC(ch,ov)}$$

$$c_{(ch,ov)}(\phi_t, t_{gi} - x, E_{gi2}) =$$

$$\exp\left[\frac{20}{\phi_t} \left(\frac{(t_{gi} - x)|E_{gi2(ch,ov)}| - \phi_t}{\phi_t} + 1 \right)^{\alpha(ch,ov)} \cdot \left(1 - \frac{(t_{gi} - x)|E_{gi2(ch,ov)}|}{\phi_t} \right) \right] \times$$

$$.(E_{gi2}) N_{DTC(ch,ov)}$$

$$\beta(\phi_{b\_eff}, x, E_{gi1}) = 1 - \left(1 - \frac{qx}{\phi_{b\_eff}}|E_{gi1}| \right)^{3/2}$$

$$\beta(\phi_t, t_{gi} - x, E_{gi2}) = 1 - \left(1 - \frac{q(t_{gi} - x)}{\phi_t}|E_{gi2}| \right)^{3/2}$$

$$N_{DTC(ov)} = \begin{cases} \frac{\varepsilon_{gi}}{t_{gi}} \left\{ n_{acc} v_t . \ln\left[1 + \exp\left(-\frac{V_g}{n_{acc} v_t} \right) \right] \right\} \\ \qquad for V_g < 0 \\ \frac{\varepsilon_{gi}}{t_{gi}} \left\{ n_{acc} v_t . \ln\left[1 + \exp\left(-\frac{V_{ge}}{n_{acc} v_t} \right) \right] \right\} \\ \qquad for V_g > 0 \end{cases}$$

$$N_{DTC(ch)} = \begin{cases} \frac{\varepsilon_{gi}}{t_{gi}} \left\{ n_{acc} v_t . \ln\left[1 + \exp\left(-\frac{(V_g - V_{FB})}{n_{acc} v_t} \right) \right] \right\} \\ \qquad for V_g < 0 \\ \frac{\varepsilon_{gi}}{t_{gi}} \left\{ n_{inv} v_t . \ln\left[1 + \exp\left(-\frac{(V_g - V_{th})}{n_{inv} v_t} \right) \right] \right\} \\ \qquad for V_g > 0 \end{cases}$$

In the above equation, $\alpha(ch,ov)$ is the fitting parameter depending upon channel or source/drain overlap tunneling, ϕ_b is the actual tunneling barrier height, n_{inv} and n_{acc} are the swing parameters, V_{FB} represents the flat band voltage, $N_{DTC(ch,ov)}$ denotes the density of carrier in channel/overlap region depending upon MOSFET biasing condition and V_{ge} is the effective gate voltage excluding poly gate non-uniformity and gate length effect and is equal to $V_g - V_{poly}$. The default values of n_{inv} and n_{acc} are S/v_t (S is the sub threshold swing) and 1 respectively. The correction $C_{F(ch,ov)}$ and transmission probability $(T_{WKB(ch,ov)})$ are different for channel and source/drain overlap region because both channel and overlap component have different value of $V_{ox(ch,ov)}$ and $N_{DTC(ch,ov)}$. It is because of the fact that overlap region has almost zero flat band voltage as both SDE region and overlying poly-gate Si are heavily doped n^+ regions. The $N_{DTC(ch,ov)}$ has been given differently for both region as above. The gate oxide voltage for the channel and SDE overlap are calculated as follows.

Case (i): when $V_g > 0$

In this biasing condition MOSFET device, there is a depletion layer in the poly gate thereby causing an additional potential drop across the gate. The SDE region enters into accumulation and substrate region enters into the week inversion below V_{th} and strong inversion beyond V_{th}. Therefore both the channel and EDT component are present and are comparable.

Case (ii): when $V_{FB} < V_g < 0$

Here, gate tunneling current is dominated by the EDT where electric field is such that electron are directed from the accumulated poly-gate into the overlap region. On other hand, substrate is in depletion /weak inversion and constitutes negligible tunneling current. This region of biasing is primarily responsible for off-state power dissipation. Thus, EDT plays an important role in the evaluation of off-state power dissipation

Case (ii): when $V_g < V_{FB}$

In this region of operation, substrate goes into accumulation. As a result both current components become comparable. The voltage across the gate oxide for different region of operation is as follows.

$$V_{gi} = \begin{cases} (V_g - \phi_s - V_{FB}) \, for \, V_g < 0 \\ (V_{ge} - \phi_s - V_{FB}) \, for \, V_g > 0 \end{cases} \qquad (12)$$

Where ϕ_s is the surface band bending of the substrate and are calculated for channel and overlap region depending upon the biasing condition of the MOSFET device including the poly non-uniformity, gate length effects and image force barrier lowering. The accurate surface potentials expressions in case of channel in weak inversion/depletion, strong inversion and in accumulation can be taken from [27]. The gate effective voltage including the effect of nonuniform dopant distribution in the gate is derived as follows.

$$\therefore V_{ge} = (V_{FB} + \phi_{so} - \Delta V_{p1} - \Delta V_{p2}) +$$

$$\frac{(q\varepsilon_{si} N_{poly} T_{gi}^2)}{\varepsilon_{gi}^2} \left[\sqrt{1 + \frac{2\varepsilon_{ox}^2 (V_g - V_{FB} - \phi_{so})}{q\varepsilon_{si} N_{poly} T_{gi}^2}} - 1 \right] \qquad (13)$$

The ϕ_{so}, by taking the quantization effect into account, is given [28] as follows.

$$\phi_{so} = 2\phi_s + \Delta\phi_s^{QM} - V_{BS} \qquad (14)$$

Where $\Delta\phi_s^{QM}$ can be taken from [27]. This equation (15) includes the non uniformity in the gate dopant profile through a term ΔV_{p1} and fringing field effect *i.e* gate length effect through a term ΔV_{p2}. The potential drop ΔV_{p1} due to non uniform dopant profile in poly Si gate, caused by low energy implantation, is given [29] by

$$\Delta V_{p1} = \left(\frac{kT}{q}\right) \ln\left(\frac{N_{poly\_top}}{N_{poly\_bottom}}\right) \qquad (15)$$

The N_{poly_top} and N_{poly_bottom} are the doping concentration at the top and bottom of the polysilicon gate. The potential

drop ΔV_{p2} due to gate length effect, caused by very short gate lengths is given as below

$$\Delta V_{p2} \approx \frac{\Delta Q}{C_d} = \frac{2qAN_d}{L_g C_d} \left(V/_{cm}\right) \qquad (16)$$

$$C_d = \delta\frac{\varepsilon_{gi}}{\pi} \ln\left[\frac{3 - \cos\left\{\pi\left(\frac{T_F - T_{gi}}{T_F}\right)\right\}}{1 + \left\{\pi\left(\frac{T_F - T_{gi}}{T_F}\right)\right\}}\right] \qquad (17)$$

where A denote the triangular area of the additional charge, L_g is the gate length, C_d is the depletion capacitance in the sidewalls [30], ε_{gi} is the permittivity of the gate insulator, T_F is the thickness of the field oxide, T_{gi} is the thickness of the gate insulator and δ is fitting parameter equal to 0.95 normally.

III. SIMULATION SET UP

Figure 2 shows the schematic of device structure of N-MOSFET with high-k gate dielectric used in this study.
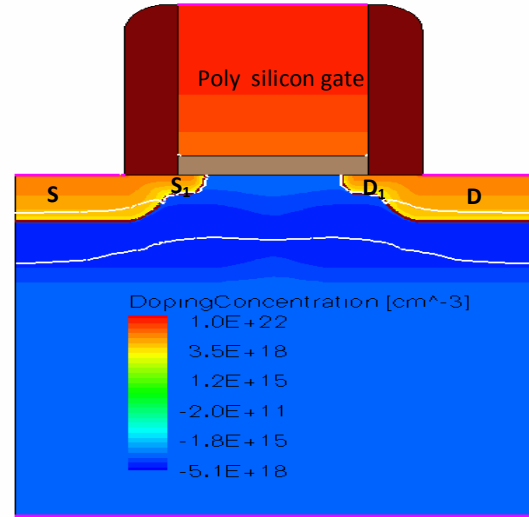

Fig. 2. NMOSFET device structure with high-k gate dielectrics used in simulation

The deep S/D region is composed of a heavily doped silicon and a silicide contact. The doping of the silicon S/D region is assumed to be very high, 1×10^{20} cm^{-3}, which is close to the solid solubility limit and introduces negligible silicon resistance. The dimension of the silicon S/D region is taken as 20 nm long and 50 nm high. This gives a large contact area resulting in a small contact resistance.

The heavily doped silicon called deep S/D region extend into the silicon film at both ends and constitute the extended S/D for the device (labelled by ''S$_1$''and ''D$_1$'' in Fig. 2). The lengths of these extended regions at both ends are equal and are denoted by S$_1$ and D$_1$. S/D implantation is performed after defining the gate and the oxide spacer. Boron ions were implanted into the channel region to reduce the leakage current and to keep a low accepter concentration in the non-

overlapped channel region. The doping concentration of the acceptors in silicon channel region is assumed to be graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of 1×10^{18} cm^{-3} and 1×10^{17} cm^{-3} near the channel. The halo implantation done around the S/D also reduces short-channel effects, such as the punch-through current, DIBL, and threshold voltage roll-off, for different non-overlap lengths.

The MOSFET has a 50-nm-thick n+ poly-Si gate with metallurgical gate length of 25 nm and a 1-nm gate oxide. The oxide spacer has been assumed to reduce the gate capacitance. Here, Lo represents the overlap length, which is controlled by the S/D implantation energy. Lo = 5 nm optimized with off current is used in this work. The MOSFET with L_{met} of 25 nm was designed to have a V_T of 0.19 V. We determined V_T by using a linear extrapolation of the linear portion of the I_{DS}-V_{GS} curve at low drain voltages. The operating voltage for the devices is 1V. The simulation study has been conducted in two dimensions, hence all the results are in the units of per unit channel width. The simulation of the device is performed by using Santaurus design suite [31]-[32] with drift-diffusion, density gradient quantum correction and advanced physical model being turned on.

IV. RESULTS AND DISCUSSION

In this section, computation of gate tunneling currents for a n-channel fully depleted nanoscale MOSFET through different dielectric structures have been carried out. This model is computationally efficient and easy to realize. This model calculates the gate tunneling current with energy loss(E_{loss}) during inelastic trap assisted tunneling process and $\alpha_{(ch/ov)}$ as fitting parameters. It also assume in our calculation that $N_{trap}(x,E)$ is a constant irrespective of position and energy level. Thus, present model is applicable to many alternate high-k nano MOSFET simply by adjusting the two fitting parameter. The variation of total gate tunneling current with gate bias for a given values of gate insulator thickness has been presented for possible alternative gate dielectrics such as Si_3N_4, Al_2O_3 and HfO_2. The impact of dielectric constant (K) of gate dielectric on total gate tunneling current is reported in results.

The comparision between the simulated data and the model value for gate tunneling current is presented in Fig.3, 4 and 5 for HfO_2, Al_2O_3 and Si_3N_4 gate dielectics respectively. Fig. 3 shows the gate tunneling current versus gate bias for HfO_2 gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of 1×10^{17} cm^{-3} while that of polysilicon gate is 1×10^{22} cm^{-3} at the top and 1×10^{20} cm^{-3} at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and silicon. The comparision between the simulated data and the model value for gate tunneling current is presented in Fig.3, 4 and 5 for HfO_2, Al_2O_3 and Si_3N_4 gate dielectics respectively. Fig. 3 shows the gate tunneling current versus gate bias for HfO_2 gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of 1×10^{17} cm^{-3} while that of polysilicon gate is 1×10^{22} cm^{-3} at the top and 1×10^{20} cm^{-3} at bottom of the polysilicon

gate i.e. interface of high-k gate dielectric and silicon. The simulation was carried out with L_{met} = 25 nm, L_{ov} = 5nm, t_{HfO2} = 5.64 nm, ϕ_b(HfO$_2$) =1.5 ev [33], m_{eff} = 0.18m$_o$[33], $\sigma_{t=}$ 9.3×10^{-16} cm^2 [34], N_{trap} = 7.67×10^{12} cm^{-2} [34]. The trap position (x_t) is extracted to be $0.43\, t_{HfO2}$ in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 5.64 nm. The fitting parameters E_{loss}, $\alpha_{(ch)}$ and $\alpha_{(ov)}$ has been taken to 0.2 eV, 0.75 and 0.45 respectively to fit the model with the simulated value.
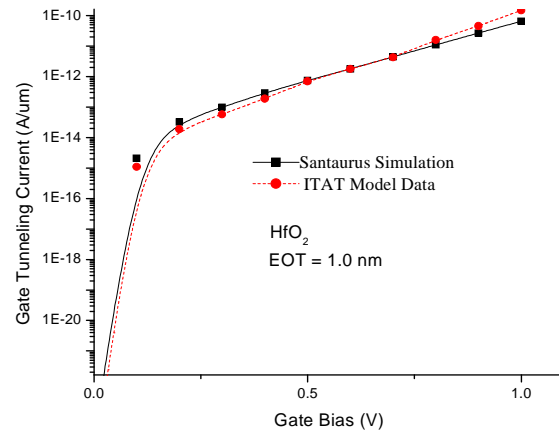

Fig 3. Comparison of analytical model data with Santaurus simulated data for HfO_2 based high-k MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L_{met}=25nm and S/D overlap length of L_{ov}=5 nm in nano scale regime

The model result obtained analytically through inelastic trap assisted tunneling current model is compared with the simulated data for HfO_2 gate dielectrics in Fig. 3. It is shown in Fig. 3 that results calculated by ITAT have better agreement with the simulated results This shows that for high-k gate dielectrics the dominant tunneling mechanism is trap assisted tunneling. This may be due to the fact that the possibility of carrier tunneling directly from channel to gate is low at large physical thickness of gate insulator (high-k gate dielectric) for a given equivalent oxide thickness (EOT).

Fig. 4 shows the gate tunneling current versus gate bias for Al_2O_3 gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of 1×10^{17} cm^{-3} while that of polysilicon gate is 1×10^{22} cm^{-3} at the top and 1×10^{20} cm^{-3} at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and silicon. The simulation was carried out with L_{met} = 25 nm, L_{ov} = 5nm, t_{Al2O3} =2.31 nm, ϕ_b(Al$_2$O$_3$) = 2.8 ev [33], m_{eff} = 0.30 m$_o$[33], $\sigma_{t=}$ 7.03×10^{-17} cm^2 [35], N_{trap} =2.4x 10^{12} cm^{-2} [35]. The trap position (x_t) is extracted to be $0.45\, t_{Al2O3}$ in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling

current of MOS capacitors with gate oxides of 2.31 nm. The fitting parameters E_{loss}, $\alpha_{(ch)}$ and $\alpha_{(ov)}$ has been taken to 0.4 eV, 0.55 and 0.38 respectively to fit the model with the simulated value.
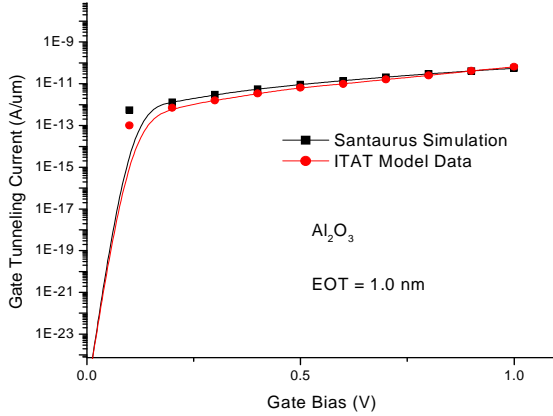

Fig 4. Comparison of analytical model data with Santaurus simulated data for Al$_2$O$_3$ based high-k MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L$_{met}$=25nm and S/D overlap length of L$_{ov}$= 5 nm in nano scale regime

It is shown in Fig. 4 that ITAT model shows good agreement with the santaurus simulation. Again, it is observed that for high-k gate insulator dominant gate tunneling mechanism is inelastic trap assisted tunneling ITAT. This is because of the fact that high-k gate dielectrics have higher trap density through which the tunneling of carrier becomes easier that results in increased tunneling current from channel to gate through traps.

Fig. 5 shows the gate tunneling current versus gate bias for Si$_3$N$_4$ gate dielectric materials with the equivalent oxide thickness (EOT) of 1 nm at substrate doping (Na) of 1×10^{17} cm^{-3} while that of polysilicon gate is 1×10^{22} cm^{-3} at the top and 1×10^{20} cm^{-3} at bottom of the polysilicon gate i.e. interface of high-k gate dielectric and silicon. The simulation was carried out with L$_{met}$ = 25 nm, L$_{ov}$ = 5nm, t_{Si3N4} =1.92 nm, ϕ_b (Si$_3$N$_4$)=2.0 ev [33], m$_{eff}$ = 0.20 m$_o$[33], σ_t =3×10^{-13} cm^2 [36-37], N$_{trap}$ =3×10^{11}cm^{-2} [38-39]. The trap position (x_t) is extracted to be $0.47 t_{Si3N4}$ in the inelastic tunneling model by comparing the magnitude of J$_{ITAT}$ with that of direct tunneling current of MOS capacitors with gate oxides of 1.92 nm. The fitting parameters E_{loss}, $\alpha_{(ch)}$ and $\alpha_{(ov)}$ has been taken to 0.2 eV, 0.87 and 0.64 respectively to fit the model with the simulated value.

The Figure 5 shows that present ITAT model produces agreeable results between modeled gate current and santaurus simulation data for Si$_3$N$_4$ high-k gate insulator structures. This is obvious as discussed above. Thus it is clear from Fig.3,4 and 5 that ITAT model is dominant for high-k gate insulator structures of MOSFET and is used throughout this work.
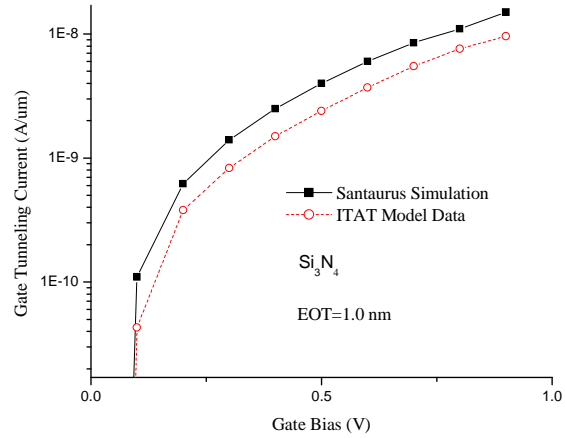

Fig 5. Comparison of analytical model data with Santaurus simulated data for Si$_3$N$_4$ based high-k MOSFET with equivalent oxide thickness (EOT) of 1.0 nm, metallurgical gate length of L$_{met}$=25nm and S/D overlap length of L$_{ov}$=5 nm in nano scale regime.
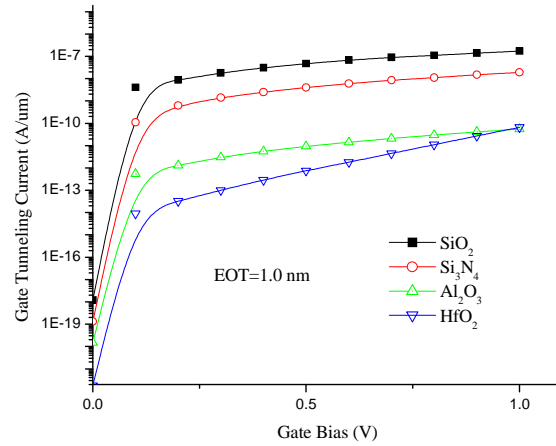

Fig 6. Gate tunneling current vs gate bias for different high-k gate dielectrics-HfO$_2$,Al$_2$O$_3$,Si$_3$N$_4$ in nano scale regime with EOT of 1.0 nm at L$_{met}$=25nm and L$_{ov}$=5.0 nm

The calculated gate current of various high-k gate insulator structures with different high-k dielectrics as a function of the gate voltage are plotted in Fig.6. For all the various high-k materials being studied, the equivalent oxide thickness (EOT) is taken to be 1.0 nm. Other device parameters mentioned earlier are used. Fig.6 shows that HfO$_2$,Al$_2$O$_3$,Si$_3$N$_4$ high-k gate dielectrics demonstrate significant gate leakage reduction compared to SiO$_2$ gate dielectric. This is because vertical electric field responsible for carrier tunneling decreases as the physical thickness of gate insulator increases with increase in dielectric constant(k). The reduction of gate tunnel current is ineffective somewhere near and above the barrier height of the high-k dielectric layer (HfO$_2$, K=22), due to the dominating tunneling near and over the barrier height of the high-k layer, although this is not a serious concern for the bias range of nanoscale MOS devices. Thus, the resulting gate current is

determined by the interplay among the barrier height, dielectric constant and gate bias voltage as well.

V. CONCLUSION

A simplified physical model applicable to gate leakage current in high-k based MOSFETs was presented. The model is based on inelastic trap-assisted tunneling (ITAT) mechanism combined with a semi-empirical direct tunneling current model. It was found that the results simulated by the ITAT model show good agreement with the santaurus simulated results for different gate-dielectric simply by adjusting two fitting parameters.

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