International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:6, No:6, 2012

# Theoretical Considerations of the Influence of Mechanical Uniaxial Stress on Pixel Readout Circuits

Georgios C. Dogiamis, Bedrich J. Hosticka, and Anton Grabmaier

***Abstract*—**In this work the effects of uniaxial mechanical stress on a pixel readout circuit are theoretically analyzed. It is shown, that the effects of mechanical stress on the in-pixel transistors do not arise at the output, when a correlated double sampling circuit is used. However, mechanical stress effects on the photodiode will directly appear at the readout chain output. Therefore, compensation techniques are needed to overcome this situation. Moreover, a simulation technique of mechanical stress is proposed and diverse layout as well as design recommendations are put forward, in order to minimize stress related effects on the output of a circuit.

***Keywords*—**mechanical uniaxial stress, pixel readout circuit.

## I. Introduction

FLEXIBLE electronics gain increasing attention during the last years with applications ranging from foldable displays up to consumer and biomedical devices [1],[2]. Furthermore, ultra-thin silicon (Si) chips, with thicknesses less than 20μm are being employed towards this direction, i.e., for realizing bendable, foldable and in general flexible circuits [3].

However, the effects of mechanical stress, generated from the mechanical deformation during bending, on the diverse circuits of a flexible chip have to be analyzed. The main goal is to design and fabricate circuits, which are minimally stress dependent (unless they are operated as stress sensors), achieving thus a uniform operation under any stressed state. The authors are currently conducting research on the effects of mechanical stress on several devices and circuits, with an ultimate goal to design a bendable integrated CMOS image sensor, operation of which is stress independent. For this reason, a theoretical analysis should be performed, describing how the applied mechanical stress will affect the output of a pixel readout circuit. Moreover, a way of simulating these effects would be advantageous for the designer of such analog circuits.

The organization of the paper involves five sections. After a brief introduction in section I, the aforementioned theoretical analysis follows in section II. In section III a novel simulation technique is presented and is followed by its results. Section IV addresses several layout and design recommendations to achieve a minimal dependence on the mechanical stress. Finally, to cap it all, concluding remarks are put forward in section V.

G. C. Dogiamis is with the University of Duisburg-Essen, Duisburg, 47057, DE (phone: +49 203-379-2819; fax: +49 203-379-2888; e-mail: georgios.dogiamis@uni-due.de;gdoyamis@ieee.org).

B. J. Hosticka is with the University of Duisburg-Essen, Duisburg, 47057, DE and the Fraunhofer Institute IMS, 47057, Duisburg, DE (phone: +49 203-378-3222; fax: +49 203-379-2888; e-mail: bedrich.hosticka@ims.fraunhofer.de).

A. Grabmaier is with the University of Duisburg-Essen, Duisburg, 47057, DE and the Fraunhofer Institute IMS, 47057, Duisburg, DE (phone: +49 203-378-3105; fax: +49 203-379-2888; e-mail: anton.grabmaier @ims.fraunhofer.de).

This research is supported by the German Research Foundation (DFG). under the contract number: GR 3328/5-1.

## II. Pixel Readout Chain under Uniaxial Mechanical Strain

Since the application of uniaxial mechanical stress changes the electrical characteristics of the basic devices used in the analog IC design [4]–[7], the analog designer has to gain insight on how the effects generated by the mechanical strain influence the operation of the circuit. The goal of this section is to systematically analyze the influence of uniaxial mechanical stress on the signal path of a pixel readout chain, similar to the one depicted in Fig. 1. This readout technique makes use of an in-pixel source follower to read out the voltage stored in the photodiode- and storage- capacitance before and after the light exposure period. In the beginning, both the photodiode and the storage capacitor are reset at the voltage $V_{pix}$. Subsequently an exposure period comes during which charge is generated in the photodiode causing the voltage drop at its terminals. Both values before and after the exposure time are sampled and amplified through a correlated double sampling switched capacitor (SC) circuit using two non-overlapping clocks $\varphi_1$ and $\varphi_2$.

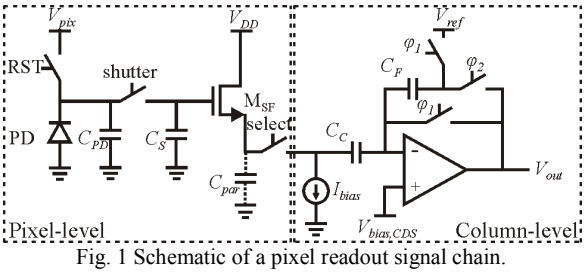


Fig. 1 Schematic of a pixel readout signal chain.

### A. pn-Photodiode

In this subsection the influence of mechanical stress on the photodiode is modeled. As stated in [8]–[10] compressive (tensile) mechanical stress causes a Si-bandgap decrease (increase), usually designated as bandgap narrowing

(widening). Therefore, not only the leakage current of the photodiode (i.e., dark current) will be influenced [9], but also the generated photocurrent is expected to change under the application of moderate stress levels. However, there is no experimental evidence on how the photocurrent is changing under the application of uniaxial mechanical stress. The authors are at the time investigating this dependence and experimental as well as theoretical results will be communicated shortly. For our analysis though, it suffices to assume that the change of the photocurrent due to the application of mechanical stress is given by:

$$I_{PD}^{\sigma}=(1+a_{PD})\cdot I_{PD}, \quad (1a)$$

where $I_{PD}$ is the generated photocurrent under the unstressed condition, the superscript $\sigma$ signifies uniaxial mechanical stress, while $\alpha_{PD}$ is the mechanical stress coefficient ($\alpha_{PD} < 1$), which can take both positive and negative values. Note that $\alpha_{PD}$ is stress dependent. If for example a linear dependence on mechanical stress is assumed, (1a) becomes then:

$$I_{PD}^{\sigma}=(1+a_{PD})\cdot I_{PD}=(1+\pi_{PD}\sigma)\cdot I_{PD}, \quad (1b)$$

where $\pi_{PD}$ is the piezojunction coefficient in $Pa^{-1}$, and $\sigma$ is the applied uniaxial mechanical stress in Pa. (A positive value of $\sigma$ denotes tension, while a negative one denotes compression.)

The photodiode voltage after the integration time $t_{int}$ (light exposure period) can be calculated now as:

$$V_{PD}=V_{pix} - \frac{t_{int}\cdot I_{PD}}{C_s+C_{PD}} \quad (2)$$

Using (1a) and (2) we can find the voltage across the photodiode in the stressed condition using the voltage in the unstressed state:

$$V_{PD}^{\sigma}-V_{pix}=(1+a_{PD})\cdot(V_{PD}-V_{pix}). \quad (3)$$

*B. In-Pixel Source Follower*

The in-pixel source follower buffers the voltage stored at the storage capacitor and thus its behavior under stressed conditions must be examined. However, before starting our analysis, it is important to define how the column current source is implemented. Let us examine two different configurations as shown in Fig. 2. Fig. 2a shows an implementation of a simple current source using one nMOSFET biased in the saturation regime making use of an external constant gate-source voltage $V_{bias}$. Fig. 2b shows a current source using a current mirror configuration with an external reference current $I_{bias}$.

Starting from the former configuration and using the square law equation for modeling of the drain-source current of the transistors, we can write for the drain current of the source follower:

$$I_{bias}=\frac{\mu_{n,bias}C_{ox}}{2}\left(\frac{W}{L}\right)_{bias}\cdot(V_{bias}-V_T)^2 = I_{SF} \quad (4a)$$

The output voltage can be determined from (4b):

$$I_{SF}=\frac{\mu_{n,SF}C_{ox}}{2}\left(\frac{W}{L}\right)_{SF}\cdot\left(V_{in}-V_{out,SF}-V_T\right)^2, \quad (4b)$$

where $\mu_n$ is the electron mobility, $C_{ox}$ is the specific gate oxide capacitance, $W$ and $L$ the width and length of the transistor channel, respectively, $I_{SF}$ and $I_{bias}$ the current through $M_{SF}$ and $M_{bias}$ respectively. For given constant $V_{in}$ and $V_{bias}$, the output $V_{out,SF}$ of the source follower can be calculated using the above equations.

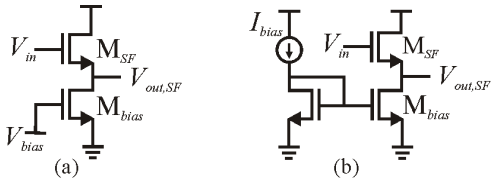


Fig. 2 Current source using (a) a MOSFET with a constant gate-source voltage (b) a current mirror biased through a constant external reference current.

The influence of mechanical stress in the various parameters of (4a) and (4b) must be modeled in order to calculate the output $V_{out,SF}^{\sigma}$ under a stressed condition. The application of uniaxial stress on MOS transistors has extensively been studied the past 15 years [5]–[7],[11] and can be modeled using a first-order but accurate approximation as a direct change of the electron mobility. Thus the observed drain-source current change under mechanical stress can be written as:

$$\frac{\Delta I_{DS}}{I_{DS}} \approx \frac{\Delta\mu}{\mu} = \pi_N\cdot\sigma \equiv a_N, \quad (5)$$

where $\pi_N$ is the nMOSFET piezoresistance coefficient in $Pa^{-1}$, and $\sigma$ is the applied uniaxial mechanical stress in Pa. The piezoresistance coefficients of a certain technology can be experimentally determined and are dependent on the channel orientation of the MOSFET in respect to the direction of the applied uniaxial stress [7] and linearly dependent on the applied stress. Moreover, geometrical changes of $W$ and $L$ have been neglected in (5); an assumption that is valid for moderate stress levels (<250 MPa) [7]. Furthermore, the threshold voltage is essentially independent of stress [7]. For moderate stress levels $|a_N| \ll 1$ [5],[12]. Similar equations are also valid for pMOSFETs under stress.

Of great importance is to calculate the minimum input voltage $V_{in}$, which still maintains $M_{bias}$ in saturation under the unstressed and the stressed state. When the lower transistor is at the *verge of saturation* the following equations hold:

$$V_{out,SF} = V_{dsat,bias} = V_{bias} - V_T = V_{dsat,bias}^{\sigma} = V_{out,SF}^{\sigma}, \quad (6)$$

since $V_{bias}$ is a constant external reference voltage. Rewriting (4a) and (4b) under a stressed condition using (5) and (6) and assuming the general situation of different channel orientations of $M_{SF}$ and $M_{bias}$ we have:

$$I^{\sigma}_{bias}=\frac{\mu^{\sigma}_{n,bias}C_{ox}}{2}\left(\frac{W}{L}\right)_{bias}\cdot(V_{bias}-V_T)^2=(1+a_{N,bias})I_{bias} \quad (7a)$$

$$I^{\sigma}_{SF}=\frac{\mu^{\sigma}_{n,SF}C_{ox}}{2}\left(\frac{W}{L}\right)_{SF}\cdot(V^{\sigma}_{in}-V_{dsat,bias}-V_T)^2=I^{\sigma}_{bias} \quad (7b)$$

$$\mu^{\sigma}_{n,SF}=(1+a_{N,SF})\mu_{n,SF} \quad (7c)$$

Setting the two currents $I^{\sigma}_{bias}$ and $I^{\sigma}_{SF}$ equal and using (4a), (4b) and (6) we end up with a relation between the needed minimum overdrive input voltage in the stressed and unstressed condition in order maintain $M_{bias}$ in saturation:

$$V^{\sigma}_{ov}=\sqrt{\frac{(1+a_{N,bias})}{(1+a_{N,SF})}}V_{ov} \quad (8a)$$

$$V_{ov}=V_{in}-V_{bias},\ V^{\sigma}_{ov}=V^{\sigma}_{in}-V_{bias} \quad (8b)$$

The next step is to calculate the change of the source follower small-signal gain under stress, when both transistors are working in the saturation regime. First we calculate the changes of the transistors transconductances and output conductances under stress with the help of (4a)-(6c):

$$g^{\sigma}_{m,bias}=\sqrt{2\mu^{\sigma}_{n,bias}C_{ox}\left(\frac{W}{L}\right)_{bias}I^{\sigma}_{bias}}=(1+\alpha_{N,bias})\cdot g_{m,bias} \quad (9a)$$

$$g^{\sigma}_{m,SF}=\sqrt{2\mu^{\sigma}_{n,SF}C_{ox}\left(\frac{W}{L}\right)_{SF}I^{\sigma}_{SF}}=\sqrt{(1+\alpha_{N,SF})(1+\alpha_{N,bias})}\cdot g_{m,SF} \quad (9b)$$

$$g^{\sigma}_{ds,bias}\approx\lambda I^{\sigma}_{bias}=(1+\alpha_{N,bias})g_{ds,bias} \quad (9c)$$

$$g^{\sigma}_{ds,SF}\approx\lambda I^{\sigma}_{SF}=(1+\alpha_{N,bias})g_{ds,SF}, \quad (9d)$$

where λ is the channel length modulation coefficient.

Then we substitute these results in the well known formula for the source follower small signal gain as follows:

$$A^{\sigma}_{SF}=\frac{g^{\sigma}_{m,SF}}{g^{\sigma}_{m,SF}+g^{\sigma}_{ds,SF}+g^{\sigma}_{ds,bias}} \quad (10)$$

$$\Rightarrow A^{\sigma}_{SF}=\frac{g_{m,SF}}{g_{m,SF}+\sqrt{\frac{(1+a_{N,bias})}{(1+a_{N,SF})}}(g_{ds,SF}+g_{ds,bias})}\approx A_{SF}$$

where the body effect has been neglected and the output conductances are assumed to be substantially smaller than the transconductances.

Similarly, following the same technique for the source follower in Fig. 2b, its voltage gain and needed overdrive under mechanical stress are given by:

$$A^{\sigma}_{v}=\frac{g^{\sigma}_{m,SF}}{g^{\sigma}_{m,SF}+g^{\sigma}_{ds,SF}+g^{\sigma}_{ds,bias}} \quad (11a)$$

$$\Rightarrow A^{\sigma}_{SF}=\frac{g_{m,SF}}{g_{m,SF}+\sqrt{\frac{1}{(1+a_{N,SF})}}(g_{ds,SF}+g_{ds,bias})}\approx A_{SF}$$

$$V^{\sigma}_{ov}=\sqrt{\frac{1}{(1+a_{N,SF})}}V_{ov} \quad (11b)$$

,where $V_{ov}=V_{in}-V_{dsat,bias}-V_T$ and $V^{\sigma}_{ov}=V^{\sigma}_{in}-V^{\sigma}_{dsat,bias}-V_T$. In this case the current mirror adjusts the gate source of the lower transistor and hence its $V_{dsat}$, which can be again calculated using the square law equation similar to (4a) in the stressed and unstressed condition. In this case the transistors comprising the current mirror are assumed to be matched and in the same orientation on wafer. If the mirror transistors are placed with different orientation on chip, then a current mismatch is expected due to the different piezoresistance coefficients among the MOSFETs [8].

Equations (9a), (9b), and (10) as well as (11) and (12) provide us a valuable insight into the change of the output voltage of the presented source follower configurations. As depicted in Fig. 3, the input-output characteristic is expected to shift under stress for both circuits, maintaining however its slope (since the small signal gain $A_{SF}$ remains constant under stress). Hence, according to the configuration used, a drift $\delta^{\sigma}_{SF}$ of the output voltage can be calculated under a constant applied mechanical stress $\sigma$ and for a given $V_{in}$ using (8a) or (11) accordingly:

$$V^{\sigma}_{out,SF}=V_{out,SF}+\delta^{\sigma}_{SF} \quad (12)$$

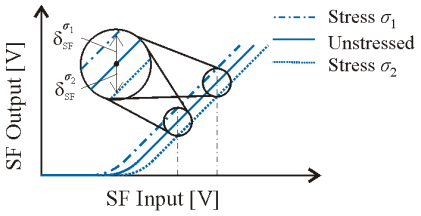


Fig. 3 Drift of the input-output characteristic of the presented source follower configurations under mechanical stress

### C. Correlated Double Sampling Circuit

In this subsection the last circuit of the readout chain is analyzed. This SC-correlated double sampler (CDS) consists of an amplifier using capacitive feedback and sampling switches. Two non-overlapping clocks $\varphi_1$ and $\varphi_2$ control the reset and sampling periods of the circuit. During $\varphi_1$ the CDS output is reset to $V_{bias,CDS}$. During $\varphi_2$ and with the right control of the select switch the *difference* of the values stored at the input terminals in two different time instants is stored at the capacitors. This difference multiplied by the amplification of the stage $A_{CDS}$, will then constitute the output of the readout chain.

Under mechanical stress the capacitances of $C_C$ and $C_F$ are considered in our analysis constant, since poly-poly on-chip capacitors can be used, where the capacitor value changes under moderate stress levels are assumed negligible. Next, the switches, typically realized using MOSFETs, will show some change of their charging characteristic under stress, as we

described in subsection II.*B*. The increase (decrease) of the drain current under stress will impact their charging ability and hence we expect a change of the needed charging or discharging time of the capacitors, without observing however a change on the final charge stored it the capacitors.

Furthermore, the amplifier used for our analysis, is a folded cascode amplifier. Mechanical stress will introduce changes both in his DC as well as AC characteristics, which can be calculated with the same technique used in II.*B*. However, the important parameter for this stage is the open loop gain of the amplifier $A_{CDS,OL}$, which will be also affected. This change is important when we analyze this amplifier in an open loop configuration. In our circuit though, we have a heavy feedback loop through $C_F$, and the close loop gain of the circuit will be equal to $A_{CDS}= C_F/C_C$, as long as the open loop gain of the amplifier remains high enough. Since the changes introduced from the application of moderate level of mechanical stress are small, we consider the closed loop gain of the amplifier to remain constant under stress. Hence the output of this stage under stress is considered constant and can be calculated using charge conservation as:

$$V_{out,CDS}= V_{ref}+A_{CDS}\left(V_{in}^{\varphi 2} - V_{in}^{\varphi 1}\right)=V_{out,CDS}^{\sigma}\,, \qquad (13)$$

where $A_{CDS}= C_F/C_C$ is the closed loop gain of the stage, $V_{ref}$ is the reference voltage needed to adjust the DC output level of the CDS circuit, and $V_{in}^{\varphi 1}$, $V_{in}^{\varphi 2}$ are the input voltages during $\varphi_1$ and $\varphi_2$ respectively.

### D. Overall Effect on the Signal C η

In this subsection the results of the previous subsections are all brought together in an aggregate relationship, which describes the overall effect of the pixel readout signal chain. Using (3), (10), (12), and (13) we end up with:

$$V_{out}= V_{ref}+A_{SF}A_{CDS}\left(V_{PD}-V_{pix}\right) \qquad (14a)$$

$$V_{out}^{\sigma}= V_{ref}+A_{SF}^{\sigma}A_{CDS}^{\sigma}\left(\left(V_{PD}+\delta_{SF}^{\sigma}\right)-\left(V_{pix}+\delta_{SF}^{\sigma}\right)\right) \qquad (14b)$$

Hence the relationship of the output voltage between the stressed and unstressed condition can be calculated as:

$$V_{out}^{\sigma}= V_{ref}+(1+a_{PD})A_{SF}A_{CDS}\left(V_{PD}-V_{pix}\right)$$

$$\overset{(14a)}{\Longrightarrow} V_{out}^{\sigma} - V_{ref} = (1+a_{PD})\left(V_{out}-V_{ref}\right) \qquad (15)$$

The last equation reveals, that the changes at the source follower output due to the application of uniaxial mechanical stress are suppressed by using the CDS stage at the end of the readout chain. Thus, the analog designer is free to decide the optimal source follower configuration for the most advantageous operation of the circuit. However the photodiode dependency on mechanical stress due to $\alpha_{PD}$ is fully reflected at the output. Therefore, this dependence should either be minimized by applying appropriate layout rules or compensated using for example a bank of compensating capacitors in the CDS stage.

## III. Simulation Technique and Results

In this section a novel, simple simulation technique is presented that enables to simulate mechanical stress on MOSFETs – and circuits – into Cadence® providing satisfying results when compared with the theoretical calculations. It is in general typical for a designer to layout transistors on chip having either a 0° or 90° channel orientation relative to the main crystallographic direction of the wafer, as shown in Fig. 4.

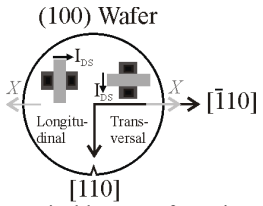


Fig. 4 Two typical layouts of transistors on chip

Moreover, applying a uniaxial mechanical stress using either a 4-point bending apparatus [6] or a cylindrical apparatus as the one the authors use [5], has as a result that the direction of the applied uniaxial stress is either parallel to or vertical to the channel orientation (current flow) of the layouted transistor on chip. Thus it is of great importance of a designer to be able to simulate the designed circuits under different mechanical stresses and under these two orientations of the transistors relative to applied stress.

As described in section II and using (5) we need to induce a drain-source current change by changing the mobility of the carriers, which in turn is linearly dependent on the applied mechanical stress $\sigma$ through the piezoresistive coefficient $\pi_N$ for nMOSFETs or $\pi_P$ for pMOSFETs. These coefficients depend also on the relative orientation of the applied stress to the current flow (channel orientation) of the transistor [5],[6]. Thus we have a set of four coefficients which should be determined experimentally, as shown in Table I:

TABLE I
Piezoresistive Coefficients of MOSFETs

| Coefficient | Orientation relative to applied stress |
|---|---|
| $\pi_{N,L}$ | Longitudinal NMOS |
| $\pi_{N,T}$ | Transversal NMOS |
| $\pi_{P,L}$ | Longitudinal PMOS |
| $\pi_{P,T}$ | Transversal PMOS |

Having these coefficients we can now embed them into our simulation software. However, changing the equations of the simulator, which compute the effective carrier mobility is not trivial and, of course, time-consuming. On the other hand a closer examination of the square law equation of a MOSFET in saturation (similar to (4a)) reveals that:

$$dI_{ds}\Big/d\mu_n = \frac{C_{ox}}{2}\left(\frac{W}{L}\right)_n\cdot(V_{GS} - V_T)^2 = I_{ds}\Big/\mu_n \qquad (16a)$$

$$dI_{ds}/dW_n = \frac{\mu_n C_{ox}}{2}\left(\frac{1}{L}\right)_n \cdot (V_{GS} - V_T)^2 = I_{ds}/W_n \quad (16b)$$

$$\xrightarrow{(16a)(16b)} \quad dI_{ds}/I_{ds} = d\mu_n/\mu_n = dW_n/W_n \quad (16c)$$

Equation (16c) suggest that an equal change of the drain-source current can be achieved by changing the width of the transistor for the same amount as (5) dictates, instead of changing its effective mobility. The advantage of this approach is that the designer has a direct access to the width of the device parameter through the properties window of the simulator. Moreover, callback functions can be easily integrated in Cadence®, which intervene and change automatically the entered width value from the user. Thus the simulator is fed with a slightly changed width value, which includes the effects of mechanical stress on the transistor DC characteristics. These callback functions need two parameters to calculate the change of the width, i.e., the value of the applied stress $\sigma$ and the orientation of the transistor channel to the applied uniaxial stress:

$$W_{sim} = W \cdot (1 + \pi\sigma) = W + W^{\sigma} \quad , \quad (17)$$

where $W_{sim}$ is the channel width used for the simulation, $W$ is the real channel width of the transistor, $W^{\sigma}$ is the added channel width used for the emulation of mechanical stress (can also take negative values), $\pi$ is one of the piezoresistive coefficients of Table I in $Pa^{-1}$, and $\sigma$ is the applied uniaxial mechanical stress in Pa. Equivalently stated, an extra transistor in parallel is connected to the one designed, in order to induce the current change observed under mechanical stress. As already mentioned in section II these changes are small for moderate stress levels (< 10%) and hence the added widths are much smaller in comparison to the real transistor widths.

However, adding even this relatively small transistor in parallel to the real one (layouted), introduces extra parasitic resistances and capacitances at its terminals, thus affecting its AC characteristics as well; a rather not desired situation. Therefore, another callback function is introduced, which actually stores the real width of the transistor $W$. This value is then used only for the calculation of the source/drain perimeter and area coefficients, which in turn are used to compute the parasitic capacitances of the device. As a result the parasitics are not scaled along with the change of the width of the device. Furthermore, the changed parasitic resistance due to the increased width could also introduce some errors. However, assuming that not the transistors with the shortest channel length in the underlying technology are used (which is typical in analog design), the parasitic resistance change of the MOSFET is much smaller than its channel resistance and thus not significantly affecting its performance. Simulation results of a source follower under diverse tensile mechanical stresses are depicted in Fig. 6 and 7, agreeing well with our theoretical calculations.

## IV. Design and Layout Considerations

In this section design and layout considerations are presented for minimizing (or maximizing in case of a stress sensor) the stress dependence of the analog circuit. In the case of matched transistors, for minimizing the dependence on stress and also keeping the matching in a high level, these should be layouted in the same orientation. Moreover, in a branch of a circuit comprised of only nMOSFETs or only pMOSFETs, the analog designer should also try to keep the orientation of these transistors the same. As a result all transistors would change their DC characteristics in the same direction under the application of uniaxial stress i.e., all would increase or decrease their current sink/source ability; hence moving not far away from their initial bias point design. If, however the transistors are placed in different orientations the bias point of the circuit is subject to greater changes. Similar observations are valid for a branch with pMOSFETs near the power line and nMOSFETs near ground.

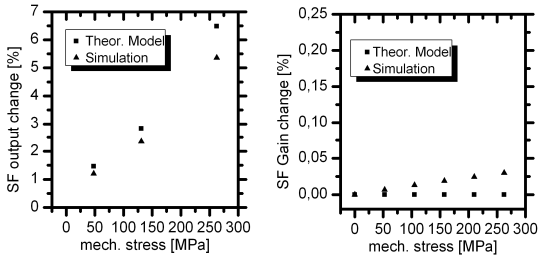


Fig. 6 Theoretical calculations vs. Cadence® simulation of a source follower under various tensile mechanical stresses

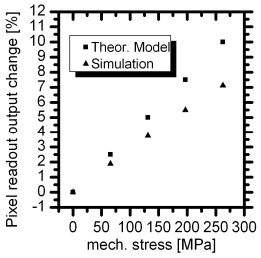


Fig. 7 Theoretical calculations vs. Cadence® simulation of the presented pixel readout chain under various tensile mechanical stresses

Using values from the literature [5],[7], it is advantageous to place pMOSFETs on a 90° channel orientation relative to the applied stress, while the nMOSFETs of the same branch on a 0° orientation, since they exhibit identical piezoresistive coefficients. Moreover, nMOSFETs placed on a 0° orientation relative to stress show a minimum dependence on the applied uniaxial stress. Another recommendation is that a bias point near the verge of saturation should be avoided (unless needed), since under even small uniaxial stress application the device could leave the saturation region and enter the linear region of operation; thus negatively influencing the operation of the circuit. Therefore, biasing in deep saturation is advisable. Moreover, minimum overdrive voltages should also be avoided. Biasing well above the threshold will also increase

the sensitivity even for very small threshold changes [7].

## V. Conclusion

The suppression of the effects of mechanical stress on the source follower of a pixel readout chain through the CDS stage is a very important result; the ultimate goal of the authors' research is to systematically analyze the behavior of a CMOS image sensor on ultra-thin bendable silicon (Si) chips as well as design it with a minimal stress dependence. The first pixel readout chains using the described technique have been designed and layouted and experimental results will be published shortly. Furthermore, the analysis technique presented in this paper, allows the analog designer to take into consideration the effects of uniaxial mechanical stress on the designed circuit. An apriori knowledge of the applied mechanical stress will be helpful in minimizing the effects of the mechanical stress on the circuit by following the proposed layout and design rules. Moreover, the presented simulation technique is a quick method for the designer to visually comprehend, how the circuit will behave under the stressed condition.

## Acknowledgment

The authors would like to thank the German Research Foundation for the financial support of this research.

## References

[1] D. Kim, N. Lu, R. Ma, Y. Kim, R. Kim, S. Wang, J. Wu, S. Won, H. Tao, A. Islam, K. Yu, T Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H. Chung, H. Keum, M. McCormick, P. Liu, Y. Zhang, F. Omenetto, Y. Huang, T. Coleman, J. Rogers, "Epidermal Electronics," *Science,* vol. 333, pp. 838–843, Aug. 2011.

[2] W. Wong, A. Salleo, (Eds.), *Flexible Electronics-Materials and Applications*. : New York: Springer-Verlag, 2009, pp. v-vi.

[3] J. Burghartz, W. Appel, C. Harendt, H. Rempp, H. Richter, M. Zimmermann, "Ultra-thin chip technology and applications, a new paradigm in silicon technology, " *Solid-State Electronics*, vol. 54, pp. 818–829, 2010

[4] M. Koganemaru, T. Ikeda, N. Miyazaki, and H. Tomokage, "Experimental Study of Uniaxial-Stress Effects on DC Characteristics of nMOSFETs," *IEEE Trans. Components and Packaging Technologies,* vol. 33, No. 2, pp. 278–285, June 2010.

[5] N. Wacker, H. Rempp, S. Schmiel, and J.N. Burghartz, "Accurate measurement of piezocoefficients in CMOS transistors on conventional and ultra-thin Silicon Chips," *Proc. SAFE*, pp. 605-608, Nov. 2008.

[6] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, and R. Gwoziecki,"Electrical analysis of external mechanical stress effects in short channel MOSFETs on (001) silicon," *Solid-State Electronics*, vol. 48, no. 4, pp. 561–566, 2004.

[7] A. T. Bradley, R. C. Jaeger, J. C. Suhling, and K. J. O'Connor, "Piezoresistive characteristics of short-channel MOSFETs on (100) silicon," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2009–2015, Sep. 2001.

[8] R. C. Jaeger, J. C. Suhling, R. Ramani, A. T. Bradley, and J. Xu, "CMOS Stress Sensors on (100) silicon," *IEEE Journal of Solid State Circuits*, vol. 35, no. 1, pp. 85–95, Jan. 2000.

[9] T. Wang, C. Ko; S. Chang, S.Wu, T. Kuan, and W. Lee, "The Effects of Mechanical Uniaxial Stress on Junction Leakage in Nanoscale CMOSFETs," *IEEE Trans. Electron Dev*ices, vol. 55, pp. 572-577, Feb. 2008.

[10] A. Hamada, T. Furusawa, N. Saito, and E. Takeda, "A new aspect of mechanical stress effects in scaled MOS devices," *IEEE Trans. Electron Devices*, vol. 38, no. 4, pp. 895–900, Apr. 1991.

[11] S. Dhar, H. Kosina, V. Palankovski, E. Ungersboeck, and S. Selberherr,"Electron mobility model for strained-Si devices," *IEEE Trans. Electron Devices*, vol. 52, no. 4, pp. 527–533, Apr. 2005.

[12] N. Wacker, H. Rempp, S. Schmiel, and J.N. Burghartz, "Compact Modeling of CMOS Transistors under Uniaxial Stress," *Proc. SAFE*, pp. 179-181, Nov. 2009