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Synchronization Technique for Random Switching Frequency Pulse-Width Modulation

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***Abstract*—**This paper proposes a synchronized random switching frequency pulse width modulation (SRSFPWM). In this technique, the clock signal is used to control the random noise frequency which is produced by the feedback voltage of a hysteresis circuit. These make the triangular carrier frequency equaling to the random noise frequency in each switching period with the symmetrical positive and negative slopes of triangular carrier. Therefore, there is no error voltage in PWM signal. The PSpice simulated results shown the proposed technique improved the performance in case of low frequency harmonics of PWM signal comparing with conventional random switching frequency PWM.

***Keywords*—**Random switching frequency pulse-width modulation.

I. Introduction

PULSE-WIDTH modulation (PWM) techniques have been widely used in power electronic systems. PWM techniques generally operate with a fixed switching frequency causing power spectrum to be concentrated at multiples of the switching frequency. This gives rise to the harmonic spikes and can produce unwanted effects in the power converter such as acoustic noise, torque ripple, and electromagnetic interference (EMI). If these effects are the concerned problems, frequency modulation (FM) and random switching frequency PWM (RSFPWM) techniques were used to distribute the harmonic powers over the spectrum resulting the harmonic spikes reduced [1-4].

However, there are some concerned problems in RSFPWM techniques because they can produce low frequency harmonics at PWM signal. These low frequency harmonics generate the low frequency ripples at the converter output voltage increasing total harmonic distortion (THD). Therefore, this paper proposes the synchronized random switching frequency PWM. The processing of synchronization of the clock signal frequency with triangular carrier frequency is explained. The simulated results by Pspice program are shown that the low frequency ripples at the buck converter output reduced.

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II. Constant Switching Frequency PWM

In the constant switching frequency pulse-width modulation (CSFPWM) technique, a triangular carrier signal that consists of the symmetrical negative and positive slopes is compared with a reference signal v_{ref} to obtain PWM switching gate drive as shown in Fig. 1 (a) and (b). The modulation index M is determined by

$$M = \frac{v_{ref}}{v_p} \tag{1}$$

where

v_{ref} is the amplitude of reference signal.

v_p is the maximum voltage of triangular carrier.

The switching time $t_{(+)}$ and $t_{(-)}$ are the functions of modulation index and the time constant of integrator circuit.

$$t_{(-)} = \frac{v_p(1+M).V_s}{RC} \tag{2}$$

$$t_{(+)} = \frac{v_p(1+M).V_s}{RC} \tag{3}$$

Fig. 1 (c) shows the harmonic spectrum of v_{pwm} that consists of the fundamental and high peak harmonics concentrated at the multiples of switching frequencies, f_s.

In the RSFPWM technique, a random noise is used to control the triangular carrier frequency[4]. Therefore, the frequency of PWM is randomly distributed in wide frequency range causing the harmonic spectrum reduction as shown in Fig. 1 (d) – (f). Although, this process can solve the problem of harmonic peaks, it causes low frequency harmonics as shown in Fig. 1 (f). These harmonics produce low frequency ripples at converter output voltage increasing the total harmonic distortion (THD)[3].

III. Synchronization Random Switching Frequency PWM

In CSFPWM the both slopes of triangular carrier v_{tri} are symmetrical every cycle period. There is therefore no error in this process resulting without low frequency harmonics. In RSFPWM the random noise $\pm v_n(t)$ generated by pseudo random binary sequence (PRBS) is added with $\pm V_{dc}$ voltage applying as the input of integrator circuit to generate the negative and positive slopes of v_{tri}, as shown in Fig. 2 (a).

Assuming the positive slope is generated by $-V_{dc}-v_n(t)$ in period of t_n while the negative slope is generated by $+V_{dc}+v_n(t)$ in period of t_{n+1}. This shows that the negative slope is not equal to the positive slope. This causes the duty cycle error in some periods of RSFPWM, which acts the noise source producing the low frequency harmonics. Fig. 2 (b) shows the block diagram of the proposed technique SRSFPWM.

The clock signal will be produced from the output of hysteresis circuit. Assuming the PRBS operates at the rise edge of clock signal. At the time period t_{clk1} the control switch S(+) is the positive pulse used to be the clock signal of PRBS. The voltage level of random noise $n_s(t)$ is changed by the triggering of S(+). This $n_s(t)$ voltage level will be used to produce the positive slope while the negative slope is still produced from the same $n_s(t)$ voltage level. Therefore, the both slopes are symmetrical in this time period. When the next control switch S(+) arrives, this process will be repeated. This process makes the clock signal frequency as same as the triangular carrier frequency. However, the clock signal frequency affects the harmonic distribution [4].

Therefore, the N-counter is used to control the speed of PRBS. In Fig. 2 (b) the counter is set by two. This gives two pulses of v_{tri} that are symmetrical in each period of clock signal. Therefore, this technique guarantees no duty cycle error when it is used in PWM process. Fig. 2 (c) shows the approximation of error in RSFPWM process. In Fig. 2 (c) the dash and dot lines are asymmetrical and symmetrical triangular carriers, which are used to produce PWM signals.

The error voltage pulses are approximated by symmetrical PWM, $v_{srsfpwm}$ subtracting with asymmetrical PWM, v_{rsfpwm}. The error time t_{err} can be approximated by

$$t_{err} = \frac{v_p(1+M).n_s(t)}{RC} \tag{4}$$

In order to reduce the error time; 1) the time constant of integrator circuit should be small. This means the switching frequency increased resulting high switching loss. 2) the amplitude of random noise voltage, $n_s(t)$ should be low. However, it affects the amplitude of harmonic distribution[4]. 3) the modulation index M should be low. However, some applications need using high M. Therefore, a good random PWM technique should be considered these requirements.

IV. Simulated Results

Fig. 3 (a) shows the buck converter used in the simulation by Pspice program comparing between the proposed and conventional techniques. The parameters are set as following: f_{smin} = 3.5 kHz, f_{smax} = 8.5 kHz, PRBS is set 8 Bits, v_p = 2 V, and M = 0.5. The parameters of FFT are set at the period time 200ms and frequency resolution 5 Hz. The simulated results of the PWM waveforms are shown in Figs. 4 and 5.

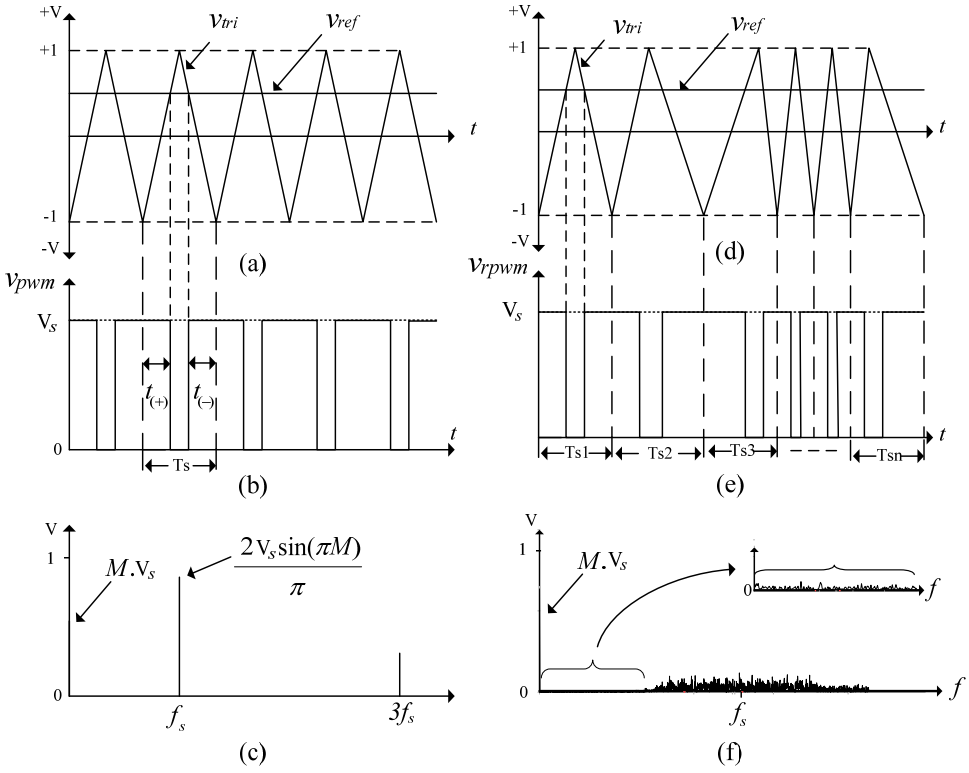

Fig. 1 Waveforms of (a)-(c) CSFPWM and (d)-(f) RSFPWM

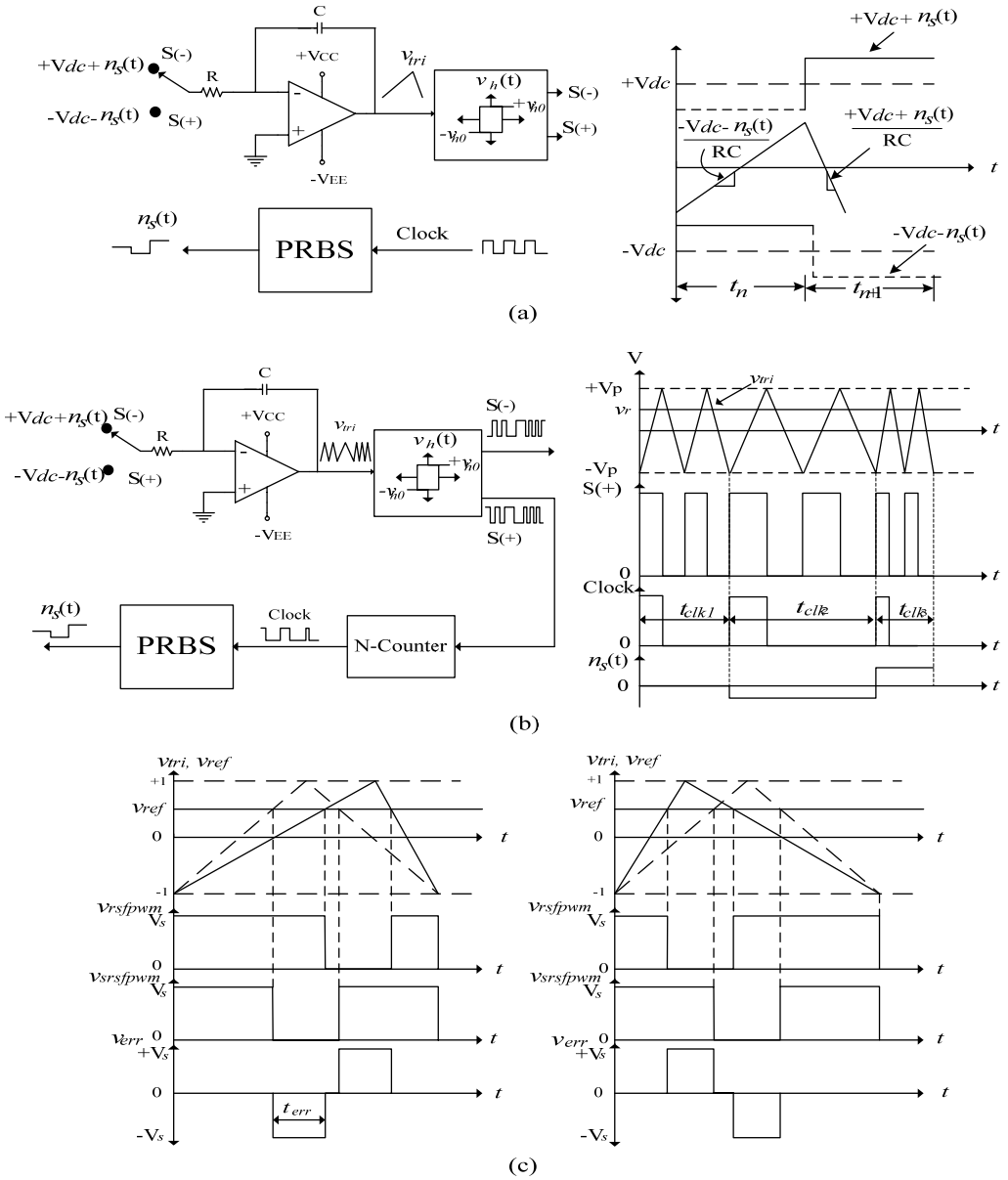

Fig. 2 Block diagram of (a) the conventional RSFPWM and (b) the proposed SRSFPWM. (c) Error approximation

In Fig. 4 showing the results of RSFPWM process, the slopes of triangular carrier are asymmetrical causing duty cycle error in some periods. Fig. 5 shows the results of SRSFPWM process, the frequency of clock signal is synchronized with triangular carrier every period. This means the negative slope equaling to positive slope in each period resulting no duty cycle error. The PWM signal in Figs. 4 and 5 were used to control the buck converter. Their results are shown in Fig. 6 and 7. Fig. 6 shows the simulated results of RSFPWM. It produces the low frequency ripples in the inductor current and output voltage of buck converter. Because the harmonic spectrum of v_D consists of low frequency harmonics, therefore, the low-pass filter can not suppress these harmonics. The low frequency ripple problem causing from RSFPWM can be solved by SRSFPWM technique as shown in Fig. 7. These simulated results are concluded in Fig. 8. It shows the percentage of ripple output voltage of SRSFPWM technique is lower than that of RSFPWM technique. The other important parameter that uses to measure the performance of random PWM techniques is the harmonic peak. The simulated results in Fig. 9 are to measure the harmonic peak at low and high frequency range. At low frequency range 1-1000Hz, it shows that the amplitude of harmonic peak of RSFPWM is lower than that of SRSFPWM technique. At high frequency range, RSFPWM process has a

good characteristic of harmonic distribution with low frequency of clock signal. This results the harmonic peak reduction. In SRSFPWM technique the N-counter affects the harmonic distribution. At low N-counter the harmonic peak is lower than at high N-counter.

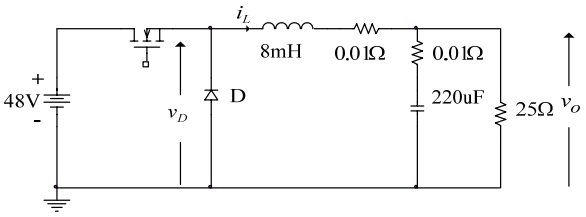

Fig. 3 Buck converter circuit

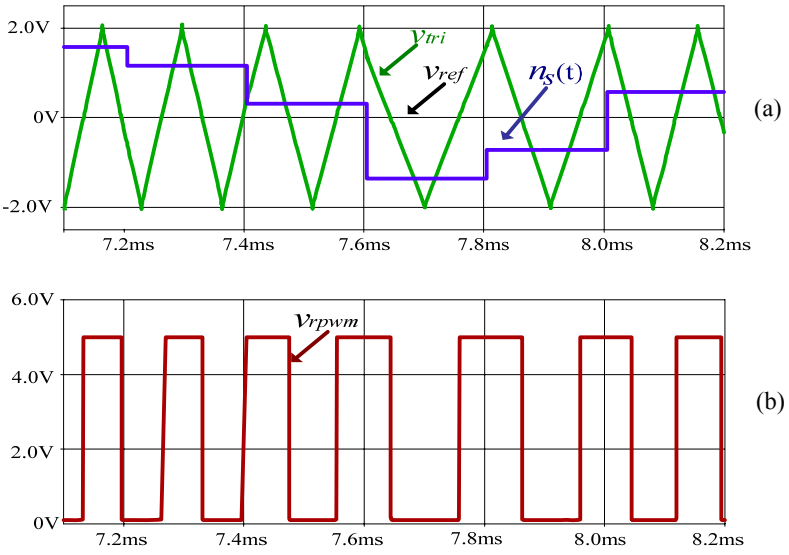

Fig. 4 Waveforms of RSFPWM. (a) v_{tri}, v_{ref}, and $n_s(t)$ and (b) PWM signal

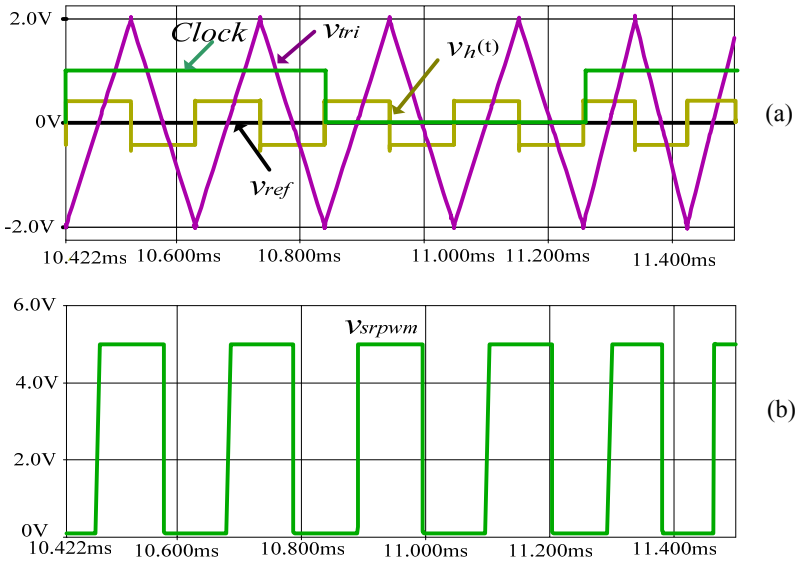

Fig. 5 Waveforms of SRSFPWM. (a) v_{tri}, v_{ref}, and $n_s(t)$ and (b) PWM signal

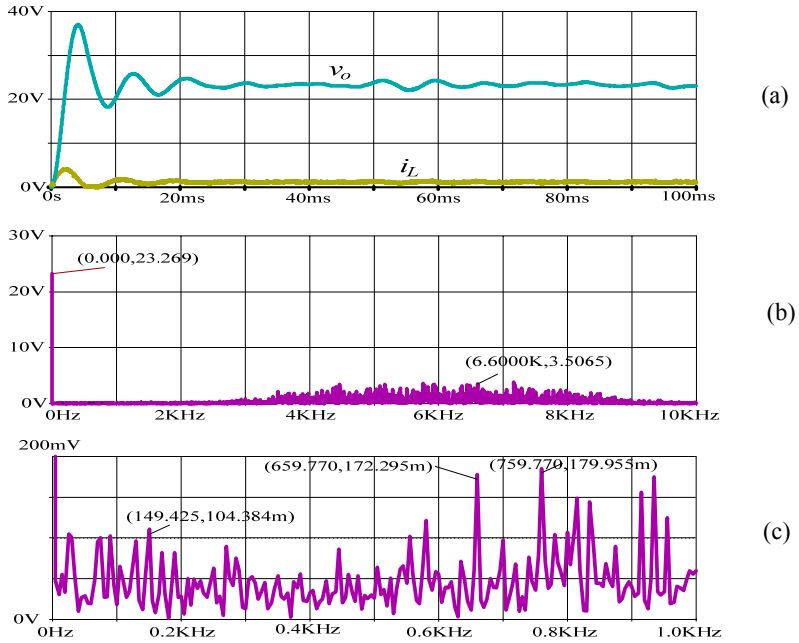

Fig. 6 Waveforms in buck converter controlled by RSFPWM; f_{clk}=3 kHz and M = 0.5
(a) Output voltage, v_o and inductor current, i_L.
(b) and (c) Harmonic spectrum of v_D in high and low frequency rang

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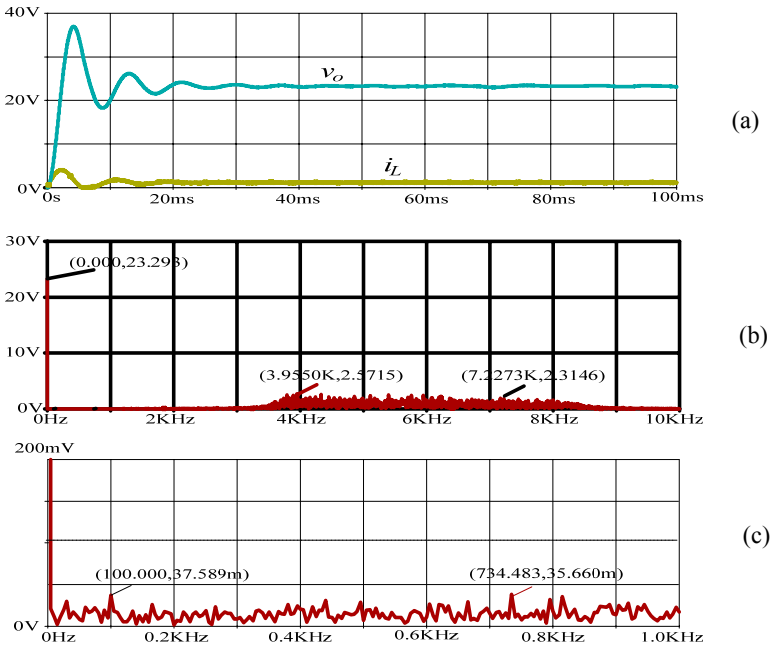

Fig. 7 Waveforms in buck converter controlled by SRSFPWM; N=2 and M = 0.5
(a) Output voltage, v_o and Inductor current, i_L.
(b) and (c) Harmonic spectrum of v_D in high and low frequency rang

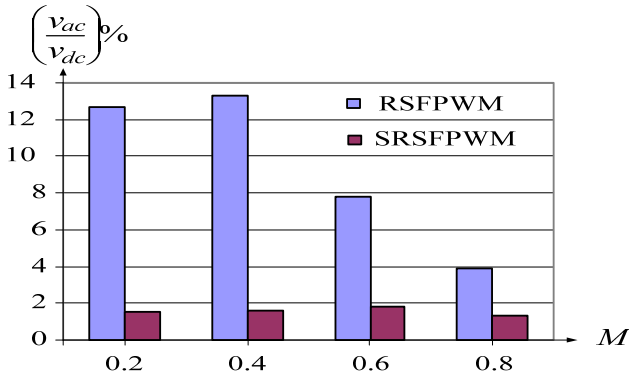

Fig. 8 Percentage of ripple output voltage; RSFPWM uses f_{clk} = 3 kHz and SRSFPWM uses N=2

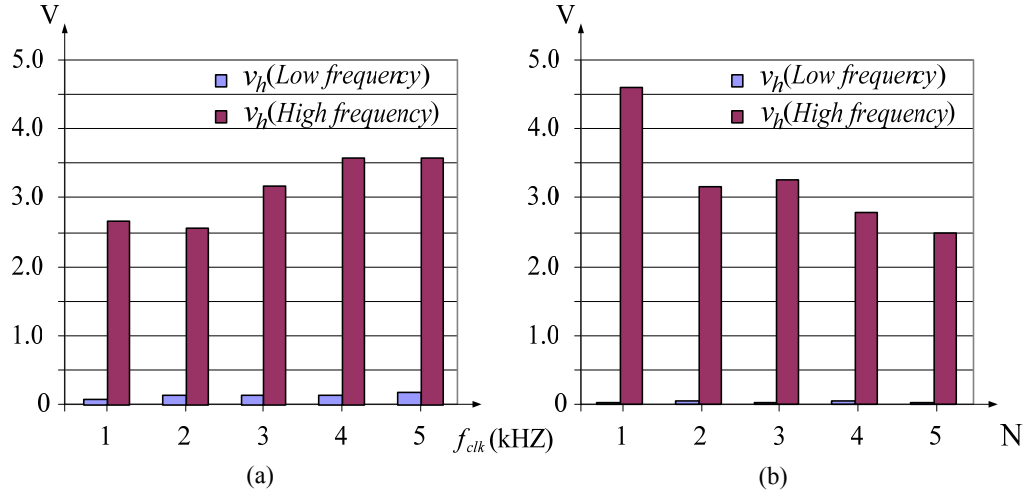

Fig. 9 Amplitude of harmonic peak of (a) RSFPWM and (b) SRSFPWM; M = 0.5

V. Conclusion

This paper proposed the synchronized random switching frequency PWM technique. The problem of asymmetry of slopes of triangular carrier is eliminated. The simulated results show that the proposed technique can reduce the low frequency ripples of output voltage up to 11 percent at M = 0.2 when compared with conventional random switching frequency PWM technique.

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