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Switching Behaviors of $HfO_2/NiSi_x$ Based RRAM

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***Abstract*—**This paper presents a study of Ni-silicides as the bottom electrode of HfO_2-based RRAM. Various silicidation conditions were used to obtain different Ni concentrations within the Ni-silicide bottom electrode, namely Ni_2Si, NiSi, and $NiSi_2$. A 10nm HfO_2 switching material and 50nm TiN top electrode was then deposited and etched into 500nm by 500nm square RRAM cells. Cell performance of the Ni_2Si and NiSi cells were good, while the $NiSi_2$ cell could not switch reliably, indicating that the presence of Ni in the bottom electrode is important for good switching.

***Keywords*—**HfO_2-based, Ni-silicide, NiSi, resistive RAM (RRAM).

I. Introduction

RESISTIVE RAM (RRAM) has been researched extensively in recent years to address scaling issues in flash memories based on charge-trapping non-volatile memory (NVM) [1]-[12]. The fast program/erase and low operating voltages make it suitable either for embedded NVM or stand-alone NVM using standard CMOS process. Furthermore, the simple metal-insulator-metal structure of the RRAM allows for high density integration.

A popular choice of top metal electrode and dielectric is TiN/HfO_2 [10]-[12]. Oxygen vacancies are believed to form within the HfO_2 due to the applied electric field during SET process as the TiN acts as an oxygen gettering layer. The oxygen is then released back into the HfO_2 during the RESET process.

This work presents a study of Ni-silicide as the bottom electrode, with HfO_2 as dielectric and TiN as top electrode. Various silicidation conditions were used to form Ni-silicides with different Ni concentrations, namely Ni_2Si, NiSi, and $NiSi_2$. It was found that the Ni_2Si and NiSi cells performed well, while the $NiSi_2$ cell could not switch reliably, indicating that the presence of Ni in the bottom electrode is important for good switching.

II. Device Fabrication

Devices were fabricated on *p*-type (~10^{15} cm^{-3}) 8-inch silicon wafers. The bottom electrode (BE) was first formed through silicidation of the silicon substrate under the various conditions listed in Table I. First, Ni is deposited and then the first silicidation performed at high temperatures. Excess Ni is then removed by wet etch in H_2SO_4:H_2O_2:H_2O solution after the first anneal. A second anneal is done after the Ni removal for D3 only. After silicidation, 10nm HfO_2 switching oxide and 50nm TiN top electrode (TE) were deposited through physical vapor deposition (PVD). The TE was then patterned into 500nm by 500nm patterns by lithography using a 248nm KrF scanner. The TE is then dry etched using Cl_2 chemistry. SiO_2 is then deposited as pre-metal deposition (PMD) and contact holes etched to contact TE and BE. This is followed by metallization with Al using TaN as a barrier metal.

Figs. 1 (a) to (c) show the transmission electron micrographs (TEM) images of D1-D3, respectively. Fig. 1 (d) to (f) shows the energy dispersive x-ray spectroscopy (EDX) line scans of D1-D3, respectively. It is clear from the EDX that the Ni concentration is highest for D1 and lowest for D3, with D2 having a concentration between the two.

III. Results and Discussion

Figs. 2 (a) to (c) show the typical switching characteristics of D1-D3, respectively. It can be seen that the switching current tends to be high (>1mA). This could indicate a large filament is formed during the forming/SET. Also, the SET voltages are fairly low (~0.6V for D1 and ~0.8V for D2). Unfortunately, D3 fails to switch after the forming process, which could be due to the low Ni concentration.

The memory window for D1 and D2 is >10x, which should be sufficient to resolve both low resistance state (LRS) and high resistance state (HRS). D2 appears to have a slightly larger memory window, with one RESET cycle even causing the HRS to drop lower than the typical HRS level, resulting in nearly a 100x memory window. However, this phenomena was found to only occur sometimes. Although D2 was found to be the best performing cell, it should be noted that the Ni-silicide surface of the BE is quite rough, as can be seen in Fig. 1 (b). This could result in some switching non-uniformity. This could also be the reason for the large drop in current during that one RESET process. Conversely, this could also possibly result in over SET or negative parasitic SET.

TABLE I
Nickel Silicdation Conditions for Bottom Electrodes

Device	D1	D2	D3
Ni thickness	30nm	30nm	15nm
Silicidation 1st step	300°C, 30sec	440°C, 30sec	220°C, 120sec
Silicidation 2nd step	None		440°C, 30sec

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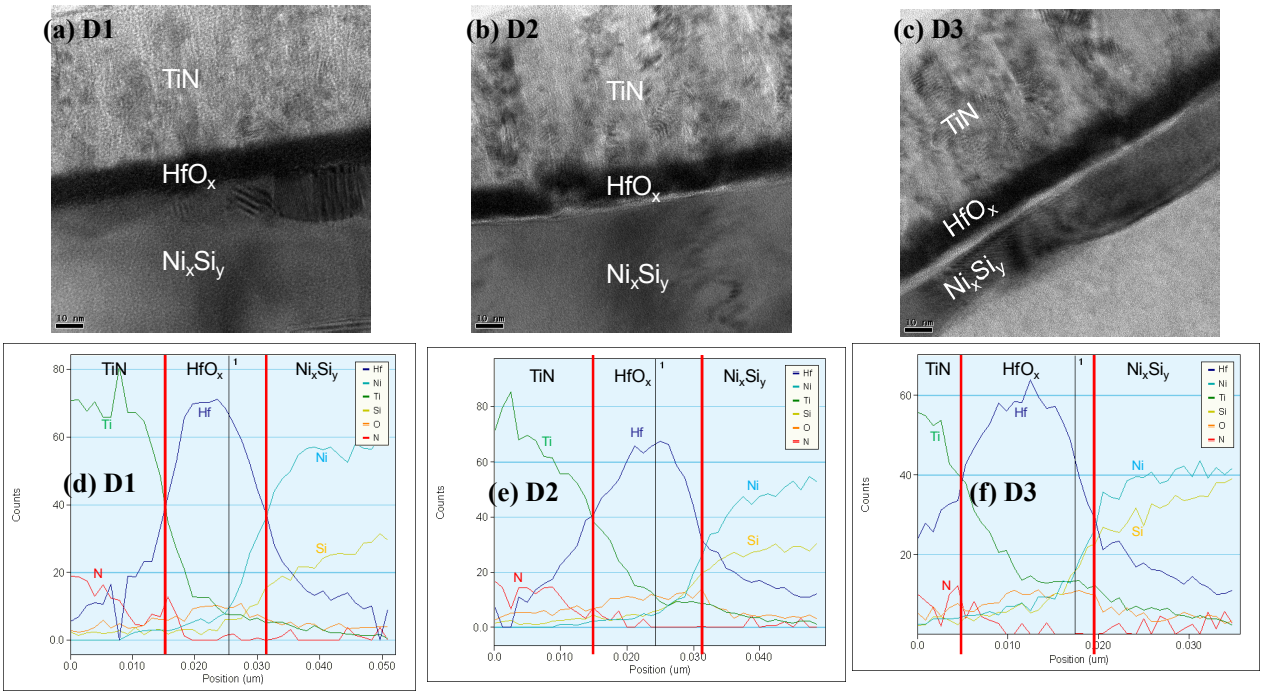
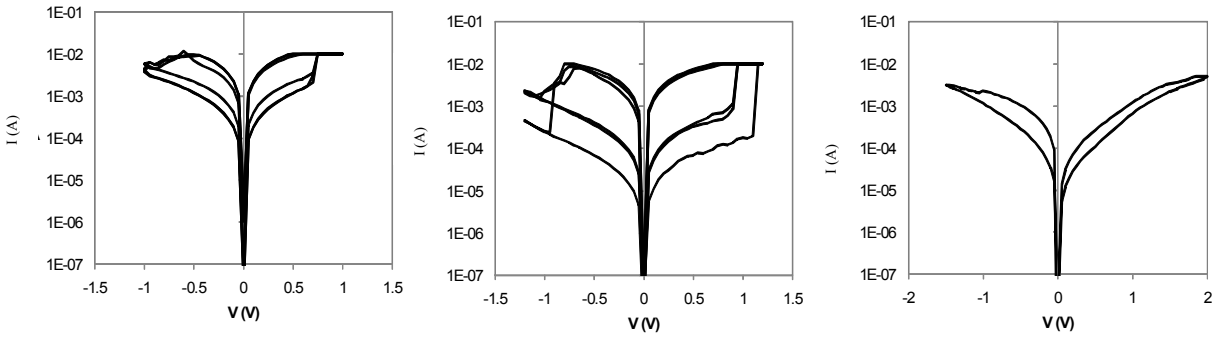


Fig. 1 (a)-(c) Transmission electron micrographs (TEM) and (d)-(f) electron dispersive x-ray spectroscopy (EDX) line scans from TiN to Ni-silicide of the various devices, D1-D3, respectively



(a) D1 (b) D2 (c) D3

Fig. 2 (a)-(c) Switching I-V characteristics of the various devices, D1-D3, respectively

IV. Conclusion

A study of Ni-silicide as the bottom electrode of RRAM is presented. HfO_2 was the dielectric and TiN was the top electrode. Various silicidation conditions were used to form Ni-silicides with different Ni concentrations, namely Ni_2Si, NiSi, and $NiSi_2$. It was found that the Ni_2Si and NiSi cells performed well, while the $NiSi_2$ cell could not switch reliably, indicating that the presence of Ni in the bottom electrode is important for good switching.

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