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Sigma-Delta ADCs Converter a Study Case

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***Abstract*—**The Sigma-Delta A/D converters have been proposed as a practical application for A/D conversion at high rates because of its simplicity and robustness to imperfections in the circuit, also because the traditional converters are more difficult to implement in VLSI technology. These difficulties with conventional conversion methods need precise analog components in their filters and conversion circuits, and are more vulnerable to noise and interference. This paper aims to analyze the architecture, function and application of Analog-Digital converters (A/D) Sigma-Delta to overcome these difficulties, showing some simulations using the Simulink software and Multisim.

***Keywords*—**Analysis, Oversampling Modulator, A/D converters, Sigma-Delta.

I. Introduction

THE sigma-delta conversion [1]-[3] technique exists for several years but its most extensive use was made possible due to technological advances like the advent of digital signal processors implemented in VLSI technology [4], which brought the need for A/D converters, high- resolution that could be integrated into the manufacturing process optimized for digital circuits and systems. In the literature, we can find several application and research [5], [6].

In addition, the implementation of sigma-delta conversion was made possible by the continuous improvement in digital signal processors, also in order to mitigate limits in the dynamic range available for the implementation of the interfaces between analog and digital representation of signals.

The A/D converters based on sigma-delta modulation (ΣΔ) [5], [6] combine high sampling rates with the Nyquist frequency with feedback and digital filtering in order to exchange resolution in time for amplitude. These converters are insensitive to circuit imperfections and component mismatches since they employ only a simple two-level quantizer and embedded quantizer within a feedback loop.

A ΣΔ modulator [7], therefore, provide a mean of exploring the higher density and speed of VLSI digital circuits, to avoid the difficulty of implementing complex functions of analog circuits within a limited dynamic range analog [6].

A ΣΔ modulator consists [7] of an analog filter, quantizer with a negative feedback. The feedback acts to reduce the noise of quantization at low frequencies, while emphasizing the high frequency noise.

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Once the signal is sampled with a frequency that is much larger than the Nyquist rate, the quantization noise of high frequency can be removed without affecting the signal bandwidth by a digital low-pass filter operating in ΣΔ modulator output.

The modulator has first order, whereas the filter consists of a simple integrator. However, the quantization error of the first order modulator is highly correlated and the oversampling ratio to achieve a higher resolution than 12 bits is incredibly high. First order modulator can be extended to higher orders.

In this work a first order ΣΔ converter will be analyzed and simulated to show the simplicity and scalability.

II. Digital Modulation

The principles of operation of A/D Sigma-Delta [1]-[4], are linked to concepts that will be demonstrated in the following topics.

A. Quantization

First, amplitude quantization and sampling in time are the important parts of digital modulators. Regular sampling at rates greater than twice the bandwidth of the signal does not introduce distortion, but the quantization introduces. The primary objective in the design of modulators is to limit this distortion. Starting a description of some basic properties of quantization will be useful to specify the noise modulators. Fig. 1 shows the uniform quantization of a ramp signal and its quantization error [1]-[7].

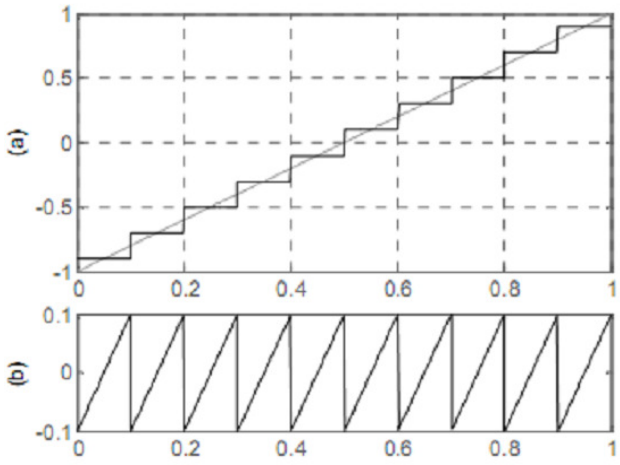

Fig. 1 (a) Ramp Signal; (b) Quantization error

It will be useful to represent the signal quantized x by a linear function G with an error e then we have:

$$y = Gx + e \quad (1)$$

The gain *G* is the slope that passes through the center of the quantization characteristic then, if the quantizer does not saturate, the error is bounded by ± Δ/2.

The error is completely defined by the entrance, but if the input changes randomly between the samples in amounts comparable to or exceeds the threshold spacing without causing saturation, then the error is uncorrelated from sample to sample and has equal probability of being anywhere in the range ± Δ/2.

If we assume that the statistical error has properties that are independent of the signal, then we can represent it by a noise, and some of the most important modulator properties can be determined.

In many cases, experiments can confirm these properties, but there are two cases that cannot apply these concepts. Note that, if the input is constant or when changes regularly by multiples or submultiples of the size of the sampling step, for example as in feedback circuits.

The quantization error *e* has an equal probability of being anywhere in the range ± Δ/2, its average value is given by:

$$e_{RMS}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \quad (2)$$

We use a one-sided representation of frequencies, in other words, we assume that all power is in the range of positive frequencies.

When a quantized signal is sampled in the frequency f_s=1/*T*, all energy is concentrated in the frequency range $0 \leq f < f_s/2$. So, if the quantization noise spectral density is white noise, the samples are given by:

$$E(f) = e_{RMS}\sqrt{\frac{2}{f_s}} = e_{RMS}\sqrt{2T} \quad (3)$$

We can use this result to analyze examples of oversampling modulators.

A signal in the frequency range $0 \leq f < f_o$, for a sign contained in the band $f_o \leq f < f_s / 2$ is added, it needs to be modulated by f_s. The oversampling ratio (OSR), defined as the ratio of the sampling frequency f_s and the Nyquist frequency $2f_o$ is given by:

$$OSR = \frac{f_s}{2f_o} = \frac{1}{2f_oT} \quad (4)$$

If the signal excitation is sufficiently large and uncorrelated the quantization error, the noise power that falls into the signal band will be given by:

$$n_o^2 = \int_0^{f_o} e^2(f)df = e_{RMS}^2(2f_oT) = \frac{e_{RMS}^2}{OSR} \quad (5)$$

So as result of the oversampling, the noise entry reduces. Therefore, each sampling frequency double reduces the input noise by 3*dB*, increasing the resolution in only half a bit.

B. First-Order Feedback Quantizer

An oversampling quantizer more efficient is the sigma delta modulator (ΣΔ) shown in Fig. 2 [1].

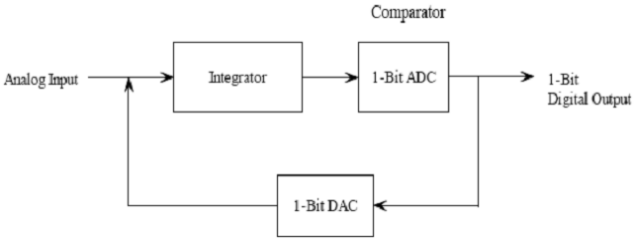

Fig. 2 Block diagram of a first order sigma-delta modulator.

The ΣΔ modulators usually are used with two quantization levels. In this work will be used a first-order modulator to demonstrate the operation of these converters. The input circuit feeds the quantizer via an integrator and the quantized output is feedback to a subtraction of the input signal. This feedback forces the average value of the quantized signal to achieve an average value of the entry. Any persistent difference between the two is the accumulative error in the integrator that eventually corrects it.

C. Modulation Noise in Busy Signals

Analysing the sigma-delta modulator block diagram depicted in Fig. 2, we can add a signal which represents the quantization error of the equation and a gain G defined as quantization unit.

Because of these data samples of the circuit, we represent the integration of accumulation, also with a unity gain. Can easily be shown that the output of the accumulator is:

$$w_i = x_{i-1} - e_{i-1} \quad (6)$$

and the quantized signal is:

$$y_i = x_{i-1} + (e_i - e_{i-1}) \quad (7)$$

Then the circuit differentiates the quantization error, making the error of modulating the first difference of the quantization error while leaving the signal unchanged, except if there is any delay.

To calculate the effective resolution of the ΣΔ modulator, we assumed the signal has white noise, which is the error is uncorrelated with the signal. The spectral density of the modulation noise can be expressed as:

$$n_i = e_i - e_{i-1} \quad (8)$$

$$N(F) = E(F)\left|1 - \varepsilon^{-j\omega T}\right| = 2e_{RMS}\sqrt{2T}\sin\left(\frac{\omega T}{2}\right) \quad (9)$$

where

$$\omega = 2\pi f$$

In the Fig. 3, we compare the spectral density with the spectral density of quantization noise when the oversampling ratio is 16. Clearly, the feedback around the quantizer reduces the noise at low frequencies but increases at high frequencies.

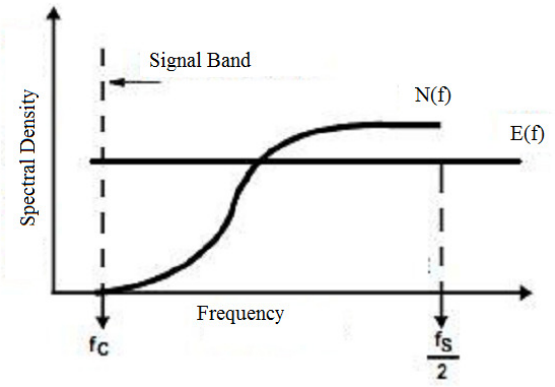

Fig. 3 The density of the noise *N(f)* from ΣΔ quantization compared with that of ordinary quantization *E(f)*.

The total noise power in the signal band is given by:

$$n_0^2 = \int_0^{f_0} |N(f)|^2 df \approx e_{RMS}^2 \frac{\pi^2}{\sqrt{3}} (2f_0T)^3 f_s^2 \gg f_0^2 \qquad (10)$$

and its RMS value yields:

$$n_0 = e_{RMS} \frac{\pi}{\sqrt{3}} (2f_0T)^{3/2} = e_{RMS} \frac{\pi}{\sqrt{3}} (OSR)^{-3/2} \qquad (11)$$

Each oversampling ratio by a factor of 2 in this circuit reduces noise by 9*dB* and increases 1.5 extra bits in resolution. The improvement of the resolution requires that the modulated signal is decimated to the Nyquist frequency using a digital selective filter. Otherwise, the components of high frequency noise will affect the resolution when it is sampled in the Nyquist frequency.

In [2] [3], we find how the RMS noise of a PCM signal can be expressed as $\sqrt{2}e_{RMS}(2f_0T)$. Therefore taking a triangularly weighted sum over each Nyquist interval gives an RMS noise $4e_{RMS}(2f_0T)^{1.5}$. An optimization of these techniques for attenuating the high frequency noise is demonstrated in [4]. This decimation allow more noise in the signal band than those using filters with impulse response that are longer than a Nyquist interval, but such techniques have been used because of simple circuit implementation.

III. Decimating the Modulated Signal

Decimation is the name given to the process that reduces the word rate of encrypted signals digitally that was sampled above the Nyquist frequency [1], [4]. Changing the word size usually results in reduced bit rate. The value of this exchange depends on the type of coding involved. For example, the quantization noise PCM is decreased by 6*dB* for each bit more in word, but it decreases only 3*dB* for each doubling in the rate of sampling.

So, decimating a PCM signal results in drastic bitrate decrease because their code is inefficient. A more efficient way is the oversampling ΣΔ modulation, where the quantization noise can be reduced by more than 15*dB* for each doubling in sampling rate.

A proper decimation is required for down sampling the bit rate modulation ΣΔ and converts it into a form more suitable for processing and transmission. A popular approach in the design of decimation filters for ΣΔ converters is based on the structure of multistage as can be seen in Fig. 4.

Fig. 4 Multistage decimator

This approach has become more popular due to the fact that this filter implementation usually has fewer coefficients. For example, we can convert a human voice signal, which is sampled at 8*k*Hz, using a ΣΔ conversion that have generally a factor 64 times oversampling, thus the sampling frequency of this signal is 512*k*Hz.

In decimation stage, we chose a multistage decimation, where each stage is a FIR filter. Each stage decreases the frequency in four times and, consequently, the word size increases, maintaining the output frequency of the last stage with 8 *k*Hz. During the process the quantization noise of the high frequencies introduced by the feedback were removed and also the unwanted frequency components in addition to f_s / 2 (4 *k*Hz).

IV. Project of a ΣΔ Converter

In this work will show a ΣΔ converter, demonstrating the implementation of each part of the circuit according to the theory explained in the previous sections. A ΣΔ converter is always composed of decimation filters and a modulator, which produces the bitstream data.

The bitstream data signal is represented by a series of bits, with a rate much higher than the data rate of the A / D. Its main property is the average that represents the input signal level. Its digital outputs *high* and *low* are, respectively, the highest and lowest possible output values. The ΣΔ modulator is the core of oversampling ΣΔ converters, this part produces a continuous stream of bits.

In this work we designed a first order modulator which it is enough to demonstrate the features of this type of modulation. Higher-order modulators can be implemented from that, just using a cascade configuration. In Fig. 5 can be seen a model of a first order ΣΔ modulator.

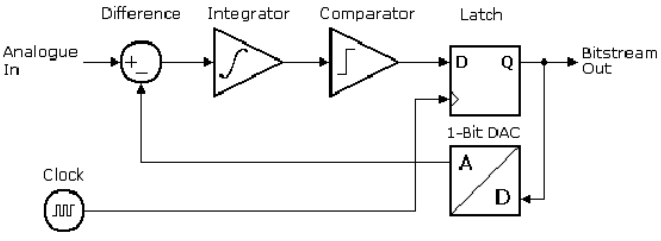

Fig. 5 First order ΣΔ modulator

The modulator works as in Fig. 6.

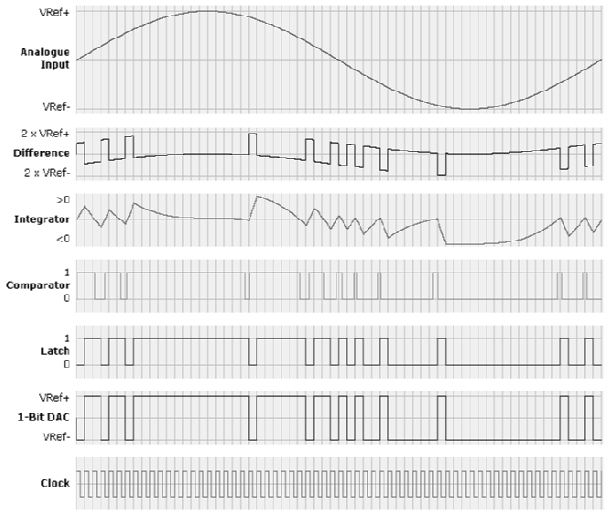

Fig. 6 Signals within a First Order Analogue Modulator

This work has being done to convert a sine wave of 1V amplitude with a frequency of 3.4 *k*Hz in order to simulate how it would be a conversion of a voice signal. The comparator checks if the output of the integrator is greater than 0 and is given a pulse of 5V to feed the flip-flop if it is true, otherwise it is issued 0V output from the comparator.

The oversampling frequency is controlled by the clock used in the flip-flop, in our case the Nyquist frequency $f_s = 2f_0$, i.e., f_s = 8 *k*Hz is the sampling frequency used for most voice signals. In this context the oversampling frequency used is 64 times the Nyquist frequency. For these parameters the clock of the modulator is 512 *k*Hz. For the 1-bit D/A encoder which is used in the feedback we used a comparator to check the flip-flop output. If the output is 0, the comparator uses the reference voltage of 1V and transforms the signal 0 to -1V, if the flip-flop is one; its voltage is 5V which was lowered to the reference voltage of 1V.

The comparators output is used as feedback to the circuit by making a subtraction of the input signal. The modulator circuit can be seen in Fig. 7.

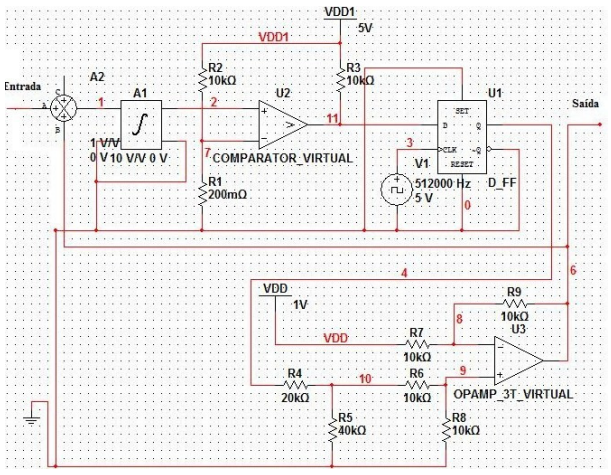

Fig. 7 ΣΔ modulator circuit

The circuit of the modulator was implemented in Multisim® software. For purposes of comparison Fig. 8 shows the modulator's bitstream input and output.

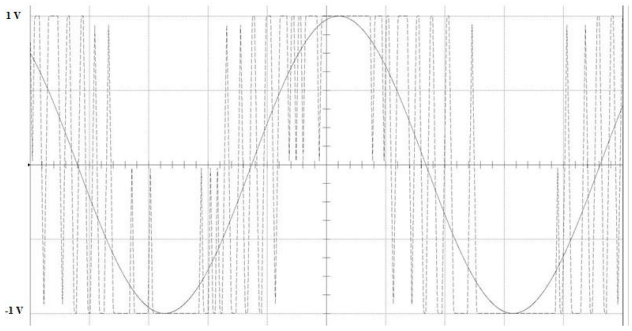

Fig. 8 Input and output of the ΣΔ modulator

In the generating process, the output bitstream of the modulator causes the quantization noise is mostly concentrated in high frequencies, this is a great advantage to this type of conversion, because high frequencies are eliminated in subsequent proceedings.

This relationship can be expressed by:

$$SNR = (6.02N + 1.76) + 10\log_{10}\left(\frac{f_s}{2f_0}\right) \quad (12)$$

To continue the design analysis of the converter will be used the Simulink software for the process of decimation using digital filters. In the decimation process is necessary to turns the signal into its Nyquist frequency and to increase the size of the word that will form the encoded signal, since until then the output of the modulator had a bitstream.

As was said before, the decimation of the project was divided into 3 smaller decimals to improve the use. Each has a decimation factor of 4, i.e. the signal frequency decreases by four times at each stage of the decimation, reaching 8 *k*Hz at the end of the process.

The number of bits of the word increases at each stage of decimation, as we have a decimation that decreases the frequency of 64 times the size of the word bits of the converter is 6 bits. For these values the signal noise of the converter ΣΔ being designed in this work will be:

$$\text{SNR} = 55.94dB \quad (13)$$

In Fig. 9 is shown the full converter. Both the analog part of the modulator, as the digital part is filtered.

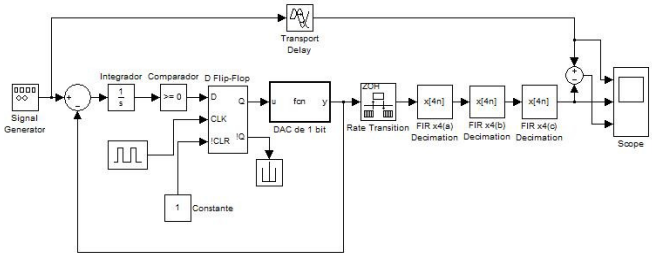

Fig. 9 Full sigma-delta converter

In modulator's output was inserted a block that keeps a constant frequency at 512 kHz for the decimation process. Was also inserted a delay entry block in order that the comparison could be made between input and output of the converter to demonstrate the quantization error. This comparison can be seen in Fig. 10. The output of decimation provides a digital signal that follows the same waveform input.

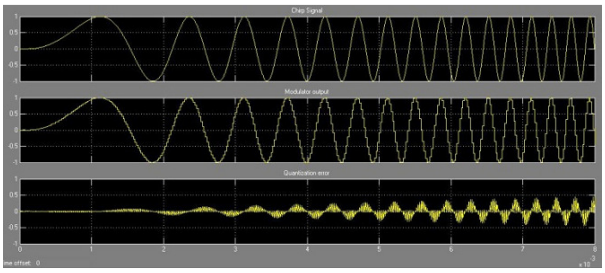

Fig. 10 Comparison between input and output

V. Application of White Noise as Output of the System

In this section, we put a source of white noise in the output of analog simulation model of the system studied.

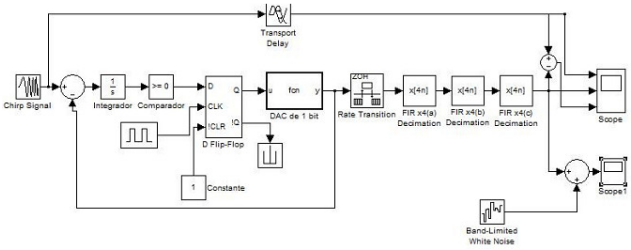

Fig. 11 Analogue simulation model with white noise source at the output of the system

White noise is a purely random signal and its spectrum has power at all frequencies. It is important to note that white noise has a stochastic characteristic. This means in practice that a white noise across the frequency band is important. The noise being white does not mean knowledge of their distribution. A white noise can have different probability distributions. Below is the waveform of the source of white noise that was entered into the system.

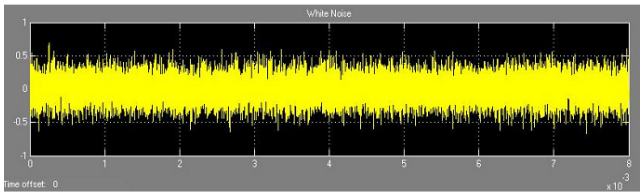

Fig. 12 Waveform of white noise applied in the output

The graph of the output with the noise source is:

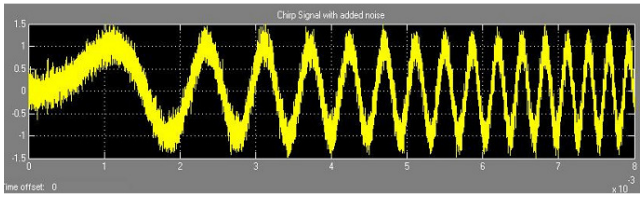

Fig. 13 Output of the system with the added noise

VI. Conclusion

Through the theories and simulations we can verify the functionality and applicability of the A/D converters of the type Sigma-Delta, emphasizing its simplicity of implementation, conversion speed of the analog signal to digital and the improvement in signal to noise ratio compared to other types of converters A/D. Although, the Sigma-Delta modulator has been introduced in 1962, only recently with the advent and advancement of VLSI technology it has gained importance. The increasing use of digital techniques also contributed to the effective use of A/D converter high accuracy.

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