Sensitivity of input blocking capacitor on Output voltage and current of a PV inverter employing IGBTs

Z.A. Jaffery, Vinay Kumar Chandna, and Sunil Kumar Chaudhary

Abstract—This paper present a MATLAB-SIMULINK model of a single phase 2.5 KVA, 240V RMS controlled PV VSI (Photovoltaic Voltage Source Inverter) inverter using IGBTs (Insulated Gate Bipolar Transistor). The behavior of output voltage, output current, and the total harmonic distortion (THD), with the variation in input dc blocking capacitor (C_{dc}), for linear and non-linear load has been analyzed. The values of C_{dc} as suggested by the other authors in their papers are not clearly defined and it poses difficulty in selecting the proper value. As the dc power stored in C_{dc}, (generally placed parallel with battery) is used as input to the VSI inverter. The simulation results shows the variation in the output voltage and current with different values of C_{dc} for linear and non-linear load connected at the output side of PV VSI inverter and suggest the selection of suitable value of C_{dc}.

Keywords—DC Blocking capacitor, IGBTs, PV VSI, THD.

I. INTRODUCTION

VOLTAGE Source Inverters (VSI) are mostly used in Photovoltaic (PV) renewable energy applications and other distributed generation (DG) systems where inverter (DC to AC converter) is the back bone of power supply [1]. It must be reliable and robust, when it is used with PV generation located in remote areas. So It is necessary to verify the output voltage and current of the inverter under different loading condition, load may be linear or non linear [2]-[3]. Under this condition the switching device (IGBTs used in this inverter) goes under tremendous voltage and current stress, thus proper protection of this device is required [4], [5] and [6]. As PV inverter converts dc(obtained from a battery charged by solar array) into ac, a dc bus voltage is maintained with the help of dc filter capacitor, which is used to protect the source (PV array in this case) from the harmonics that are coming from load side to source side because of switching action [7]-[10]. Thus it is very necessary to verify the variation of dc filter capacitor on the performance of designed PV VSI inverter under various loading conditions.

II. PROBLEM FORMATION

In this paper a 2.5KVA RMS controlled voltage source inverter as shown in Fig. 1. is simulated. The MATLAB-

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SIMULINK diagram of the inverter with a linear load connected at the output is shown in Fig. 2. The output voltage of a high-performance distributed PV system must be sinusoidal with low total harmonic distortion (THD) under both transient and periodic load disturbances. The C_{dc} tries to maintain a constant dc voltage across input of inverter. But due to high frequency switching operation involves in the inverter operation the inverter draws a non constant current from the battery. The input blocking capacitor C_{dc} is sensitive part of any PV inverter system [11], [12] and [13]. The variation in values of this capacitor effect the magnitude of output voltage and current and Total Harmonic Distortion (THD) present in them. In this paper variation of this important parameter (dc filter capacitor) is seen on load voltage and current for linear and non linear load.This works helps the design engineer/ Research students to select proper values of C_{dc}.
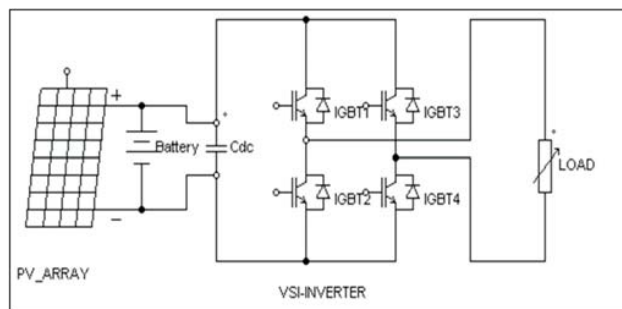

Fig. 1. PV VSI inverter schematic

III. INVERTER SIMULATION

PV voltage source inverters are described that accept dc voltage (from PV array through battery) as input and produce either single-phase or three phase sinusoidal output voltage at a low frequency relative to the switching frequency. For lighting and heating loads, voltage source square wave inverter is ideally suited as the root mean square (RMS) value of the output voltage is the only requirement that have to be controlled, but for many applications perfect sine wave is required. The higher outputs are made available to different loads with the help of suitable transformers. Voltage regulation control and sine wave generation control can easily be obtained by using Pulse Width Modulation (PWM) technique, thus PWM technique is used in this paper for simulation purpose.
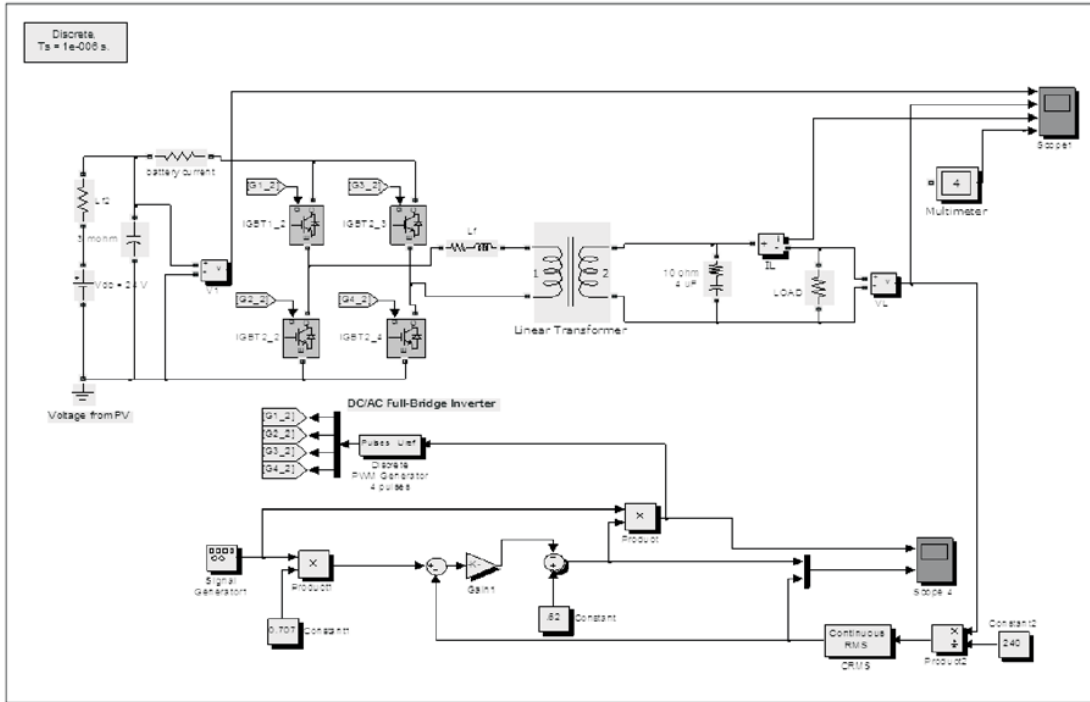
Fig. 2. MATLAB-SIMULINK model of PV Voltage Source Inverter with linear load

The linear and non-linear load taken for the simulation purpose is analogous to 2 kW heating element. Table I shows the summary of the main parameters of proposed 2500 VA inverter and load characteristics.

TABLE I
SPECIFICATION OF PROPOSED 2500VAPV-VSI

S. No.	Parameter	Value with unit
1	Rated Power	2500VA
2	Rated output frequency	Frequency at Load $= f_{\text{load}} 50\text{Hz}$
3	Rated output voltage	$\text{Vo}_{\text{load}} = 240\text{V}$
4	Battery voltage	$V_{\text{dc}} = 24\text{V}$
5	Battery and lead wire resistance	$R_{\text{batt}} - 30\text{ m}\Omega$
6	Inverter switching frequency	$f_{\text{sw}} = 12$ kHz
7	DC filter capacitor C_{dc}	$4700\mu\text{F}$
8	Linear load	$R = 32.2\Omega$
9	Non linear load	Diode Rectifier with RL Load ($R = 40\Omega$, $L = 4\text{mH}$)

A suitably designed and controlled switching power converter supplies the rated voltage, current and frequency in specific range needed for load. In order to design control strategies of a switching converter, it is necessary to know the static and dynamic behavior of system, under linear and non-linear loading patterns [10]-[13]. From the PWM modulation, the analysis of harmonic components in the proposed inverter can be preformed. The output voltage produced by comparison of the two reference signals and the carrier signal can be expressed as

$$V_0 = (\theta) = A_0 + \sum_{n=1}^{\infty}(A_n \cos n\theta + B_n \sin n\theta) \quad (1)$$

If there are P pulses per quarter period, and it is an odd number, then the coefficients B_n and A_0 would be zero, where n is an even number. Therefore, Eq. (1) can be rewritten as

$$V_0(\theta) = \sum_{n=1,3,...}^{\infty} A_n \cos \theta \quad (2)$$

$$A_n = -\frac{2V_{\text{dc}}}{n\pi} \sum_{m=0}^{P} \sum_{i=1} 4[(-1)^{\text{int}(i/2)} \sin(n\alpha_{m+i})], \quad (3)$$

where m is a pulse number. The Fourier series coefficients of the conventional single-phase full-bridge inverter by sinusoidal PWM are given as

$$A_n = \frac{4V_{\text{dc}}}{n\pi} \sum_{m=1}^{P} [(-1)^m \sin(n\alpha_m)]. \quad (4)$$

Where as % THD present in output voltage and current could be determined by the formula given below

$$\text{THDin}(\%) = \frac{\sqrt{V_{n^2} + V_{n+1^2} V_{n+2^2}}}{V_1} \times 100 \quad (5)$$

Most of the voltage source inverter uses load voltage RMS (Root Mean Square) controller in order to regulate the amount of output voltage at load side. RMS controllers provide a cost effective, ease of implementation, solution to the voltage source inverter. A commonly used RMS voltage controller for a full-bridge inverter using MATLAB SIMULINK is shown in Fig. 2. The reference input voltage (Vref) to PWM generator block is obtained by comparing the normalized load voltage

TABLE II
OUTPUT VOLTAGE AND %THD FOR LINEAR LOAD

S.No	Blocking Capacitor (μF) C_{dc} LINEAR LOAD	O/p Voltage in Volts	% THD in O/P Voltage
1	1	222.9	4.15
2	10	223.3	4.16
3	100	227.2	4.13
4	500	235.7	3.99
5	1,000	237.1	3.96
6	5,000	237.6	3.98
7	10,000	237.8	3.98
8	20,000	238.3	3.90
9	30,000	239.0	3.76
10	40,000	239.6	3.50
11	47,000	240.1	3.38
12	50,000	240.2	3.33
13	80,000	241.6	2.95

TABLE III
OUTPUT CURRENT AND %THD FOR LINEAR LOAD

S.No	Blocking Capacitor (μF) C_{dc} LINEAR LOAD	O/p Current in A	% THD in O/P Current
1	1	6.924	4.15
2	10	6.936	4.16
3	100	7.057	4.13
4	500	7.32	3.99
5	1,000	7.363	3.96
6	5,000	7.38	3.98
7	10,000	7.384	3.98
8	20,000	7.401	3.90
9	30,000	7.422	3.76
10	40,000	7.422	3.76
11	47,000	7.455	3.38
12	50,000	7.461	3.33
13	80,000	7.504	2.95

by an ideal and normalized value of load RMS voltage. After comparison the error signal was fed to error gain block in order to adjust value of gain according to the variation in depth of modulation due to sudden change in load. This signal is than compared with a standard modulation index (0.62) in order to get the reference signal for PWM generator (V_{PWM}). The PWM generator than generates PWM pulses and send it to full bridge inverter block in multiplexed form for the switches present in the inverter.

IV. SIMULATED RESULT AND CONCLUSION FOR THE EFFECT OF FILTER CAPACITOR C_{DC} VARIATION ON OUTPUT VOLTAGE AND % THD WITH LINEAR LOAD

The MATLAB simulation model of RMS controlled PV VSI as shown in Fig. 2. has dc filter capacitor (C_{dc}) at the dc side of the inverter, is used to maintain the dc bus voltage. It is necessary to know the variation of this capacitor on the performance of the inverter. Table II shows the different values of the C_{dc} and the corresponding values of the output voltage and percentage of total harmonic distortion (THD) for linear load and Fig. 3. shows the graphical representation of the same.
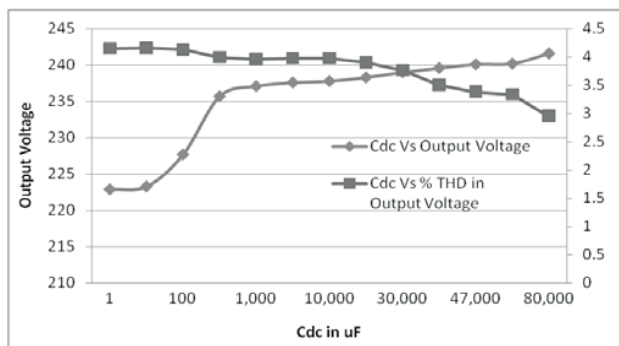

Fig. 3. Output voltage and THD variation with respect to C_{dc}

From the graph as shown in Fig. 3., the lower values of C_{dc} allows more distortion to interact with the input, thus THD is high and dip in the output AC voltage. The higher values of C_{dc} provides low impedance path to the distortions that are coming from the switching of inverter, thus maintains the DC voltage. Hence one should select the higher value of C_{dc} for better performance of inverter to maintain DC voltage under linear load. Under this condition the snubber resistor R_s and snubber capacitor C_s are kept constant at 1e5? ohm and 130nF respectively.
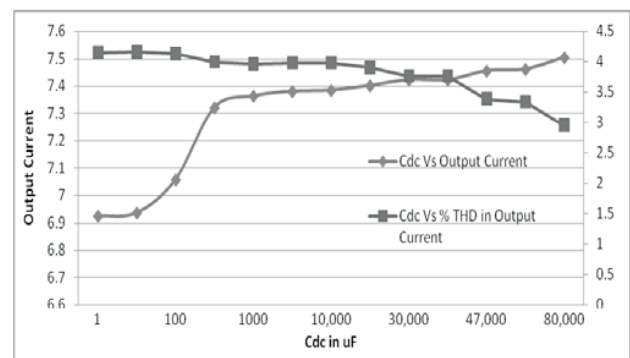

Fig. 4. Output current and THD variation with respect to C_{dc}

It was observed from Fig. 5.that for a value of $47,000\mu$F of input dc capacitor, the output voltage and current magnitude was 240V and 7.455 A, nearly equal to the rated value of designed inverter. From table II and III the THD recorded in voltage and current at this value of input capacitor was 3.38%.Fig.5. shows the variation in battery current, Voltage across C_{dc}, Load current and Load voltage of PV-VSI with linear load having C_{dc} value $47,000\mu$F.
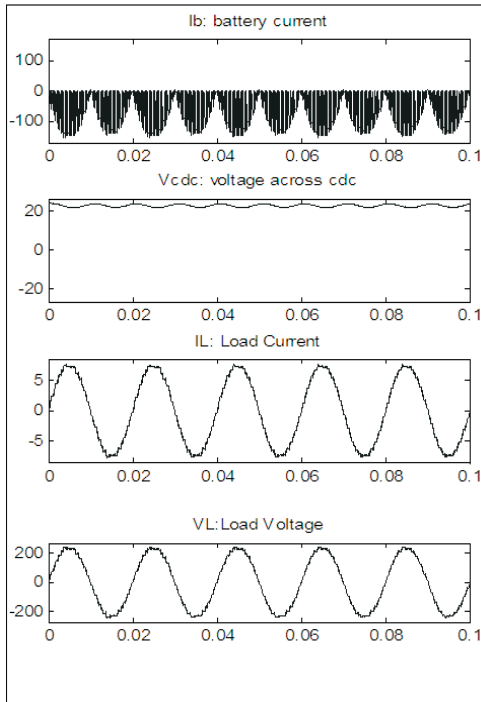
Fig. 5.   Battery current, Voltage across C_{dc}, Load current and Load voltage of PV-VSI with linear load

TABLE IV
OUTPUT VOLTAGE AND %THD FOR NON LINEAR LOAD

S.No	Blocking Capacitor (μF) C_{dc} LINEAR LOAD	O/p Voltage in Volts	% THD in O/P Voltage
1	1	230	4.04
2	10	230.4	4.05
3	100	233.9	4.05
4	500	240.9	3.88
5	1,000	242.0	3.86
6	5,000	242.4	3.89
7	10,000	242.6	3.89
8	20,000	243.0	3.83
9	30,000	243.6	3.72
10	40,000	244.2	3.60
11	47,000	244.6	3.52
12	50,000	244.8	3.49
13	80,000	245.9	3.23

V. SIMULATED RESULT AND CONCLUSION FOR THE EFFECT OF FILTER CAPACITOR CDC VARIATION ON OUTPUT VOLTAGE AND % THD WITH NON LINEAR LOAD

Table IV shows the output voltage and % THD variation for the change in C_{dc}, with non-linear load and Fig. 6. shows the graphical representation, that shows the increase in the output voltage and % THD after a certain value of C_{dc}, even if RMS controller is used to maintain the output. Table V shows the output current and % THD variation for the change in C_{dc}, with linear load and Fig. 7. shows the graphical representation. The simulation shows, with the increase in the value of dc
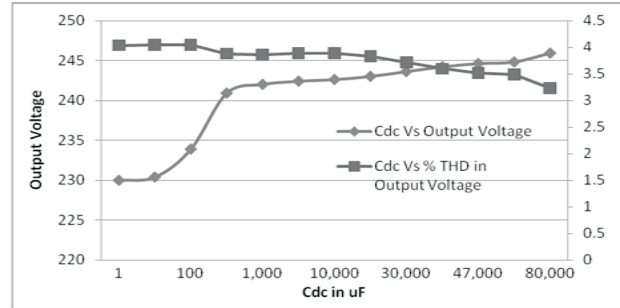

Fig. 6.   Output voltage and THD variation with respect to C_{dc} with non linear load

TABLE V
OUTPUT CURRENT AND %THD FOR NON LINEAR LOAD

S.No	Blocking Capacitor (μF) C_{dc} LINEAR LOAD	O/p Current in Volts	% THD in O/P Current
1	1	5.688	3.10
2	10	5.697	3.11
3	100	5.783	3.13
4	500	5.959	2.95
5	1,000	5.987	2.93
6	5,000	5.998	2.94
7	10,000	6.001	2.94
8	20,000	6.013	2.86
9	30,000	6.028	2.74
10	40,000	6.043	2.61
11	47,000	6.053	2.52
12	50,000	6.057	2.48
13	80,000	6.086	2.19

filter capacitor (C_{dc}) the output current and percentage THD stabilizes in a favorable range.

Table V shows the output current and % THD variation for the change in C_{dc}, with non-linear load and Fig. 7. shows the graphical representation and found that there is a non-linearity and higher % THD up to C_{dc} of 100 μf and also the effect is more for higher values C_{dc}. Though the output current is stabilizing but the % THD is further increasing because of nature of load. Thus, careful selection of the filter capacitor is necessary. It was observed from Fig. 8.with a value of
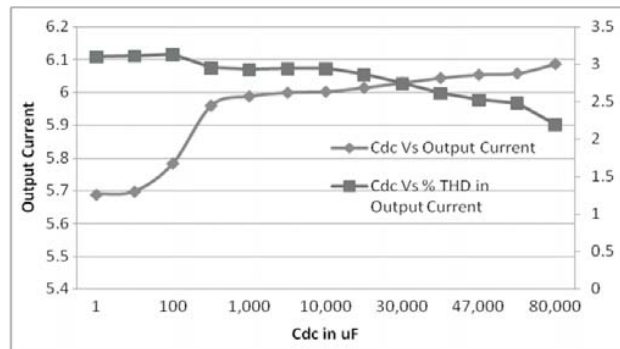

Fig. 7.   Output Current and THD variation with respect to C_{dc}

47,000uF of input dc capacitor, the output voltage and current magnitude was 244.6V and 6.053 A, higher than the rated value of designed inverter. From table IV and V the THD recorded in voltage and current at this value of input capacitor was 3.52%and 2.52% respectively.
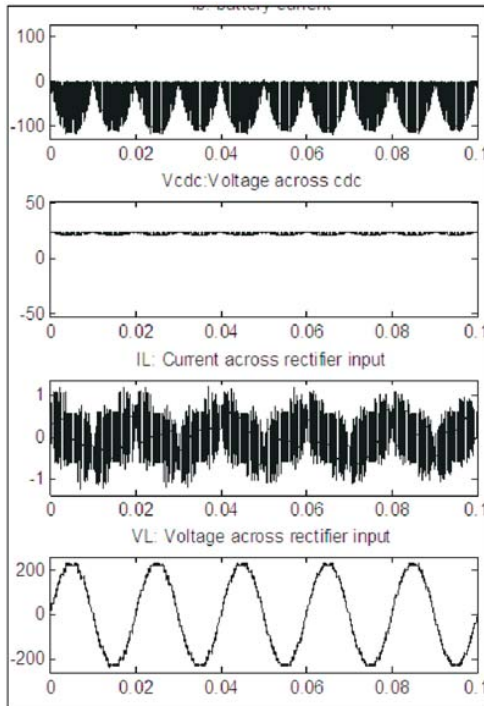

Fig. 8.   Battery current, Voltage across C_{dc}, Load current and Load voltage of PV-VSI with non linear load

VI. CONCLUSION

The simulation of RMS controlled PVVSI is done for various values of the filter DC capacitor (C_{dc}) for linear and non-linear load. Tables and figures show the variation in the output voltage, current and their respective percentage total harmonic distortions. The simulation results will be helpful for the practicing engineers and the students for particular selection of filter capacitor and also for the sensitivity of these parameter variations on the performance of the Photovoltaic Voltage Source inverter.

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