International Journal of Information, Control and Computer Sciences
ISSN: 2517-9942
Vol:8, No:2, 2014

Schmitt Trigger Based SRAM Using Finfet Technology- Shorted Gate Mode

Vasundara Patel K. S., Harsha N. Bhushan, Kiran G. Gadag, Nischal Prasad B. N., Mohmmed Haroon

***Abstract*—**The most widely used semiconductor memory types are the Dynamic Random Access Memory (DRAM) and Static Random Access memory (SRAM). Competition among memory manufacturers drives the need to decrease power consumption and reduce the probability of read failure. A technology that is relatively new and has not been explored is the FinFET technology. In this paper, a single cell Schmitt Trigger Based Static RAM using FinFET technology is proposed and analyzed. The accuracy of the result is validated by means of HSPICE simulations with 32nm FinFET technology and the results are then compared with 6T SRAM using the same technology.

***Keywords*—**Schmitt trigger based SRAM, FinFET, and Static Noise Margin.

I. Introduction

THE conventional 6 transistor SRAMs using bulk CMOS technology will have high leakage current, high power consumption and a high probability of read failure. Below the channel length of 100nm the 6 transistor SRAM cell is found to be unstable. FinFET is known to reduce the leakage currents and hence the high leakage current problem is overcome using FinFET technology. In the Schmitt trigger based SRAM [1] using FinFET technology, we use the modified Schmitt trigger circuit as a drop in replacement to the inverter in a 6 transistor SRAM cell. The modified Schmitt trigger adaptively changes the threshold of the circuit to reduce the probability of read failure at lower supply voltages.

A. SRAM (Static Random Access Memory)

The read/write (R/W) memory circuits are designed to permit the modification (writing) in the memory cell, as well as their retrieval (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely (as long as sufficient power voltage is provided), without any need for a periodic refresh operation. The data storage cell or the 1-bit memory cell in static RAM invariably consists of a simple latch circuit with stable operating points (states).

SRAM cell basically has 3 modes of operation, 1.Hold mode, 2.Write mode, 3.Read mode. In the hold mode the data is stored in the cell and in the write mode the data is written onto the cell from the bit lines and in the read mode the data is read on the bit lines.

Vasundara Patel K S is with Department of Electronics and communications, BMS College of Engineering, Bangalore, Karnataka, India (phone: 080-26622130-135; fax: 080-26614357; e-mail: vasu.ece@ bmsce.ac.in).

Harsha N Bhushan, Kiran G Gadag, Nischal Prasad B N, Mohmmed Haroon, Nano technology Project Team student members, BMS College of Engg, Bangalore, Karnataka, India(phone: 080-26622130-135; fax:080-26614357).

B. FinFET

Device scaling has increased short Channel effects (SCE) [2], [3]. To overcome SCE, different transistor structures have been investigated to replace the bulk MOSFETs [4]-[8]. Among them, FinFETs are considered to be a promising candidate for scaled CMOS devices in sub-22-nm technology nodes. FinFETs have emerged as promising alternatives to bulk MOSFETs for scaled technologies because of lower short channel effects (SCE). Furthermore, threshold voltage (V_{th}) can be easily controlled by engineering the metal gate work function. Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS at the Nano scale. FinFETs are usually double-gate devices but can also be multi gate. The two gates of a FinFET can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. This gives rise to a rich design space. FinFETs have been proposed as a promising alternative for addressing the challenges posed by continued scaling i.e. instability and high leakage current. Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing. Fig. 1 shows the structure of a multi-fin FinFET [9]. The FinFET device consists of a thin silicon body, the thickness of which is denoted by TSi, wrapped by gate electrodes. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer [9]. Due to this reason, the device is termed quasi-planar. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel. The effective gate width of a FinFET is 2nh, where n is the number of fins and h is the fin height. Thus, wider transistors with higher on-currents are obtained by using multiple fins. The fin pitch (p) is the minimum pitch between adjacent fins allowed by lithography at a particular technology node. Using spacer lithography, p can be made as small as half of the lithography pitch.

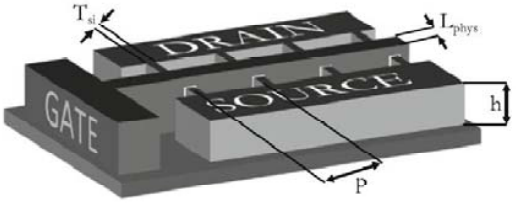

Fig. 1 General multi-gate structure

There are three modes of operation

1. Shorted gate mode (SG): Two gates tied together. (Represented by Fig.2a)
2. Independent gate mode (IG): Independent signals drive the gate. (Represented by Fig.2b)
3. Low power mode (LP): One gate is tied to reverse bias to reduce leakage.

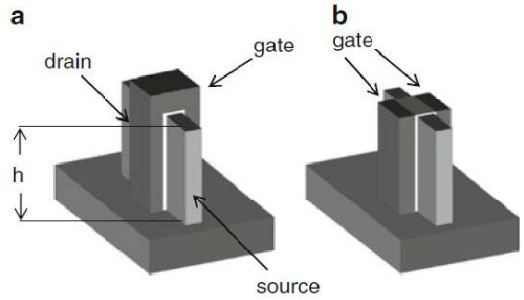

Fig. 2 (a) Shorted gate structure, (b) Independent gate structure

C. Schmitt Trigger

A Schmitt trigger is a high-performance circuit used to shape input pulses and reduce noise. It responds to a slow-changing input pulse with a fast-changing output transition. The voltage-transfer characteristics of the circuit show different switching thresholds for positive and negative going input slopes. Schmitt triggers are bitable networks that are widely used to enhance the immunity of a circuit to noise and disturbances. It is good as a noise rejecter. Schmitt trigger make use of waves, therefore it is widely used for converting analog signals into digital ones and to reshape sloppy, or distorted rectangular pulses. Hysteresis of the trigger eliminates noise making a cleaner and more reliable signal. The output of a Schmitt trigger changes state when a positive going input passes the upper trigger point (UTP) voltage and when negative going input passes the lower trigger point voltage. The circuit diagram of the modified Schmitt trigger [10] is as shown in the Fig.3. This is the modified circuit that is used as a drop in replacement to the inverter in a conventional 6 transistor SRAM.

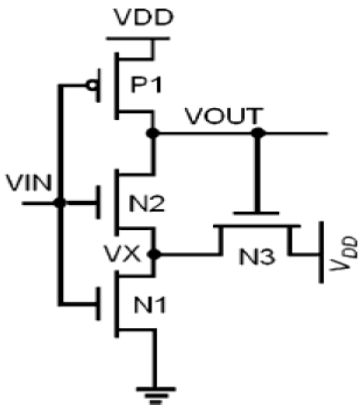

Fig. 3 Modified Schmitt trigger

II. Analysis of Schmitt Trigger Based SRAM Cell Using FinFETs

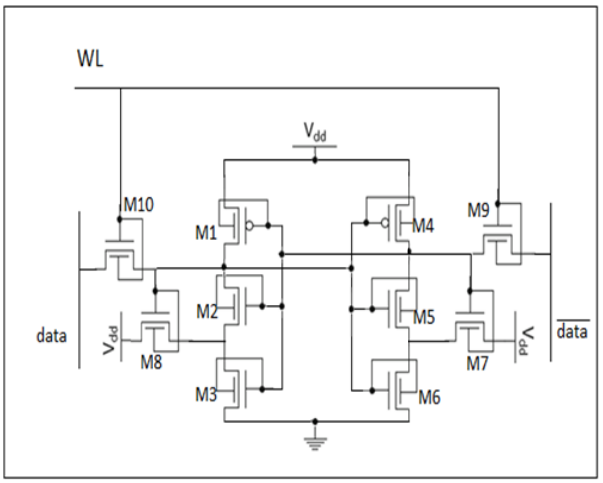

Fig. 4 Schmitt Trigger based SRAM cell

The complete schematic for the ST based SRAM bit cell is as shown in Fig. 4. Transistors M1-M2-M3-M8 forms one ST inverter while M4-M5-M6-M7 forms another ST inverter. M10 and M9 are the access transistors. The positive feedback from M7/M8 adaptively changes the switching threshold of the inverter depending on the direction In order to avoid a read failure; the feedback mechanism should increase the switching threshold of the inverter M4-M5-M6. Transistors M7 and M6 raise the voltage at node V7 and increase the switching threshold of the inverter storing “1”. Thus, Schmitt trigger action is used to preserve the logic “1” state of the memory cell [11]. The proposed ST based SRAM bit cell utilizes differential operation, giving better noise immunity [12]. It requires no architectural change compared to the conventional 6T cell architecture and hence can be used as a drop-in replacement for the present 6T based designs [13].

III. Simulation Results of Schmitt Trigger Based SRAM Cell

HSPICE simulations are done using 32nm FinFET technology. The 6T and the ST based bit cells are compared for various SRAM metrics. The width of the pass transistors were chosen in the ratio 3:1 [14], [15]. The widths of all the transistors were chosen to obtain optimum curves with least distortions in read-write and hold modes for the Hspice simulations. To do the read failure analysis, a ramp voltage is provided at one of the data or data lines and the output is measured at the other and vice versa. On superimposing both the curves, butterfly curve as shown in graph of Fig. 5 is obtained.

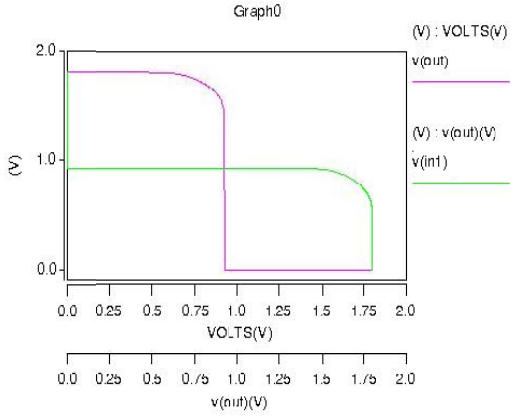

Fig. 5 Butterfly curve (HOLD mode)

TABLE I
SNM OF 6 TRANSISTOR AND SCHMITT TRIGGER SRAM CELL

VDD (V)	SNM 6T SRAM (V)	SNM ST SRAM (V)
1.8	0.175	0.25
1.6	0.1	0.2
1.4	0.1	0.2
1.2	0.06	0.15
1.0	0.05	0.1
0.8	0.04	0.08
0.6	0.03	0.04
0.5	0.0015	0.03
0.4	0.0012	0.025
0.3	READFAILURE	0.012
0.2	READFAILURE	0.012

Static Noise Margin (SNM) [12], [16] is the side of the largest square that fits in the butterfly. By reducing V_{dd} in steps, SNM can be tabulated. When the two curves flip as shown in Fig. 6, read failure is said to have occurred.

The SNM was tabulated for both ST-SRAM and 6transistors RAM as indicated by Table I and it was found that read stability of the ST SRAM is improved as compared to 6T SRAM.

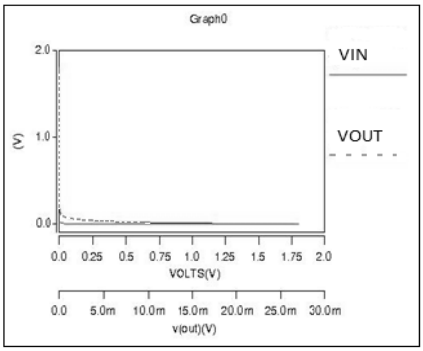

Fig. 6 Read failure occurs since the curves flip

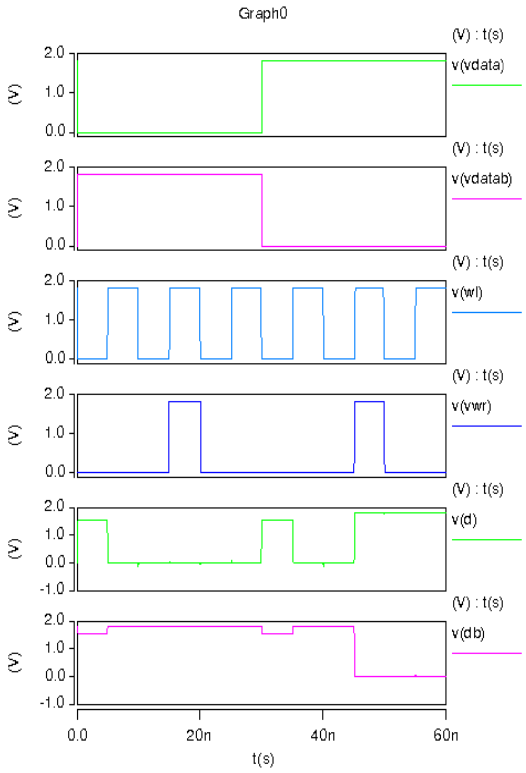

Fig. 7 Read Write analysis of 6T SRAM using FinFET.

The power consumption of the SRAM cells are observed on Synopsis Hspice simulation tools and the Table II shows the comparison between the conventional 6T SRAM cell and ST-SRAM which indicates a greater reduction in power consumption. Fig.7 shows Read Write analysis of 6T SRAM using FinFET.

The layout for the ST-SRAM cell and the conventional 6T SRAM was constructed and the access times for both the cells were measured using simulations. As indicated by the Table II, the access time also reduced for the Schmitt trigger based SRAM using FinFET technology.

TABLE II
ACCESS TIME OF 6 TRANSISTOR AND SCHMITT TRIGGER SRAM CELL.

Types	Read time	Write time
6 T SRAM	32ps	23ps
Schmitt Trigger SRAM	7ps	6ps

VI. CONCLUSION

Schmitt trigger based SRAM cell using FinFET shorted gate mode is designed and analyzed. It is shown that the access time is improved and the read failure probability is also reduced as compared to 6 Transistor SRAM cell. 32nm FinFET PTM technology file is used for this analysis. Thus Schmitt trigger based SRAM cell is better than 6 Transistor SRAM cell.

ACKNOWLEDGMENT

Authors thank BMS College of Engg for supporting the work through TEQIP phase II grants

REFERENCES

[1] UjwalShirode, Ajay Gadhe, "Read stability and read failure analysis of low voltage Schmitt Trigger based SRAM bit cell", International Journal of Engineering Research and Applications (IJERA) Vol.3, Issue 1, January-February 2013W.-K. Chen, *Linear Networks and Systems* (Book style). Belmont, CA: Wadsworth, 1993, pp. 123–135.

[2] "International Technology Road map for Semiconductors", 2006.

[3] K. Bernstein, D. J. Frank, A. E. Gattiker, W. Haensch, B.L. Ji, S. R. Nassif, E. J. Nowak, D. J. Pearson, and N. J.Rohrer, "High-performance CMOS variability in the 65-nm regime and beyond", IBM J.Res. Dev., vol. 50, no. 4/5, pp. 433–449, Jul./Sep. 2006.

[4] N. Collaert, N. A. De Keersgieter, A. Dixit, I. erain, L.-S. Lai, D. Lenoble, A. Mercha, A. Nackaerts, B.J. Pawlak, R. Rooyackers, T. Schulz, K.T. Sar, N.J. Son, M.J.H. Van Dal, P. Verheyen, K von Arnim, L. Witters, M. De, S.Biesemans, M. Jurczak, "Multi-gate devices for the 32nm technology node and beyond", Solid State Device Research Conference, 2007. ESSDERC 2007. 37th European,vol.,no., pp.143-146, 11-13 Sept. 2007

[5] K. Noda, T. Uchida, T. Tatsumi, T. Aoyama, K.Nakajima, H. Miyamoto, T. Hashimoto, and I. Sasake, "0.1pm delta-doped MOSFET using post-energy implanting selective epitaxy", in 1994- VLSI Symp. VLSI Technology Dig. Tech. Papers, pp. 19-20.R. Yan, A. Ourmazd, and K. Lee, "Scaling the Si MOSFET: From bulk to SO1 to bulk", IEEE Trans. Electron Devices, vol. 39, pp. 1704-1710, July 1992.

[6] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P.KO, and C. Hu, "A dynamic-threshold MOSFET for ultra-low voltage operation",Znt. Electron Devices Meet. Tech. Dig., 1994, pp. 809-812.

[7] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K.Asano, C. Kuo, T.-J.King, J. Bokor, and C. Hu, "A folded channel MOSFET for deep-sub-tenth micron era", in IED MTech. Dig., 1998, pp. 1032–1034.

[8] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K.Asano, C. Kuo, T.-J.King, J. Bokor, and C. Hu, "A folded channel MOSFET for deep-sub-tenth micron era," in IED MTech. Dig., 1998, pp. 1032–1034.

[9] Prateek Mishra, AnishMuttreja, and Niraj K. Jha"FinFET Circuit Design", Nano Electronics circuit design, 2011, Springer, pp. 23-54

[10] Munish Kumar, ParminderKaur, SheenuThapar, "Design of CMOS Schmitt Trigger", International Journal of Engineering and Innovative Technology (IJEIT) Volume 2, Issue 1, July 2012.

[11] Jaydeep P. Kulkarn, Keejong Kim, and Kaushik Roy, "A 160 mV Robust Schmitt Trigger Based Sub threshold SRAM" IEEE Journal Of Solid-State Circuits, Vol. 42, No. 10, October 2007.

[12] E. Seevinck, F. List, and J. Lohstroh, "Static noise margin analysis of MOS SRAM cells", IEEE Solid-State Circuits, vol. SC-22, no. 5, Oct. 1987, 748–754.

[13] BOOK title, "CMOS digital integrated circuits: analysis and design", Authored Sung-Mo Kang, Yusuf Leblebici.

[14] BOOK title, "CMOS circuit design, layout and simulation", Volume 1, Authored R. Jacob Baker.

[15] Pilo, H., Barwin, C., Braceras, G., Browning, C., Lamphier, S., Towler, F. "An SRAM Design in 65-nm Technology Node Featuring Read and Write-Assist Circuits to Expand Operating Voltage", IEEE Journal of Solid-State Circuits. 42. 4. 813 - 819 (Apr. 2007).

[16] F. J. List, "TheStatic Noise Margin of SRAM cells," in Dig. Tech. Papers, ESSCIRC (Delft, The Netherlands), Sept. 1986, pp. 16–18.

Dr. Vasundara Patel K S was born in Gowthamapara near Jog Falls, Shimoga District, Karnataka, India on July 29, 1965.She received the B.E degree in Electronics and Communication Engineering from the University of Mysore, India, in 1989. Master of Technology in Electronics engineering from BMS College of Engg.,affiliated to Vishveswaraya Technological University, Belgaum, India in 2003.

From 1989 to 1993, she served in Electronics and Telecommunication industries Pvt Ltd, Bangalore, Manufacturers of Test and Measuring instruments, as Production and Testing Engineer and also involved in research activity. She is serving BMS College of Engg. since 1999, received Ph.D Degree for her Thesis, "Design of Multi-Valued Logic Circuits/Digital Building Blocks" during 2012. She has published over 30 national, international conferences and Journal Papers. She has presented many research papers in India and abroad.

Her areas of interest are Operations research, Analog Electronic Circuits, VLSI circuits and systems; Advances in VLSI, Low power VLSI, Analog and Mixed Signal VLSI.

She is a life member of technological organizations like ISTE, IACSIT, IMAPS.

Other authors are students of BMS College of Engg.