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Robust & Energy Efficient Universal Gates for High Performance Computer Networks at 22nm Process Technology

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***Abstract*—**Digital systems are said to be constructed using basic logic gates. These gates are the NOR, NAND, AND, OR, EXOR & EXNOR gates. This paper presents a robust three transistors (3T) based NAND and NOR gates with precise output logic levels, yet maintaining equivalent performance than the existing logic structures. This new set of 3T logic gates are based on CMOS inverter and Pass Transistor Logic (PTL). The new universal logic gates are characterized by better speed and lower power dissipation which can be straightforwardly fabricated as memory ICs for high performance computer networks. The simulation tests were performed using standard BPTM 22nm process technology using SYNOPSYS HSPICE. The 3T NAND gate is evaluated using C17 benchmark circuit and 3T NOR is gate evaluated using a D-Latch. According to HSPICE simulation in 22 nm CMOS BPTM process technology under given conditions and at room temperature, the proposed 3T gates shows an improvement of 88% less power consumption on an average over conventional CMOS logic gates. The devices designed with 3T gates will make longer battery life by ensuring extremely low power consumption.

***Keywords*—**Low power, CMOS, pass-transistor, flash memory, logic gates.

I. Introduction

THE growing demand for portable devices is driving chip designers to rely on scaling down of device sizes with increased computation performance and longer battery life. The increasing chip density and complexity has led to more power dissipation.

This directly affects the battery operated portable devices and requires expensive cooling and packaging technologies. In a modern day high performance microprocessor, around 45% of the total power is consumed by the data path and memory units [1]. NAND and NOR logic gates plays an important role in building up of most of the data path units and memory. Therefore, a careful design and analysis is required for NAND and NOR gates to obtain optimum performance [2].

Logic gates carry out basic logical functions and are the primary building blocks of digital integrated circuits. They are formed by the amalgamation of transistors to realize digital operations. Every digital manufactured product, like computers, calculators, mobile, even digital watches, are made up of logic gates. For example, an adder circuit can be formed by the combination of many gate like by using NOR/NAND gates only or by using AND, OR gates and so on. The adder which is of great significance in computer networks and also for many more applications is fundamentally constructed from the logic gates.

With a focus to realize high speed and ultra low power data networks, circuits should be built with low power dissipating gates. To support the ever-changing needs of current and emerging applications, the authors have developed the most appropriate universal gates with reduced transistor count. Simulation results of proposed 3T based logic gates (NAND and NOR) utilizing standard 22nm CMOS BPTM technology illustrate a significant improvement with respect to number of transistors, propagation delay and power dissipation. The proposed new design of 3T based logic gates is based on modified CMOS inverter and pass-transistor logic (PTL). This research paper is organized as follows: In Section II, review of pass transistor and CMOS inverter logic, proposed logic gates in section III, which is followed by the simulation results using HSPICE and conclusion in Sections IV and V, respectively.

II. Review of Pass transistor and CMOS Inverter Logic

A popular and widely used alternative to complementary CMOS is pass-transistor logic (PTL). PTL attempts to decrease the quantity of transistors necessary to realize the logic by allowing the principal inputs to drive gate terminals as well as drain/source terminals as shown in Fig. 1. It is observed from Fig. 1 [3]-[5]. When the device is getting used as a pass-transistor may conduct current in either direction. The N- channel MOSFET passes a well-built logic 0 but a frail weak logic 1(threshold voltage drop V_{th}, logic high =VDD - V_{thn}) and P- channel MOSFET passes a strong logic 1 but a weak logic 0(threshold voltage drop V_{th}, logic low = V_{thp}). Thus, we can say that NMOS switches are best suitable for pull-down network and the PMOS switches are suitable for pull-up network. Keeping these in view, the study adopted a quasi-experimental research method [6], [7].

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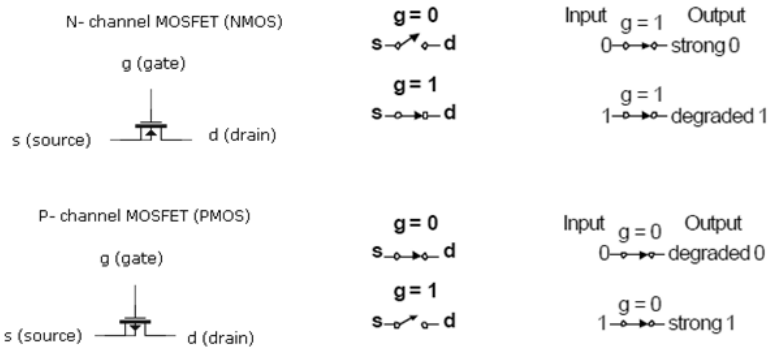

Fig. 1 Pass Transistor Logic (PTL)

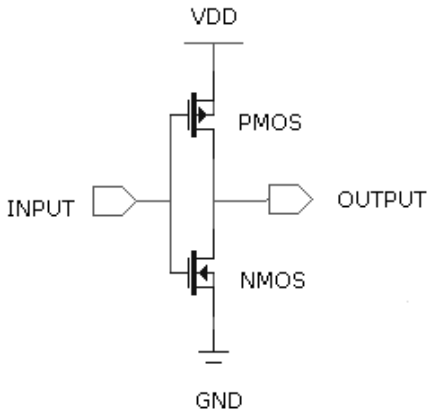

Fig. 2 CMOS Inverter

CMOS inverters are some of the most broadly used and adaptable MOSFET inverters in chip designing. They operate with less power loss and at relatively better speed. The CMOS inverter; furthermore, has very good logic buffer characteristics, in that, its noise margins are large in both low and high states. A CMOS inverter shown in Fig. 2 contains a NMOS and a PMOS transistor connected at the drain and gate terminals, a ground connected at the NMOS 's' source terminal and a supply voltage VDD at the PMOS 's' source terminal were INPUT is connected to the 'g' gate terminals and OUTPUT is connected to the 'd' drain terminals. As the input of the CMOS device varies between logic 1 and logic 0, the state of the PMOS and NMOS varies accordingly to make output as logic 0 and logic 1 respectively.

III. Three Transistor (3T) Based Logic Gates

The 3T OR and AND gates design is based on PMOS and NMOS pass transistor logic (PTL). The 3T NAND and NOR gates design is based on CMOS inverter and PTL. Output voltage degradation occurs across the PMOS and NMOS pass transistors due to V_{th} threshold voltage drop while passing the logic zero or logic one respectively in relation to the input signal. The output voltage degradation caused by threshold drop could be considerably minimized by escalating the W/L aspect ratio of the pass transistor. Equation (1) relates the threshold voltage V_{th} of a MOSFET device to its channel width W and length L.

$$V_t = V_{t0} + g\left(\sqrt{V_{SB} + \phi_0}\right) - \alpha 1 \frac{t_{ox}}{L}(V_{SB} + \phi_0)(\alpha v \frac{t_{ox}}{L} V_{ds}) + \alpha w \frac{t_{ox}}{W}(V_{SB} + \phi_0) \quad (1)$$

where t_{OX} is the oxide layer thickness, V_{t0} is the zero bias threshold voltage, g is bulk threshold coefficient, ϕ_0 is $2\phi_F$, where ϕ_F is the Fermi potential, and $\alpha_{1,}\alpha_v$ & α_w are process dependent parameters. From (1) it is understandable that by rising the width W of a MOSFET, maintaining the length L fixed it is possible to reduce the voltage degradation at output caused by threshold voltage.

A. NOR gate

The new NOR gate design using only three transistors (3T) is revealed in Fig. 3 (a). The design is based on PMOS pass-transistor logic and modified CMOS inverter. The 3T NOR functionality can be explained as follows. The PMOS M1 and NMOS M2 on the left form a modified CMOS inverter structure. The NMOS M3 on the right acts as a pass transistor (PTL). When A=0, M3 is OFF and the modified inverter present on the left (M1 & M2) functions as an ordinary CMOS inverter. Therefore, complement of input B is obtained as the output. When A=1 & B=0 , M2 is OFF, M1 and M3 are ON which leads to an undefined output state 'X', because M1

tends to pull up the output node while M3 tends to pull down the output node. Similarly when A=1 & B=1, M1 is OFF, M2 and M3 are ON leading to an undefined output state 'X', because M2 tends to pull up the output node while M3 tends to pull down the output node. For A=1 & B=0 or 1, a strong logic '0' output is required. It is possible to obtain exact output logic levels with the proposed circuit, if the channel width of M3 is made 6 times that of M2 or 3 times that of M1 similar to NAND gate. Thus M3 becomes much stronger than M1 and M2, giving a strong logic '0' at output when input A=1. For NAND and NOR gate at 0.022µm (22nm) process, the length of the channel for all transistors was taken as L=0.022µm, channel width of M1,W_{M1} = 0.200µm, channel width of M2, W_{M2} = 0.100 µm, and channel width of M3, W_{M3} = 0.600 µm. OR gate operation could be obtained with an additional CMOS inverter at the NOR output with 5 transistors only. Table I gives the state table for 3T NOR gate for better understanding. Fig. 4 gives the input- output waveform for 3T NOR gate.

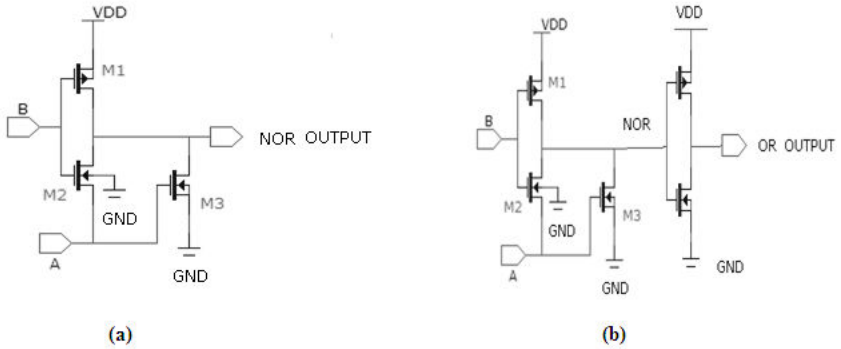

Fig. 3 (a) 3Tbased NOR gate (b) 5T based OR gate

TABLE I
STATE TABLE OF 3T NOR GATE

Inputs		Transistor State			NOR Output
		CMOS Inverter		NMOS Pass Transistor	
A	B	M1	M2	M3	
0	0	On	Off	Off	1/ VDD
0	1	Off	On	Off	0/A
1	0	On	Off	On	0/ Gnd
1	1	Off	On	On	0/ Gnd

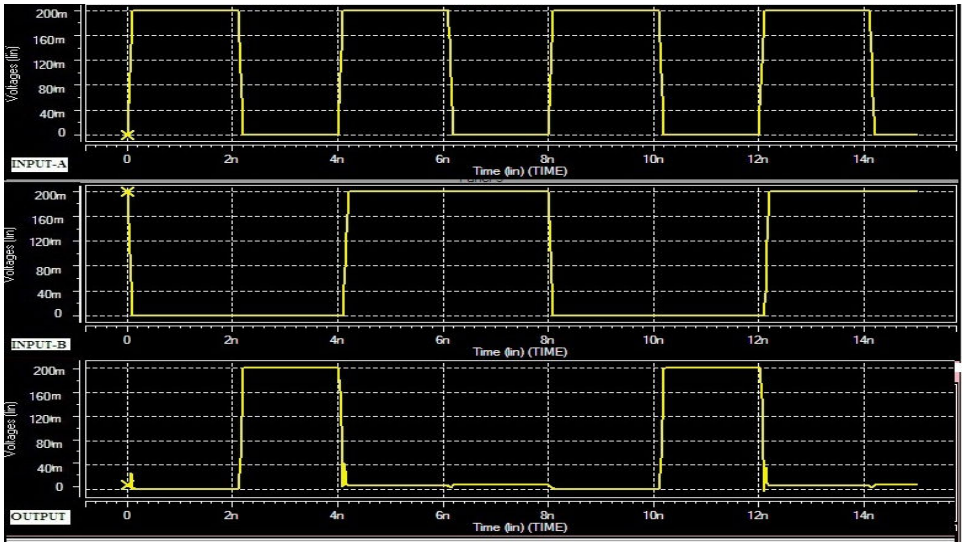

Fig. 4 Input/output waveform of 3T NOR gate @ 22nm withVDD=200 mV

B. NAND gate

The proposed new design of 3T NAND gate using three transistors is shown in Fig. 5. The design is based on PMOS pass-transistor logic and modified CMOS inverter. The PMOS M1 and NMOS M2 on the left form a modified CMOS inverter structure. The PMOS M3 on the right acts as a pass transistor. When A=1, M3 is OFF and the modified inverter present on the left (M1 & M2) functions as a standard CMOS inverter. Therefore, the complement of input B is the output. When A=0 & B=0 , M2 is OFF, M1 and M3 are ON which leads to an undefined output state 'X', because M1 tends to pull down the output node while M3 tends to pull up the output node.

Similarly when A=0 & B=1, M1 is OFF, M2 and M3 are ON leading to an undefined output state 'X', because M2 tends to pull down the output node while M3 tends to pull up the output node. For A=0 & B=0 or 1, a strong logic '1' output is required. It is possible to obtain exact output logic levels with the proposed circuit, if the channel width of M3 is made 6 times that of M2 or 3 times that of M1.ie) $W_{M3} = 6 \times W_{M2} = 3 \times W_{M1}$. Thus M3 becomes much stronger than M1 and M2, giving a strong logic '1' at output when input A=0. An AND gate operation could be obtained with an additional CMOS inverter at the NAND output with 5 transistors. Table II gives the state table for 3T NAND gate for better understanding. Fig. 6 gives the input- output waveform for 3T NAND gate.

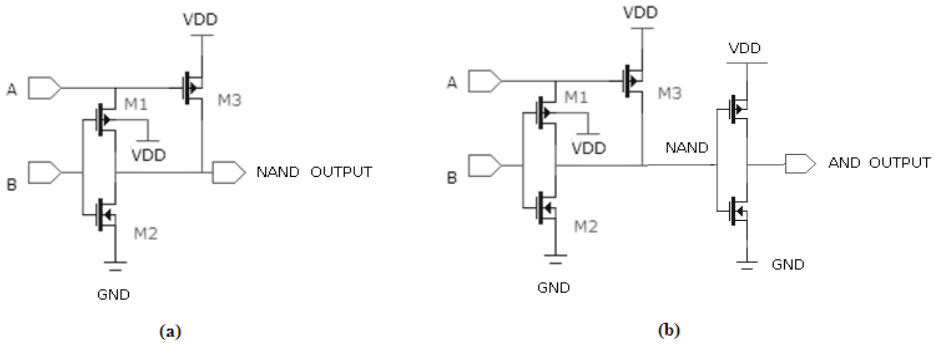

Fig. 5 (a) 3Tbased NAND gate (b) 5T based AND gate

TABLE II
STATE TABLE OF 3T NAND GATE

Inputs		Transistor State			NAND Output
		CMOS Inverter		PMOS Pass Transistor	
A	B	M1	M2	M3	
0	0	On	Off	On	1/ VDD
0	1	Off	On	On	1/ VDD
1	0	On	Off	Off	1/ B'
1	1	Off	On	Off	0/ B'

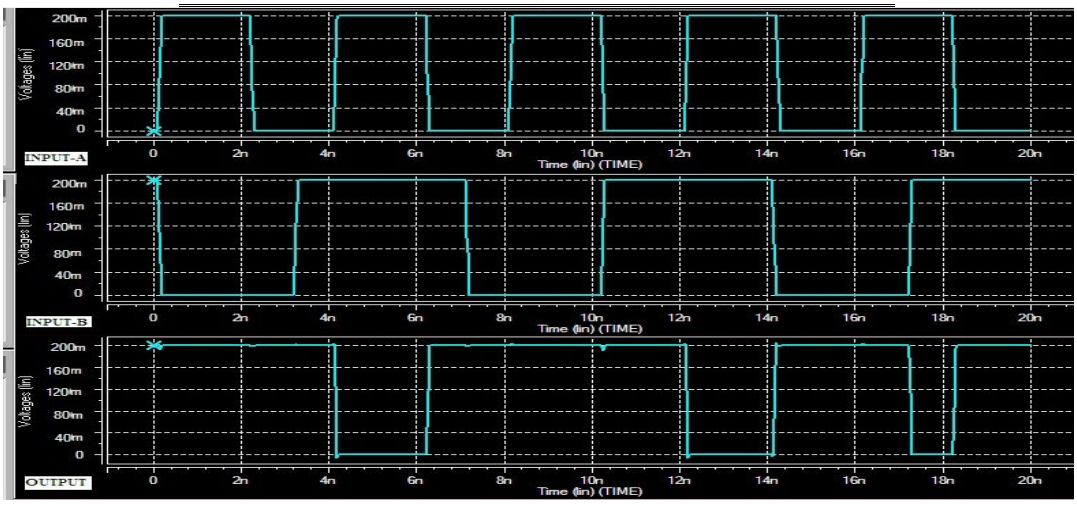

Fig. 6 Transfer characteristics of 3T NAND gate at 22nm with VDD=200Mv

IV. Results

In order to compare the results of proposed 3T based universal logic gates with existing NAND and NOR gate structures, a wide range of experiments was carried out. Schematics were designed for all circuits using Custom Designer in Synopsys for TSMC 0.18µm technology. Netlists from the schematics are utilized to simulate and test performance. The original netlists are modified according to the process technology targeted using Berkeley Predictive Technology Model (BPTM) 22nm process. The modified netlists are simulated using HSPICE tool from SYNOPSYS for delay and power estimations. The worst case delay and power measurements are made in all the cases with the operating temperature as 27°C. The performance of the proposed 3T NOR and 3T NAND circuits are evaluated based on their power dissipation and delay.

The transfer characteristics of proposed 3T Universal logic gates using HSPICE gave exact output logic levels without any voltage degradation. Logic gates of different logic structures reported in literature such as CMOS Logic, Double Pass Transistor Logic, Complementary Pass transistor Logic and Dual Value Logic have been simulated and comparisons have been presented in Table I [4]-[15]. For all logics except 3T logic gates, the transistor sizes are taken as width W_P=3.0µm for PMOS & W_n = 1.5µm for NMOS with constant length of L= 0.022µm (22nm). Fig. 7 gives the number of transistor count in each logic.

TABLE III
Power Dissipation for the Logic Gate Circuits in 22nm Process Technology with Power in Watts and Delay in PS

Logic Gate @ VDD=1V	CMOS logic		Double Pass Transistor Logic (DPL)		Complementary Pass Transistor Logic (CPL)		Dual Value Logic (DVL)		Proposed 3T based		Percentage of Power Savings compared to CMOS
	Power	Delay	Power	Delay	Power	Delay	Power	Delay	Power	Delay	
NAND	2.4743 E-12	47.1	5.5184E-12	49.5	5.8200 E-12	51.3	3.6920 E-12	51.6	1.8661 E-12	38.2	33
NOR	2.7644 E-12	54.8	5.7154E-12	53.2	6.0181 E-12	53.8	3.9153 E-12	59.8	2.1121 E-12	39.2	30

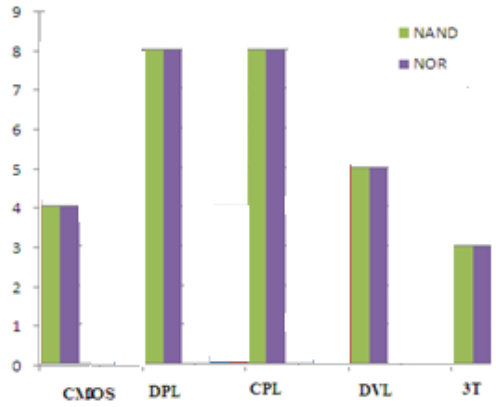

Fig. 7 Transistor count for each logic

From the results in Table III, the following can be inferred

- ✓ The dynamic power dissipation and area increases with the increase in number of switching transistors.
- ✓ Column 6 indicates that there is a lower power dissipation (dynamic & leakage) for a 3 transistor based logic gates compared to other logic gate structures.
- ✓ With a focus on delay, from column 6, the optimum delay for 3 transistor based logic gates obtained.
- ✓ Column 7 shows that 3T logic gates give more power savings compared with CMOS base case.

A. Motivation Example – SR Latch and C17 Benchmark Circuit

For evaluation of 3T NOR and 3T NAND, SR latch and the C17 benchmark circuits were considered respectively. SR latch and the C17 benchmark circuits are more complicated design example with branching, multiple fan-in and fan-out. Fig. 8 gives the gate level structure of SR latch and C17 benchmark circuits respectively.

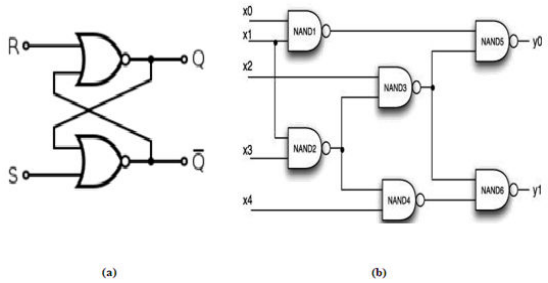

Fig. 8 (a) SR latch using NOR gates (b) C17 benchmark circuit using NAND gates

Tables IV and V gives the simulation results for SR latch and C17 benchmark circuits respectively. We have used SYNOPSYS HSPICE at 22nm with VDD = 0.2V for simulation. Column 2 of Tables IV and V gives the numerical results for SR latch and C17 circuits implemented using CMOS NOR and CMOS NAND gates respectively. Column 3 of Tables IV and V, gives the results for SR latch and C17 circuits implemented with proposed 3T NOR and 3T NAND gates respectively. Power and delay values compared shows that the circuit implemented with 3T gates give better result than the other circuit with optimum PDP. Row 5 of Tables IV and V give the count of number of transistors.

TABLE IV
SIMULATION RESULTS FOR SR LATCH

Parameters	3T NOR based SR latch	CMOS NOR based SR latch
Dynamic Power	5.4219 E-12 W	6.8401 E-12 W
Delay	89.01 ps	121.4 ps
PDP	482.6 E-24 J	830.3 E-24 J
Transistor Count	6	8

TABLE V
SIMULATION RESULTS FOR C17 BENCHMARK CIRCUIT

Parameters	3T NAND based C17 circuit	CMOS NAND based C17 circuit
Dynamic Power	35.4559 E-12 W	52.4860 E-12 W
Delay	104.4 ps	166.2 ps
PDP	3701.6 E-24 J	8723.2 E-24 J
Transistor Count	18	24

V. CONCLUSION

In conclusion, this paper presents a new set of 3T based Universal logic gates based on PTL and CMOS logic for high speed computer networks. The proposed 3T gates resulted in low power dissipation and high speed compared to the existing logic structures. According to HSPICE simulation in 22 nm CMOS BPTM process technology under given conditions and at room temperature, the proposed 3T gates shows an improvement of 32% less power consumption on an average over conventional CMOS logic gates. The devices designed with 3T gates will make longer battery life by ensuring extremely low power consumption.

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