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Replacing MOSFETs with Single Electron Transistors (SET) to Reduce Power Consumption of an Inverter Circuit

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***Abstract*—** According to the rules of quantum mechanics there is a non-vanishing probability of for an electron to tunnel through a thin insulating barrier or a thin capacitor which is not possible according to the laws of classical physics. Tunneling of electron through a thin insulating barrier or tunnel junction is a random event and the magnitude of current flowing due to the tunneling of electron is very low. As the current flowing through a Single Electron Transistor (SET) is the result of electron tunneling through tunnel junctions of its source and drain the supply voltage requirement is also very low. As a result, the power consumption across a Single Electron Transistor is ultra-low in comparison to that of a MOSFET. In this paper simulations have been done with PSPICE for an inverter built with both SETs and MOSFETs. *35mV* supply voltage was used for a SET built inverter circuit and the supply voltage used for a CMOS inverter was *3.5V*.

***Keywords*—**ITRS, enhancement type MOSFET, island, DC analysis, transient analysis, power consumption, background charge co-tunneling.

I. Introduction

THE advancement CMOS Technology has been done by the engineers for almost 30 years under Moore's law. Some researchers showed that possibly CMOS cannot be scaled down further after a few next years. International Technology Road map for Semiconductors (ITRS) has determined the size of integrated circuits for next several years obeying the rule of Moore's Law. MOSFET (metal oxide semiconductor field effect transistor) is taken to be the leading electronic device in the plan of ITRS. According to ITRS the present computing hardware are based on '22 nanometer' technology. 22 nm technology means the feature size (generally the gate length) of a typical MOSFET is 22 nm. ITRS has a roadmap where 14 nm technology, 10 nm technology and 7 nm technology will be the successor to 22 nm technology in 2014, 2016 and 2018 respectively. The minimum size of the MOSFET does not support the 7 nm technology and not even 10 nm technology (MOSFET can support up to 11nm technology only). So it is clearly understood that CMOS technology is gradually getting invalid under Moore's Law [1]. To assure further development in this field, new switching devices must be introduced. In this condition Single electron transistor (SET), an ultra-small device can be a promising replacement of MOSFET. Low supply voltage requirement and the tunneling current made SET a promising upcoming device.

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II. Supporting Theories

A. Theory of MOSFET

In CMOS technology generally the engineers use enhancement type MOSFETs. In case of enhancement type NMOS the threshold voltage V_{tn} (at zero body bias) is taken to be positive and in case of enhancement type PMOS the threshold voltage V_{tp} (at zero body bias) is taken to be negative [2]. Figs. 1 and 2 show an enhancement type NMOS and enhancement type PMOS respectively.

For an NMOS the current I_D flows through it from drain to source and (1)-(3). When NMOS is in cut off region ($V_{GS} \le V_{tn}$),

$$I_D = 0 \tag{1}$$

When NMOS is in resistive region ($V_{GS} \ge V_{tn}$ and $V_{DS} < V_{GS} - V_{tn}$),

$$I_D = \frac{\varepsilon \mu_n}{D} \frac{W_n}{L_n} \left[(V_{GS} - V_{tn}) V_{DS} - \frac{{V_{DS}}^2}{2} \right] \tag{2}$$

When NMOS is in saturation region ($V_{GS} \ge V_{tn}$ and $V_{DS} \ge V_{GS} - V_{tn}$),

$$I_D = \frac{1}{2} \frac{\varepsilon \mu_n}{D} \frac{W_n}{L_n} (V_{GS} - V_{tn})^2 \tag{3}$$

where, μ_n = mobility of an electron. For a PMOS the current I_D flows through it from source to drain and follows (4), (5) and (6). When PMOS is in cut off region ($V_{SG} \le |V_{tp}|$),

$$I_D = 0 \tag{4}$$

When PMOS is in resistive region ($V_{SG} \geq |V_{tp}|$ and $V_{SD} < V_{SG} - |V_{tp}|$),

$$I_D = \frac{\varepsilon \mu_p}{D} \frac{W_p}{L_p} \left[\left(V_{SG} - |V_{tp}| \right) V_{SD} - \frac{{V_{SD}}^2}{2} \right] \quad (5)$$

When PMOS is in saturation region ($V_{SG} \geq |V_{tp}|$ and $V_{SD} \geq V_{SG} - |V_{tp}|$),

$$I_D = \frac{1}{2} \frac{\varepsilon \mu_p}{D} \frac{W_p}{L_p} \left(V_{SG} - |V_{tp}| \right)^2 \quad (6)$$

where, μ_p = mobility of a hole. These equations [3] were used to simulate a MOSFET based inverter circuit.

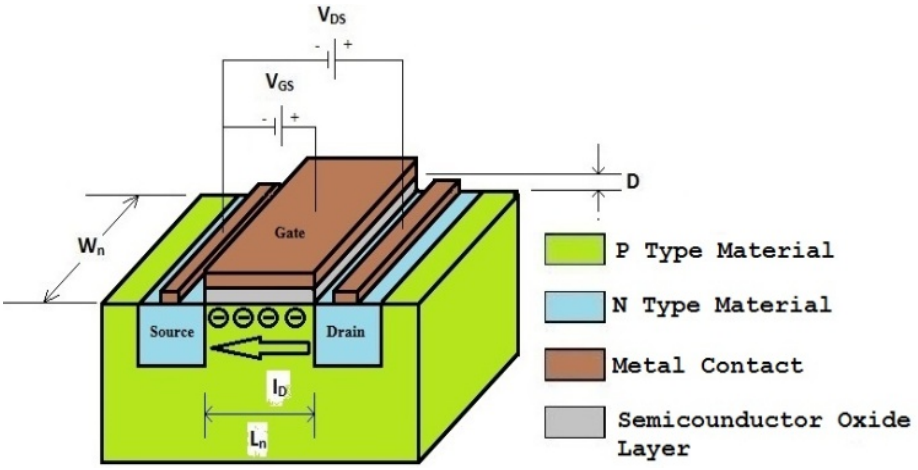

Fig. 1 Structure and action of an enhancement type NMOS

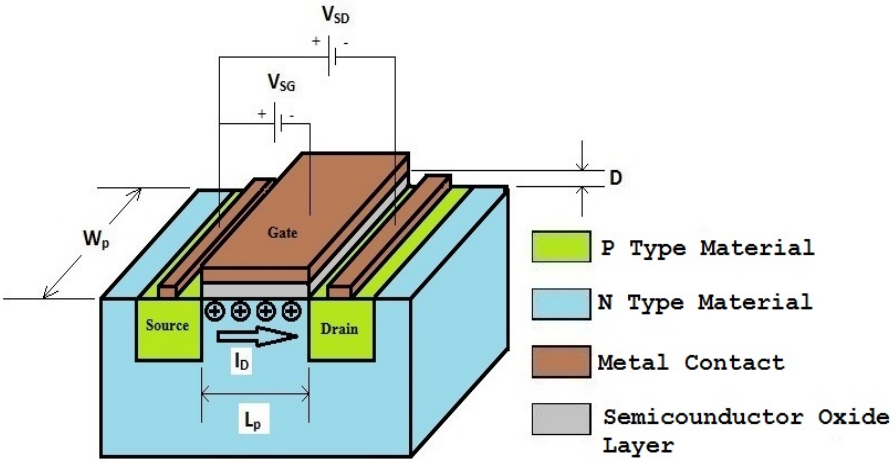

Fig. 2 Structure and action of an enhancement type PMOS

B. Theory of Single Electron Transistor (SET)

Fig. 3 shows a typical single transistor which has 3 electrodes-gate, source and drain and an island. For the purpose of proper switching another gate (gate 2) has been introduced. The gates are coupled with the island (sometimes which is termed as quantum dot) with two capacitors C_{G1} and C_{G2} respectively. Source and drain are connected with the island by two tunnel junctions. These two tunnel junctions have ultra-low capacitive impedance C_1 and C_2 respectively. By the two gates the condition of flowing tunneling current from source to drain can be controlled. Here one thing should be remembered that the current flow causes due to tunneling of electrons through the two tunnel junctions.

Fig. 4 shows the equivalent circuit for a SET. An output stray capacitor C_0 and a background charge Q_0 is introduced to this circuit model. SET is extremely charge sensitive which causes the background charge.

When *ne* (where *n* = an integer which indicates the number of elementary charges i.e., an electron that was added to the island and *e* = positive elementary charge) charge is present on the island then simple electrostatics show that voltage of the island *V* (which is a function of *n*):

$$V(n)=\frac{(ne+V_1C_1+V_2C_2+V_{G1}C_{G1}+V_{G2}C_{G2}+Q_0)}{C_\Sigma} \quad (7)$$

here, $C_\Sigma = C_1 + C_2 + C_{G1} + C_{G2} + C_0$.

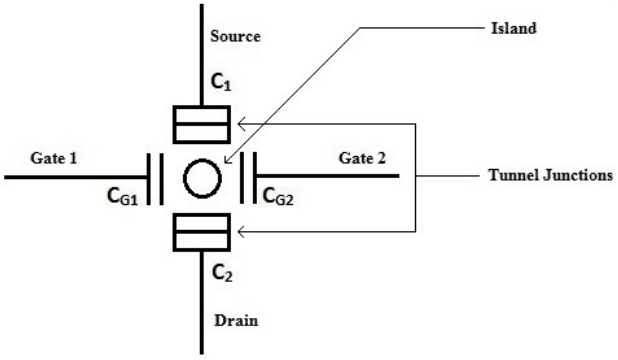

Fig. 3 Circuit representation of a single electron transistor (SET)

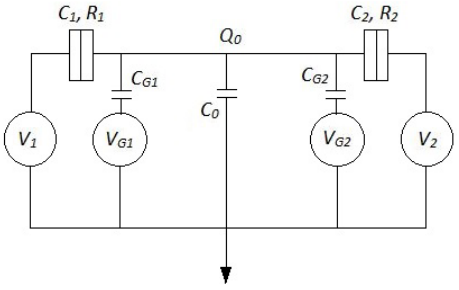

Fig. 4 Single electron transistor–schematic diagram

The amount of electrostatic energy needed to add a charge equivalent to e can be expressed by (8):

$$eV(n)+\frac{e^2}{2C_\Sigma} \quad (8)$$

The change of energy due to the tunneling of a charge e from a lead to the island is ΔE_i. Assume the voltage of the lead is V_i. So,

$$\Delta E_i = -eV_i + eV(n) + \frac{e^2}{2C_\Sigma} \quad (9)$$

Tunnel resistance, absolute temperature and the Boltzmann constant are expressed by R_i, T and k respectively. Now the rate of tunneling Γ_i can be calculated using the change of energy due to the tunneling of a charge e.

$$\Gamma_i = \frac{\Delta E_i}{e^2 R_i\left(\frac{\Lambda E_i}{kT}-1\right)} \quad (10)$$

Higher order tunnel events where two or more charges tunnel simultaneously are called co-tunneling. Co-tunneling has been ignored here. Therefore, there are four possible ways of tunneling of charge e. They are, Γ_{L1}= tunneling through tunnel junction 1 towards left, Γ_{L2} = tunneling through tunnel junction 2 towards left, Γ_{R1}= tunneling through tunnel junction 1 towards right, Γ_{R2}= tunneling through tunnel junction 2 towards right.

After determining the tunnel rates for all the pertinent charge states the probabilities of the charge states' getting occupied can be calculated from (11):

$$P(n) = P(n-1)\left(\frac{\Gamma_{L2}(n-1)+\Gamma_{R1}(n-1)}{\Gamma_{R2}(n)+\Gamma_{L1}(n)}\right) \quad (11)$$

The average current from tunnel junction 1 to 2 can be determined from (12):

$$I = \sum_n eP(n)\left(\Gamma_{R1}(n)-\Gamma_{L1}(n)\right) \quad (12)$$

Then island's average voltage can be determined by (13):

$$V = \sum_n V(n)P(n) \quad (13)$$

The voltage and current can be calculated efficiently the charge state n should be calculated which has the highest possibility to be occupied. This charge state can be calculated by the (14):

$$n_{opt} = \frac{(Q_0+V_1C_1+V_2C_2+V_{G1}C_{G1}+V_{G2}C_{G2})}{e} + \frac{C_\Sigma}{e}\frac{R_2V_1+R_1V_2}{R_1+R_2} \quad (14)$$

The basic operation of single electron transistor can be found in [4] and all these equations which were implemented using the orthodox theory of electron tunneling [5] in SET SPICE model are available in [6].

III. The Simplest Digital Circuit: An Inverter

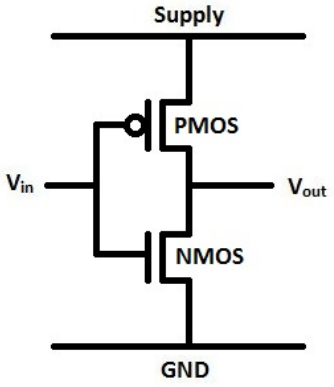

Fig. 5 CMOS inverter

Fig. 6 shows an inverter using SET. The island of the upper SET is red colored. This means the background charge is

negative. For exactly the opposite reason the island of the lower SET is blue colored. The sign of the background charge of red and blue islands are opposite but their absolute values are assumed equal. A short description on background charges and SET inverter characteristics can be found in [7].

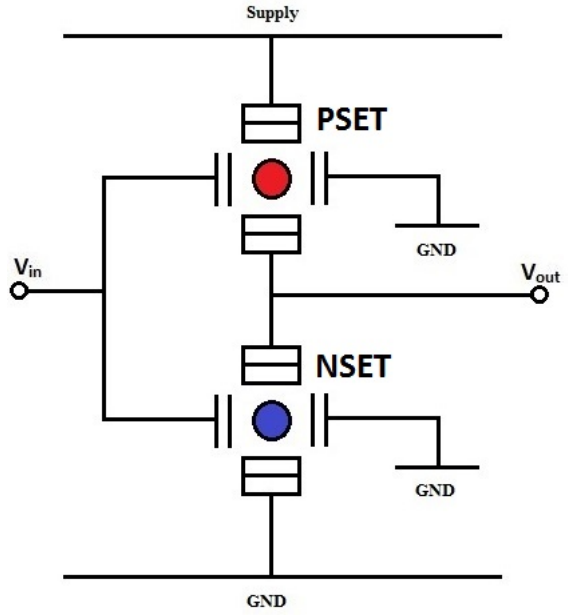

Fig. 6 SET based inverter

IV. Comparisons of CMOS Inverter and SET Based Inverter

A. Comparison of DC Analysis

Both circuits were simulated in PSPICE. Figs. 7 and 8 show the simulation results of the DC analysis of inverters using MOSFET and SET respectively.

- In case of CMOS inverter, the supply voltage=3.5 V, inversion voltage=1.7514 V.
- In case of SET built inverter, the supply voltage=3.5 mV, inversion voltage=17.514 mV.

B. Comparison of Transient Analysis and Power Consumption

The input voltage & output voltage curves and the power consumption curves across PMOS & NMOS for a CMOS inverter circuit are shown in Figs. 9 and 10 respectively. Again the input voltage & output voltage curves and the power consumption curves across PSET & NSET for a SET based inverter circuit are shown in Figs. 11 and 12 respectively.

Taking power consumption values for different times the average power consumption has been calculated using MATLAB for both circuits. Following observation were made from the simulated results of MATLAB:

- For a CMOS inveter: The average power dissipation across PMOS = 3.3713×10^{-5} Watt. The average power dissipation across NMOS = 3.1703×10^{-5} Watt. The total average power dissipation across the CMOS inverter = 6.5416×10^{-5} Watt.
- For a SET based inveter: The average power dissipation across PSET = 6.6063×10^{-12} Watt. The average power dissipation across NSET = 6.7228×10^{-12} Watt. The total average power dissipation across the SET based inverter = 13.3291×10^{-12} Watt.

V. Conclusion

The PSPICE DC analysis and transient analysis show similar results for both CMOS inverter and SET based inverter. The simulation results clearly show that total power consumption of a SET based inverter is almost 5 million times less than that of CMOS inverter. Still this SPICE model has many limitations. This model has been designed considering the orthodox theory where co-tunneling is neglected. Moreover, these simulations were done taking the temperature at 27 k which is a very low temperature compared to the room temperature. If these limitations of SET can be minimized then SET can be a leading device in future technologies.

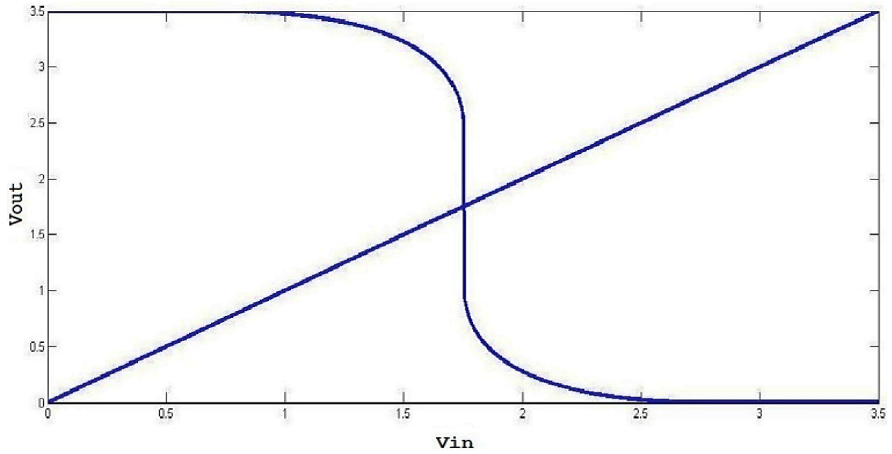

Fig. 7 DC characteristics of a CMOS inverter

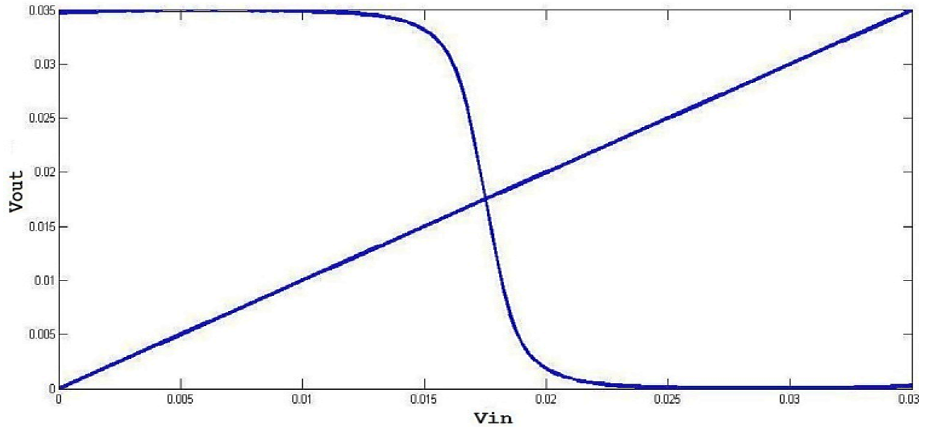

Fig. 8 DC characteristics of a SET based inverter

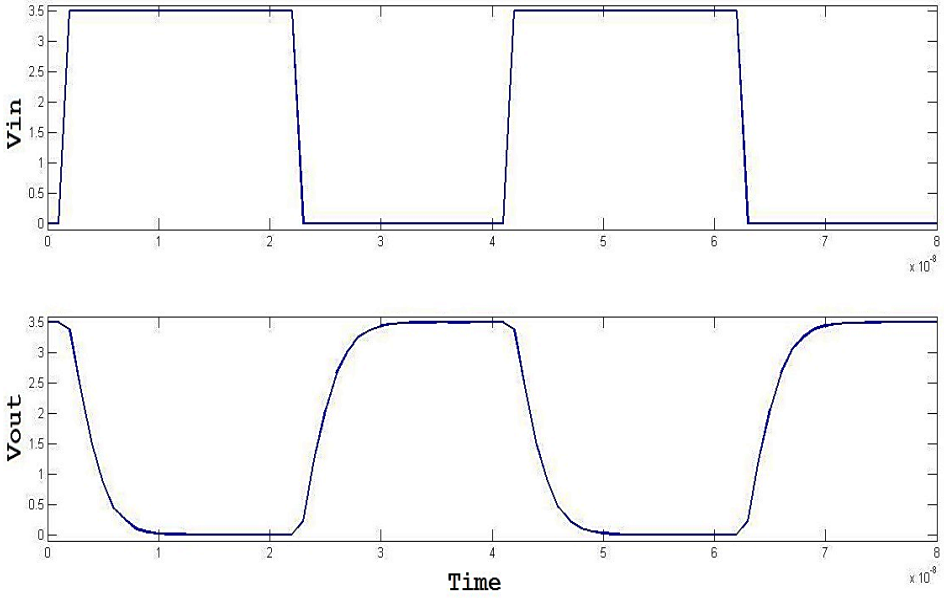

Fig. 9 Transient analysis of a CMOS inverter

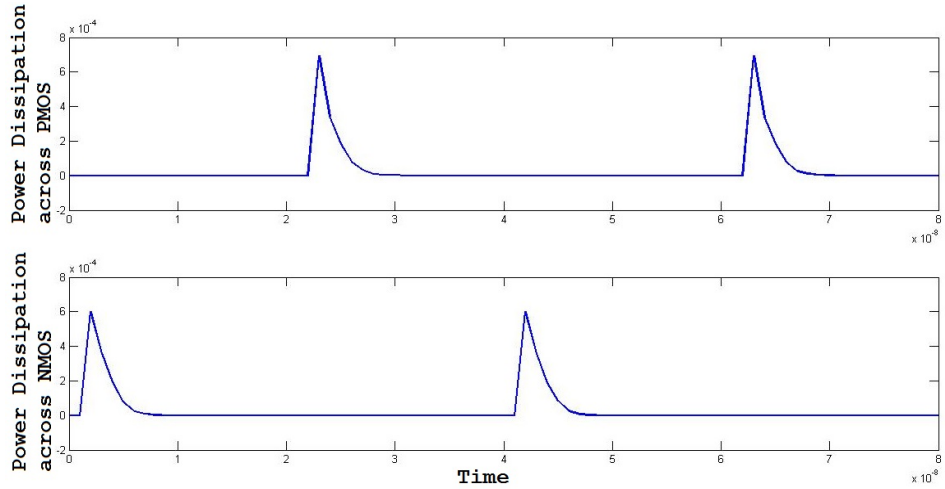

Fig. 10 Power consumption across the PMOS and the NMOS of a CMOS inverter

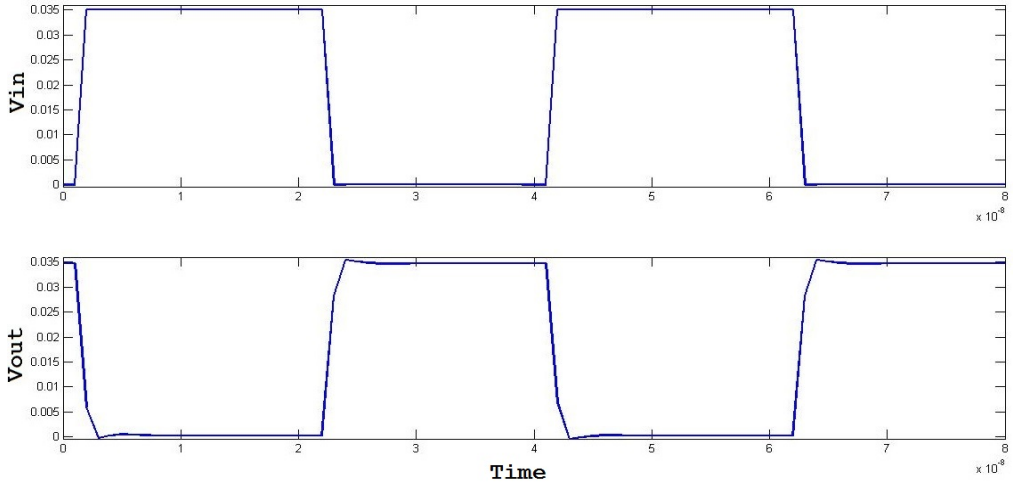

Fig. 11 Transient analysis of a SET based inverter

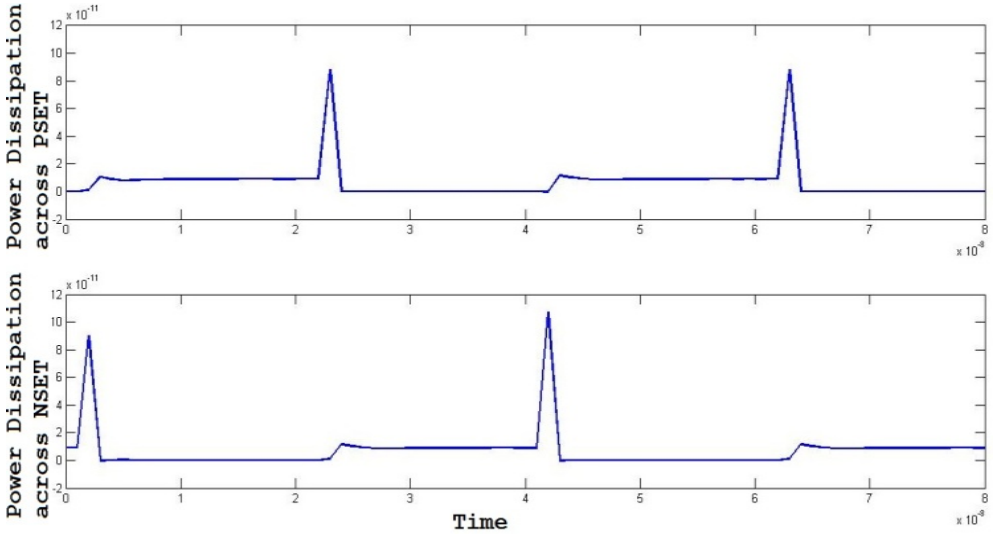

Fig. 12 Power consumption across the PSET and the NSET of a SET based inverter

REFERENCES

[1] R.R. Schaller, "Moore's Law: Past, Present, and Future," Spectrum, IEEE, vol. 34, pp. 52 - 59, August 2002.
[2] Douglas A. Pucknell and Kamran Eshraghian, Basic VLSI Design, 3rd ed., Prentice-Hall, 1995, pp.6-10.
[3] Linda E. M. Brackenbury, Design of VLSI Systems: A Practical Introduction, Macmillan, 1987, pp.13-18.
[4] K. K. Likharev, "Single-Electron Devices and Their Applications," Proceedings of the IEEE, vol. 87, pp. 606 - 632, August 2002.
[5] A. Scholze "Imulation of Single-Electron Devices," Ph.D. dissertation, Swiss Federal Institute of Technology, Zurich, Switzerland, 2000, pp.15-17.
[6] G. Lientschnig "Single-Electron and Molecular Devices," Ph.D. Thesis, Delft University of Technology, Delft, Netherlands, November 2003, pp.13-20.
[7] J. R. Tucker "Complementary Digital Logic Based on the Coulomb Blockade," Journal of Applied Physics, 72, 4399, 1992.