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Repetitive Control and Feedback Dithering Modulation of a DC/AC Converter

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***Abstract*—**Repetitive control and feedback dithering modulation are applied to a single-phase voltage source inverter, with an aim to eliminate harmonics and stabilize the inverter under load variations. The proposed control and modulation scheme comprise multiple loops of feedback, which helps improve inverter performance and robustness. Experimental results show that the designed inverter exhibits very low distortion at its output with THD of about 0.3% under different load variations.

***Keywords*—**Feedback dithering modulation, repetitive control, state feedback, inverter, harmonics elimination.

I. Introduction

THE he primary design issue for a DC-to-AC converter (or called inverter) is to maintain low total harmonic distortion (THD) under different loads [1]-[3]. Modulation and control are mainly responsible for the performance of the converter. The most common modulation scheme is the carrier-based pulse width modulation (PWM) [4]-[6]. The carrier-based PWM is effective and easy-to-use; however, it may produce significant inter-modulation harmonics and high-frequency switching harmonics, and is prone to circuit imperfections and supply variations. To compensate for the deficiency of the PWM, feedback control is usually applied to eliminate low-frequency harmonics and stabilize the converter. One of most effective control strategies for this purpose is repetitive control [1]-[3], which makes use of internal model principle [7, p. 400], placing controller poles on the frequencies of harmonics. However, the major disadvantage of repetitive control is its sensitivity to plant uncertainties (i.e., load variations in the case of inverter).

This work attempts to improve the performance of a DC-to-AC converter by employing the recently developed feedback modulation scheme called feedback dithering modulation [8], [9] in combination with the state-feedback repetitive control to enhance robustness. The experimental results shows that the additional feedbacks in modulation and control offer very low distortion (about 0.3% THD) at the converter output, and render the performance extremely insensitive to circuit non-idealities, supply variations and load variations.

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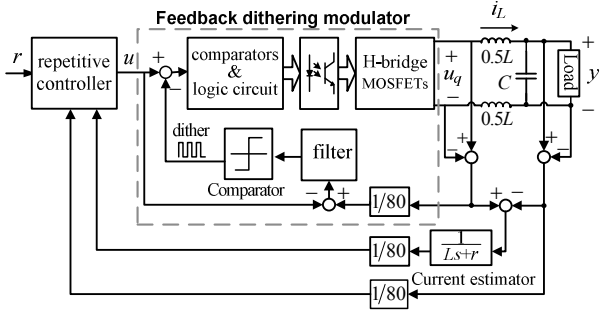

Fig. 1 Functional diagram of single-phase voltage source inverter

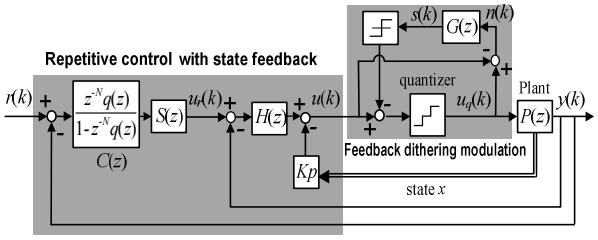

Fig. 2 Detailed block diagram of the proposed modulation and control

II. Inverter Design

Fig. 1 shows the proposed design of a single-phase voltage source inverter for converting a DC power to an AC power. It is composed of three parts: a repetitive controller, a feedback dithering modulator, and an output LC filter plus load. The repetitive controller, which has additional state feedback, is designed to eliminate harmonics and stabilize the inverter under load variations. The feedback dithering modulator is a feedback loop of circuits, including a filter, a comparator, a switching logic circuit, optocouplers, and an H-bridge of MOSFET transistors (see the dashed box in Fig. 1). The modulator converts control signal u into three-level switching waveform u_q at the output of the H-bridge. The modulator compares its output with input and automatically corrects low-frequency distortion and eliminates low-frequency noise. The output LC filter is responsible for filtering out high-frequency switching noise and recovering a desired sinusoidal waveform from the switching waveform.

Fig. 2 shows the block diagram of the control and modulation system associated with the inverter in Fig. 1. The plant P is the transfer function that describes the dynamics of

the LC filter combined with a load. A three-level quantizer represents the combined circuits of the switching logic, optocouplers, and H-bridge, and its three possible output levels corresponding to three conduction modes of the H-bridge (i.e., forward conduction, zero conduction and reverse conduction). The repetitive control includes the feedback of two state variables, output voltage u_q of the H-bridge and inductor current i_L. The inductor current is not directly measured but estimated using a current estimator that implements the admittance function of two inductors (see Fig. 1). The other detailed functions and designs of the feedback dithering modulation and repetitive control are separately explained in the following sections.

III. Design of Feedback Dithering Modulation

The feedback dithering modulator consists of a quantizer, a filter, and a comparator, as shown in Fig. 2. The modulator is actually made of a dithered quantizer; a three-level quantizer dithered by a binary signal that is generated by passing quantization noise n through filter G and a comparator. The binary dither signal is injected to the quantizer input to cancel low-frequency quantization error, thereby reducing low-frequency quantization noise [9]. The kind of modulator is operated in the sliding mode, with the filter output $s = 0$ defining the sliding surface in the state space. Quantizer output u_q (i.e., the modulator output or H-bridge output) can be expressed in the frequency domain as

$$U_q(\omega) = U(\omega) + G^{-1}(e^{j\omega})S(\omega) \tag{1}$$

where U_q, U, and S are the discrete-time Fourier transforms of u_q, u, and s, respectively. The output u_q contains the desired signal term u and the unwanted noise term which is the filter output s filtered by G^{-1}. Once the modulator is stabilized in the sliding mode, the swing of the filter output s is minimized and constrained to a certain level. G^{-1} is responsible for shaping the noise spectrum, and it can be designed to have very low gain in the frequency band of interest to eliminate unwanted noise.

Following the previous design [9], the filter G is chosen as a double integrator

$$G(z) = \frac{z-0.6}{z^2-2z+1},\ f_s = 5\times10^4 \text{ Hz} \tag{2}$$

where f_s is the sampling frequency. G^{-1} has very small gain at low frequencies, for eliminating low-frequency switching noise and harmonics at the H-bridge output.

IV. Design of Repetitive Control

Given 50 kHz sampling frequency and 50 Hz reference signal frequency, the repetitive control that includes the internal model of the 50Hz periodic signal is

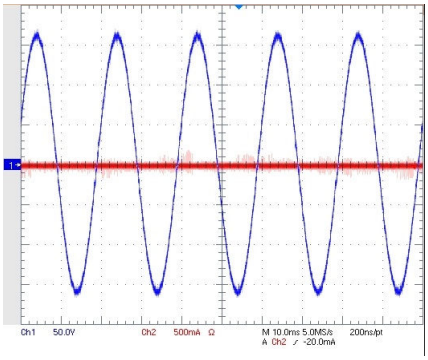

Fig. 3 Output voltage waveform (blue) and current waveform (red) of the inverter with its output open ($R_{load}=\infty$). The THD of the voltage waveform is 0.27%

TABLE I
Design Parameters

Switching Frequency	50 kHz
Input DC voltage	220 V
Output AC Voltage	110 Vrms
Output Frequency	50 Hz
Inductors' Inductance L	2.5 mH
Inductors' series resistance	0.22 Ω
Capacitor's capacitance C	10 μF

$$C(z) = \frac{z^{-N}q(z)}{1-z^{-N}q(z)},\ N = 1000 \tag{3}$$

where $q(z)$ is a zero-phase, unit-gain, lowpass filter, for giving up elimination of harmonics of frequencies above 500 Hz, in exchange for improved robustness for high-frequency uncertainties of the plant [10].

The state-feedback part of the repetitive control is designed by first regarding the feedback dithering modulator as perfectly linear and using the frequency-shaped LQR optimization method [11], [12] to derive the optimal control:

$$H(z) = \frac{0.068}{z-1} \tag{4}$$

Since H has high gain at low frequencies, the transfer function P' from u_r to y will approximate 1 within the 500Hz bandwidth of repetitive control. $S(z)$ can be used to further compensate for the deviation of P' from 1 at low frequencies to meet the sufficient stability condition [10].

$$\left\| q(z)(1-S(z)P'(z)) \right\|_\infty < 1 \tag{5}$$

The role of filter q becomes clear now. At high frequencies where SP' deviates significantly from 1, the roll-off of magnitude response of q helps maintain stability.

V. Experimental Results

Table I shows the design parameters of the inverter. The inverter converts a 220V DC power into a 50Hz 110V AC

power. The cutoff frequency of the LC output filter is 1 kHz. The modulator and controller are implemented on Altera's DE2-70 FPGA Board. The interface between the FPGA and the H-bridge is similar to that in [9], comprising two voltage-sensing lowpass amplifiers (for measuring signals u_q and y) with 25 kHz cutoff, two 12Bit analogue-to-digital converters ADS7810U, opto-couplers A3180, and Predrivers IR2110. The dead time for avoiding shoot-through current of the H-bridge is 1.2μs. The 50Hz sinusoidal reference signal is generated by a lookup table in the FPGA.

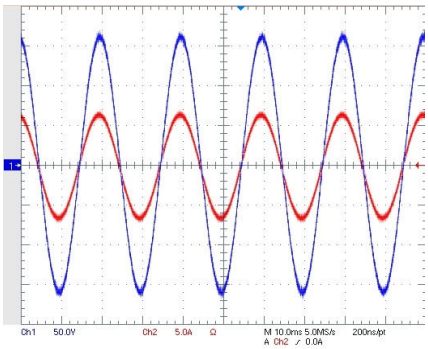

Fig. 4 Output voltage waveform (blue) and current waveform (red) of the inverter when attached to a 25Ω load. The THD of the voltage waveform is 0.32%

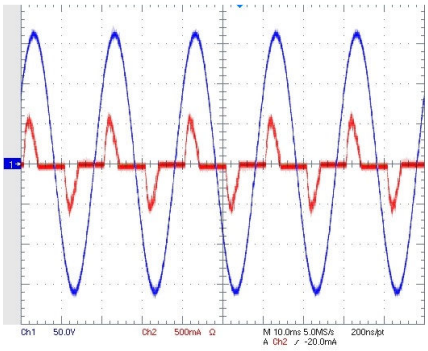

Fig. 5 Output voltage waveform (blue) and current waveform (red) of the inverter when attached to a *non-linear rectifier load*. The THD of the voltage waveform is 0.29%

Figs. 3-5 display the output voltage and current waveforms of the designed inverter when attached to different loads. It shows a consistent high performance with the THD of about 0.3%. Figs. 6 and 7 plot the voltage and current waveforms of the inverter in response to a sudden change in load. The output voltage waveform contains some unwanted glitches; the larger the current change, the larger the glitch (Compare Figs. 6 and 7). The output waveform quickly becomes normal, except for another glitch at the same position of the next period. This is the result of the periodic learning of the repetitive controller, which anticipates similar current change at the next period and tries to compensate for it.

VI. Concluding Remark

The feedback dithering modulation and the repetitive control with additional state feedback are applied to a single phase voltage source inverter. The additional feedbacks in modulation and control enhance the performance and robustness of the inverter. The only drawback of the presented modulation and control schemes is its complexity.

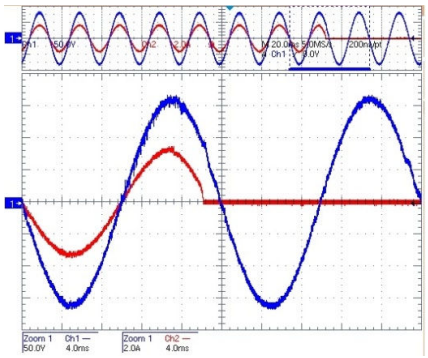

Fig. 6 Output voltage waveform (blue) and current waveform (red) of the inverter when its load changes from 50 Ω to ∞ Ω.

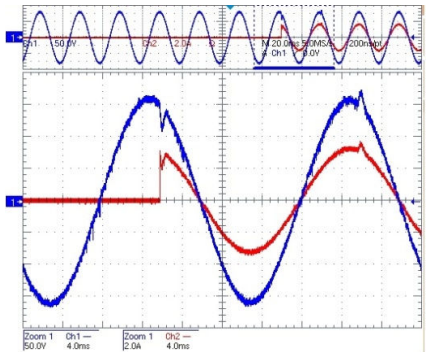

Fig. 7 The inverter load change from ∞ Ω to 50 Ω causes an instaneous 26.7% drop in the output voltage

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