Reduction of Peak Input Currents during Charge Pump Boosting in Monolithically Integrated High-Voltage Generators

Jan Doutreloigne

Abstract—This paper describes two methods for the reduction of the peak input current during the boosting of Dickson charge pumps. Both methods are implemented in the fully integrated Dickson charge pumps of a high-voltage display driver chip for smart-card applications. Experimental results reveal good correspondence with Spice simulations and show a reduction of the peak input current by a factor of 6 during boosting.

Keywords—Bi-stable display driver, Dickson charge pump, high-voltage generator, peak current reduction, sub-pump boosting, variable frequency boosting.

I. INTRODUCTION

CHARGE pumps are used in a wide variety of applications, going from flash memories to display drivers. Depending on the application, various parameters are important. Good overall efficiency is of course a general requirement, but some applications ask specifically for a low supply voltage, high current drive capability or high output voltages.

A factor that is often ignored, is the peak input current of the charge pump. Although irrelevant for some applications, it can be a major requirement for others. Imagine for instance a smart-card application with embedded bi-stable display and display driver. The nature of the smart-card application does not allow integration of on-board batteries to power the system. Therefore, on-board electronics has to rely on electrical energy fed through smart-card contacts or delivered by an on-board RF chip that captures an electromagnetic field in case of contact-less smart-cards. It is clear that - especially in the latter case - the available supply current, and to a lesser degree also the supply voltage, is limited. Commercially available RF chips for smart-card applications can only cope with a few mA at a 3V output voltage. Add to this the relatively high driving voltages for bi-stable displays (some over 50V) and the high number of charge pump stages needed to generate these voltage levels from a low supply voltage, and one can see that successful boosting of the relatively large charge pumps becomes challenging. With the peak input current exceeding the maximum rating of the RF chip, normal operation of the RF chip cannot be guaranteed. The

Jan Doutreloigne is with the Centre for Microsystems Technology (CMST), affiliated to the Interuniversity Microelectronics Centre (IMEC) and the University of Gent, Technologiepark 914A, 9052 Zwijnaarde, Belgium (phone: +32-(0)9-264-53-56; fax: +32-(0)9-264-53-74; e-mail: jdoutrel@elis.ugent.be).

transaction between the smart-card terminal and the card itself possibly fails, resulting in erratic display updates.

In this paper, attention is paid to methods for peak input current reduction during charge pump boosting. Two specific methods will be analyzed and discussed in detail. Both these methods are implemented in the high-voltage generators of a prototype bi-stable display driver chip for smart-card applications.

II. CHARGE PUMP CIRCUIT

The charge pump we used in the bi-stable display driver, is based on the Dickson architecture originally described in [1] and shown in Fig. 1.
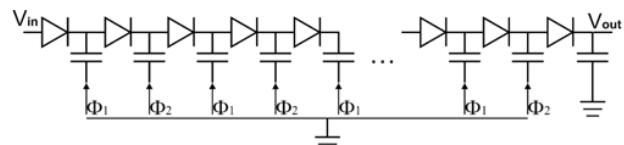

Fig. 1 Schematic of the 2-phase Dickson charge pump

A basic set of formulas derived for dimensioning this type of capacitive Dickson charge pump, can be found in [2] and [3]. Additional formulas for implementing several types of efficiency-boosting techniques are given in [4] and [5]. Using these formulas, we designed completely integrated Dickson charge pumps capable of producing output voltages up to 55V out of a 3V power supply. Since the charge pumps are embedded in a display driver for bi-stable LCDs, an extra control circuit to make the charge pump suitable for display addressing was added. A simplified diagram of the resulting Dickson-based charge pump with added control circuit is shown in Fig. 2.
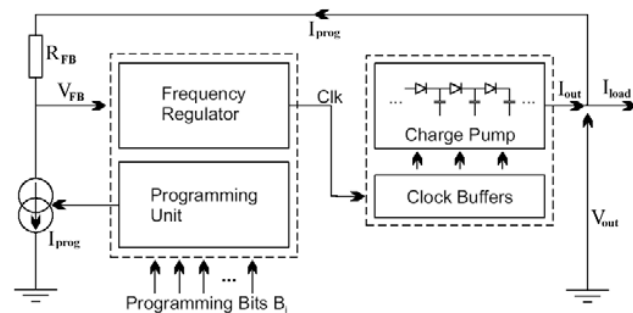

Fig. 2 Dickson charge pump with control circuit

The programming unit allows setting the output voltage in a range from 0V to 55V with 8 bit precision. The relationship between the programming bits B_i and the output voltage in a steady-state condition of the circuit, is given by:

$$V_{out} = V_{FB} + R_{FB} \cdot I_{prog} = V_{FB} + \frac{V_{ref}}{256} \cdot \frac{R_{FB}}{R_{ref}} \cdot \sum_{i=0}^{7} B_i \cdot 2^i$$

V_{ref} is a reference voltage used inside the programming unit. The reference voltage is converted into a reference current using resistor R_{ref}. From the reference current, secondary currents proportional to the weights of the programming bits B_i are derived. Adding up these currents yields the programming current I_{prog}. The feedback voltage V_{FB} is connected to a high-impedance input of a frequency regulator. The frequency regulator continuously adjusts the clock frequency of the charge pump depending on the difference between the actual output voltage (measured by sensing V_{FB}) and the desired output voltage. Therefore, the charge pump offers minimal output ripple and can cope with a variety of load conditions while still maintaining stable output voltages, set by the programming unit.

One can see that embedding a high-voltage generator of Fig. 2 in applications with limitations on the available supply voltage and supply current, provides a challenge. First of all, to convert a 3V supply voltage into a 55V output voltage requires a Dickson charge pump with a relatively high number of stages. Boosting requires a high peak input current considering the number of stages and the total charge pump capacitance. Combining several of those charge pumps together in one driver chip will increase the peak input current even more, especially if they all boost at the same time. Finally, the natural tendency of the control circuit to use the highest available clock frequency during boosting, will also have an effect on the peak input current. Considering all these factors, one can feel the need for reducing the peak input current related to the boosting process of the high-voltage generator. In the following sections, we will propose some crucial architectural changes and two specific methods for peak input current reduction during boosting.

III. PEAK INPUT CURRENT REDUCTION

A. Sequential Sub-Pump Boosting

A first method for reducing the peak input current during boosting relies on the fact that the value of this peak current strongly depends on the number of stages in the charge pump and therefore also on the total charge pump capacitance. The proposed principle of sequential sub-pump boosting is shown in the diagram of Fig. 3. Normally, all stages of the charge pump are boosted at the same time. However, by dividing the charge pump in smaller groups of stages that boost sequentially, it is possible to reduce the total capacitance the clock buffers initially see and therefore to reduce the peak input current.
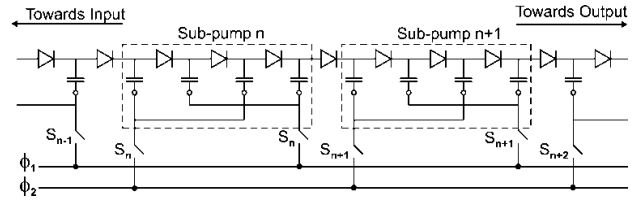

Fig. 3 Sub-pump boosting architecture

To evaluate the principle of sequential sub-pump boosting, a fully integrated 36-stage Dickson charge pump was designed using the ON Semiconductor 0.7μm I2T100 technology, capable of 55V output voltage from a 3V supply at a load current of 50μA. The stage capacitance and output capacitance are both 10pF. Using sub-pump boosting, the 36-stage pump is split in 6 groups of 6 stages that can be considered as individual sub-pumps within the global pump. The sub-pumps are boosted sequentially, starting at t = 0μs with 50μs intervals. Since the peak input current is relatively independent of the load current, the load current of 50μA was already drawn from the output during boosting. The clock frequency is constant at 7.5MHz. In this case, the sub-pumps are boosted from the output of the global pump towards the input, starting with the last sub-pump, followed by the penultimate and so forth. The actual operation of the global charge pump, however, remains the same with voltage build-up from the first towards the final stage where load currents are being applied.

Fig. 4 shows a Spice simulation result of the input current in such a charge pump with 36 stages during normal boosting and sub-pump boosting. The corresponding output voltages are shown in Fig. 5.
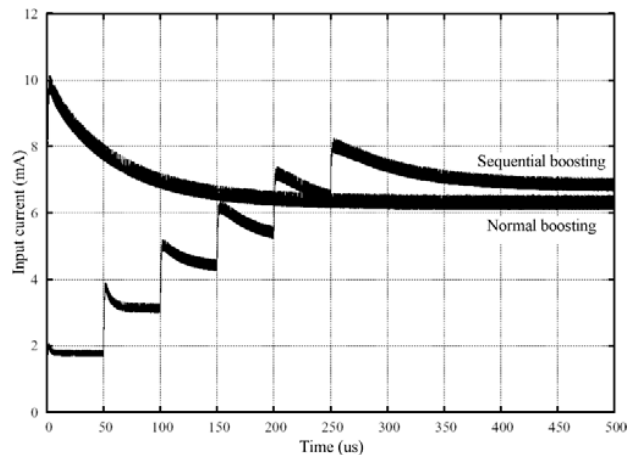

Fig. 4 Input current comparison between normal and sequential output-to-input sub-pump boosting

Fig. 4 shows the peak input current being reduced from 10.18mA to 8.25mA by sub-pump boosting over normal boosting. The trade-off manifests itself in a higher overall input current during normal operation due to the added circuitry for sub-pump boosting. The final output voltage for the sub-pump boosting is somewhat lower at 52.88V

compared to 53.93V for normal boosting, due to small voltage drops over the switches in the clock lines, degrading the voltage gain per stage towards the output. Fig. 5 also reveals the effect on the output voltage being delayed more when sub-pumps closer to the input of the pump are activated.
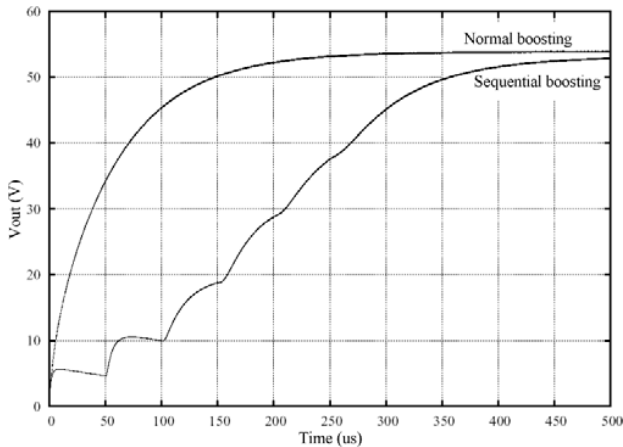

Fig. 5 Output voltage comparison between normal and sequential output-to-input sub-pump boosting

The order in which the different sub-pumps are boosted can also be reversed. Figs. 6 and 7 show the input current and output voltage for both boosting methods with the same charge pump, but this time with sub-pump boosting from the input to the output.
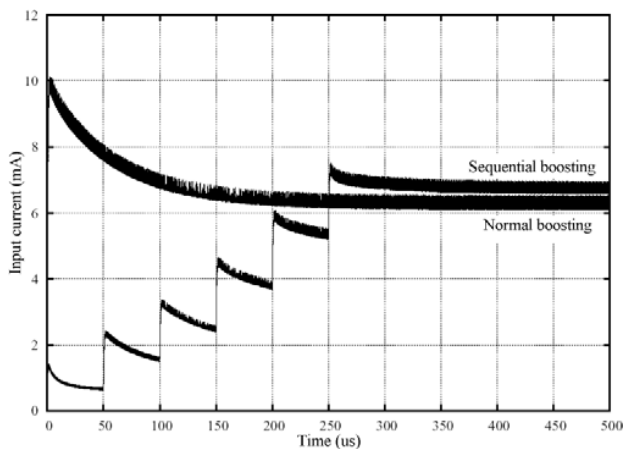

Fig. 6 Input current comparison between normal and sequential input-to-output sub-pump boosting

Although the behavior of the output voltage during sub-pump boosting in this direction is different, the steady-state output voltage is exactly the same compared to sub-pump boosting from output to input. The peak input current during boosting, however, is smaller by approximately 9% when using sub-pump boosting from input to output. During sub-pump boosting from input towards output, sub-pumps that are not yet clocked, already exhibit charge build-up in their stages due to charge transfer through the stage diodes of previous,

already clocked sub-pumps. Therefore, when the clocks of a subsequent sub-pump are switched on, the resulting peak input current is smaller due to the charges already stored in the capacitors of the sub-pump that has just been switched on. In output-to-input sub-pump boosting, there can be no reverse charge transfer from one sub-pump to a previous sub-pump. Therefore, when a previous sub-pump is switched on, the resulting peak input current is larger since there were no charges stored on the sub-pump capacitors. For the same reason, input-to-output boosting is intrinsically faster than output-to-input boosting. Fig. 7 compared to Fig. 5 reveals a reduction of the boosting time of approximately 100µs in favor of the input-to-output direction.
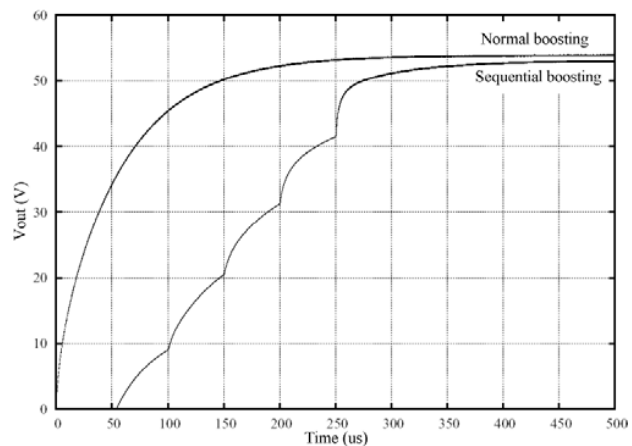

Fig. 7 Output voltage comparison between normal and sequential input-to-output sub-pump boosting

Obviously, the method of sub-pump boosting for reduction of the peak input current will be more effective when the number of sub-pumps increases. Sub-pump boosting, however, asks for direct modifications in the clock lines between the clock buffers and the charge pump capacitors, making this technique less desirable for several reasons. For instance, switches in the clock lines for sub-pump boosting slightly decrease the maximum pumping gain per stage towards the end of the charge pump due to small voltage drops over the series of switches. This effect is already visible in Figs. 5 and 7 and will only increase with increasing number of sub-pumps. Furthermore, switches potentially add additional delays to the clock signal towards the output of the charge pump. This combined with the high clock frequencies used and the large stage count in the charge pump, can lead to a phase shift of the clock signal at the end of the pump, resulting in an overlapping 2-phase clock signal in the final stages.

B. Variable Frequency Boosting

In the previously described sub-pump boosting method, a constant clock frequency is used during boosting of the individual sub-pumps. Reduction of the peak input current is obtained by exploiting the peak current dependency on the number of stages and the capacitive load of the clock buffers during boosting. In the charge pump design in Fig. 2,

however, we use a control circuit that continuously adjusts the clock frequency of the charge pump depending on the difference between the actual and desired value of the output voltage of the programmable charge pump. Therefore, the charge pump will use its maximum available clock frequency during boosting (approximately 10MHz in this case) which results in a large peak input current. A Spice simulation result of this behavior is shown in Fig. 8 with the normal charge pump boosting under zero-load conditions. The charge pump is the same as was used for sub-pump boosting and consists of 36 stages capable of 55V output voltage, this time 8-bit programmable over the 55V output range. The output voltage ramps up rapidly, displaying an overshoot phenomenon before settling at its programmed value of 55V. The overshoot is inherent to the nature of the control circuit and caused by the reaction speed of the control circuit. More specifically the reaction time is determined by the τ_{RC} time constant resulting from R_{FB} (10 MΩ in this case) combined with gate and strain capacitances in the feedback path in Fig. 2. The overshoot could be reduced by decreasing the value of R_{FB} and increasing the maximum value of I_{prog} in order to maintain the same output voltage range. This would, however, result in more current going to the control circuit and less being available for the actual load of the charge pump. More concerning, however, is the peak input current of 12.6mA during boosting which is unacceptable for some applications. Therefore, extra circuitry was added that controls the boosting mechanism in the charge pump and vastly reduces the peak input current. The idea relies on the dependence of the peak input current during boosting on the used clock frequency and reduces the peak input current by controlling the maximum available clock frequency during boosting. The basic principle is to reduce the clock frequency during boosting to values much lower than the ones needed to support the load current in steady state conditions. This technique requires that the output voltage is allowed to reach the programmed value before any load current is drawn from the output. In other words, the charge pump boosting at reduced clock frequency must be done entirely under zero-load conditions. Afterwards, the charge pump can continue its normal operation and normal load currents can be applied.

While sub-pump boosting requires circuit modifications in the clock lines towards the stage capacitors, the modifications in variable frequency boosting are situated in the clock frequency regulator itself, leaving the circuit from the clock buffers to the stage capacitors intact. The circuit diagram of the modified frequency regulator is shown in Fig. 9.

The feedback voltage V_{FB} (see also Fig. 2) is connected to the insulated gates of PMOS transistors $T_1…T_4$. The currents through T_1 and T_2 are added up and mirrored in T_5 and T_6. Together with the currents provided by T_3 and T_4, they are used to charge and discharge capacitor C_2 using switch S_3. The charging and discharging is controlled by an inverter with hysteresis, which provides the unbuffered clock signal for the charge pump.
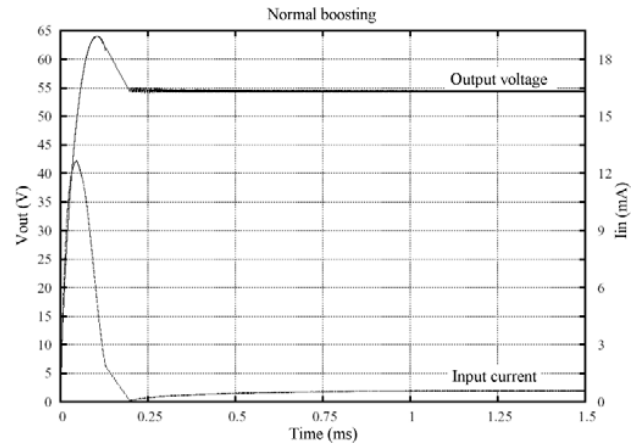

Fig. 8 Output voltage and input current during normal boosting with the control circuit of Fig. 2
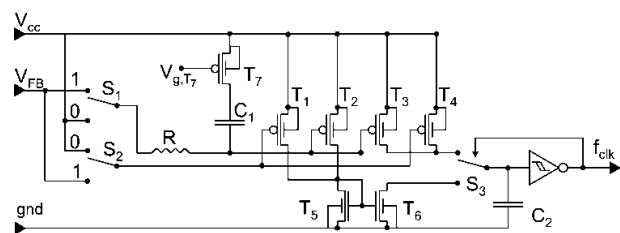

Fig. 9 Frequency regulator for variable frequency boosting

The frequency range can be set by $I_{T1} + I_{T2} = I_{T3} + I_{T4}$ and thus by the W/L ratio of those transistors. In the normal configuration, the pairs (T_1,T_2) and (T_3,T_4) are single transistors. By splitting them in separate transistors with different W/L ratios but the same combined W/L ratio as we would normally have in the case of using 2 instead of 4 PMOS transistors in the frequency regulator, we can control the boosting process and significantly reduce the peak input current. In our design we have $W_{T1} = W_{T4} = 1\mu m$, $W_{T2} = W_{T3} = 7.5\mu m$, $L_{T1} = L_{T4} = 2\mu m$ and $L_{T2} = L_{T3} = 0.7\mu m$.

Initially S_1 and S_2 are in state '0' and $V_{g,T7} = 0V$. The boosting process is started by switching S_2 from '0' to '1' so that $V_{gs,T1} = V_{gs,T4} = V_{FB} - V_{cc}$. This initial boosting process still uses a continuously regulated frequency for the charge pump clock, but the upper frequency limit and therefore the peak input current is drastically reduced. This boosting phase assumes there is no output current drawn from the output, so the output voltage is able to rise to a value close to the programmed value. 1ms after starting the boosting process, S_1 switches from '0' to '1', thus enabling PMOS transistors T_2 and T_3 and therefore extending the upper frequency limit for the clock, which is necessary to allow load currents to be drawn from the charge pump output. The duration of the initial boosting phase is chosen so that the output voltage can come within 90% of its final steady state value when programmed at the maximum output voltage.

Switching on T_2 and T_3 might still generate a considerable peak input current in case the output voltage has not yet reached the programmed value after 1ms of boosting with

reduced frequency range. To eliminate the corresponding peak current, the transient phenomenon resulting from switching on T_2 and T_3 is dampened by the R + C_1 circuit. 0.5ms after T_2 and T_3 were enabled; T_7 is switched off, disabling the τ_{RC1} time constant. At this point, the boosting process is fully completed, allowing the charge pump to respond quicker to changes in load conditions and output voltage.

A circuit simulation result of the output voltage and input current during frequency regulated boosting is shown in Fig. 10. The charge pump is exactly the same as for the results shown in Fig. 8, but now using the frequency regulator shown in Fig. 9.
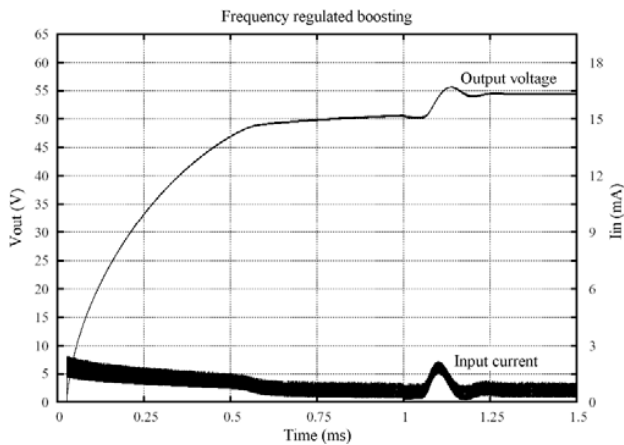

Fig. 10 Output voltage and input current during frequency regulated boosting

Comparison between Figs. 8 and 10 immediately shows the vast reduction in peak input current from 12.6mA for normal boosting to 2mA for frequency regulated boosting. In both cases, the programmable output voltage was set to its maximum value (i.e. all B_i = 1). Both figures also reveal that the overshoot in the output voltage during normal boosting is smoothened by frequency regulated boosting, but the rise time in the latter case is considerably longer.

IV. MEASUREMENTS

The sequential sub-pump boosting and variable frequency charge pump boosting mechanisms were implemented in a bi-stable display driver for smart-card applications, using Dickson charge pumps for the high-voltage generation. The driver chip, shown in Fig. 11, was processed using the 100V 0.7μm I2T100 technology from ON Semiconductor. The display driver contains 2 programmable charge pumps with 36 stages, capable of output voltages up to 55V at a 50μA load current, and 4 programmable charge pumps with 20 stages, capable of output voltages up to 30V at a 50μA load current. These 6 high-voltage generators are clearly identified in the die photograph of Fig 11.

Fig. 12 shows a measurement of the input current during the boosting process of the on-board charge pumps. The charge pumps are boosted one after the other, starting with the 2 biggest pumps followed by the 4 smaller ones, each pump

taking 1.5ms to boost, i.e. 1ms at reduced clock frequency and 0.5ms at increased clock frequency. The output voltage of one big pump was programmed at its maximum value of 55V while the other was set at 40V. The 4 smaller charge pumps were set at 30V, 27.5V, 25V and 15V.
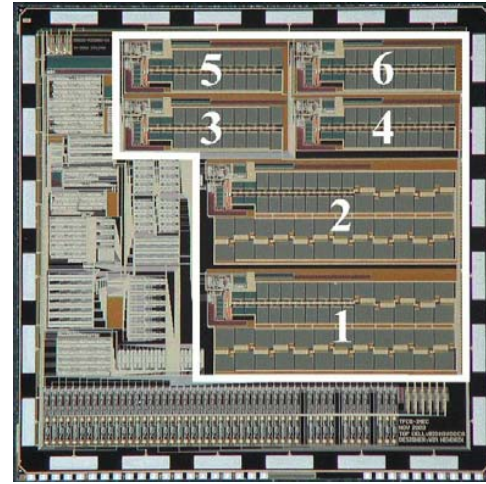

Fig. 11 Die photograph of the prototype display driver chip with 6 integrated charge pumps
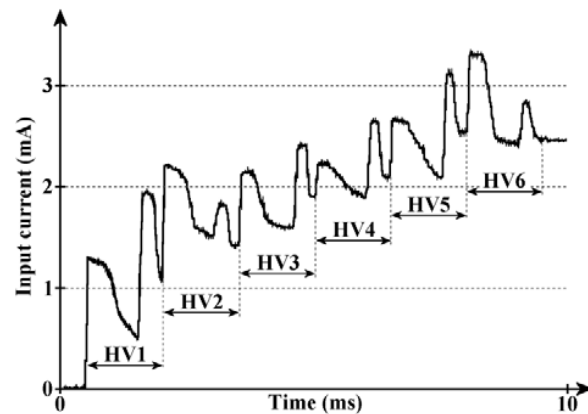

Fig. 12 Measured input current on prototype display driver chip during frequency regulated boosting of the charge pumps

The boosting of the 2 big pumps at 40V and 55V is clearly noticeable in the input current as the biggest spikes at the beginning of the sequence. As expected, the height of the spikes depends on the set output voltage but even in the case of the pump set at 55V, the amplitude of the 2 spikes is not higher than 2mA. This is in good correspondence with the Spice simulation in Fig. 10 and much less than the 12.6mA peak to be expected with normal boosting of the same charge pump. The input current spikes of the 4 smaller charge pumps are somewhat less noticeable, with an amplitude of less than 1mA per pump.

The whole process of boosting the 6 charge pumps is performed with all outputs still unloaded. Once this sequence has completed, all charge pump output voltages have reached their stable values, and these voltages can now be connected to

the display. This is done by means of a high-voltage multiplexer that connects the outputs of the charge pumps in the right order to all display electrodes according to a sophisticated addressing scheme.

V. CONCLUSION

This paper analyses the peak input currents during boosting of Dickson charge pumps, and proposes two methods for reducing those peak currents. Both methods are implemented in the high-voltage generators of a bi-stable display driver chip using the $0.7\mu m$ I2T100 technology from ON Semiconductor. Measurement results show good agreement with Spice simulations, and a reduction of the peak input current by a factor of 6 during boosting is achieved.

REFERENCES

[1] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, 1976, pp. 374-378.

[2] G. Di Cataldo, and G. Palumbo, "Design of an n-th order Dickson voltage multiplier," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 43, no. 5, 1996, pp. 414-417.

[3] G. Palumbo, D. Pappalardo, and M. Giabotti, "Charge-pump circuits: power-consumption optimization," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 11, 2002, pp. 1535-1542.

[4] G. Palumbo, D. Pappalardo, and M. Giabotti, "Modeling and minimization of power consumption in charge pump circuits," *Proc. of the 2001 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2001, pp. 402-405.

[5] C. Lauterbach, W. Weber, and D. Romer, "Charge sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 5, 2000, pp. 719-723.