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Power Integrity Analysis of Power Delivery System in High Speed Digital FPGA Board

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Abstract**—**Power plane noise is the most significant source of signal integrity (SI) issues in a high-speed digital design. In this paper, power integrity (PI) analysis of multiple power planes in a power delivery system of a 12-layer high-speed FPGA board is presented. All 10 power planes of HSD board are analyzed separately by using 3D Electromagnetic based PI solver, then the transient simulation is performed on combined PI data of all planes along with voltage regulator modules (VRMs) and 70 current drawing chips to get the board level power noise coupling on different high-speed signals. De-coupling capacitors are placed between power planes and ground to reduce power noise coupling with signals.

Keywords**—**Channel simulation, electromagnetic simulation, power-aware signal integrity analysis, power integrity, PIPro.

I. Introduction

AS the speed of the data signal increases, many reasons including power supply noise lead to the degradation of the high-speed signals. In low power high-speed digital interfaces, it is crucial to characterize the whole system power supply in order to minimize power supply noise in the system [1]. High-speed design failures show up as failures at higher operating frequency, data error rates, cross talk errors, and EMI errors [2]. The debugging of high-speed related errors may need expensive instruments, e.g. high bandwidth oscilloscope, spectrum analyzers, time domain reflectometer, to detect and understand the failure mechanism [3]. Currently, PI engineers do PI analysis of power system to ensure proper and reliable operation using Electronic Design Automation tools (EDA) before the actual fabrication of board. This reduces board failure chances significantly and also cuts production time.

SI and PI are two distinct but related realms of analysis concerned with the proper operation of digital circuits. In SI, the main concern is to make sure that transmitted 1s looks like 1s at the receiver (and same for the 0s). In PI [4], the main concern is to ensure that the drivers and receivers are provided with adequate current to send and receive 1s and 0s. SI and PI analyzes concerned with the proper analog operation of digital circuits, therefore; care must be taken at the design stage itself to ensure that the design is in accordance with high-speed design rules.

II. Power Delivery System

Different aspects of a Power Delivery Network (PDN) are studied in numerous publications [5]. The main focus of this work was to find out the PDN complex impedance Z(f) of the complete power system that defines, together with chip current waveform, the voltage variations on-chip power rails. For calculations of the voltage variations inside PDN, the next equations are commonly used in frequency domain:

$$\Delta V_{PDN}(f) = Z_{PDN}(f) \times \Delta I(f)$$

Power distribution system of FPGA board is shown in Fig. 1. In this board, there are total 10 power planes and VRMs that supply currents to 70 chips mounted on the board.

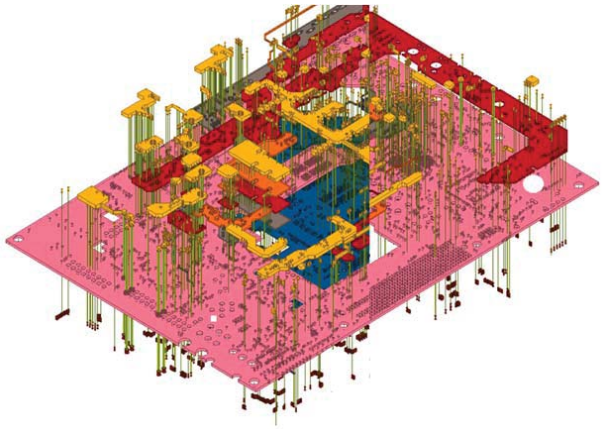

Fig. 1 Layout diagram of complete PND, VRMs, and ICs of HSD Board

The power networks are distributed across 10 layers in high speed digital board. The PDN will act not only as a means of delivering current to ICs, but also as a return current path for signals. A great deal of the crossovers between signals and PI occurs at vias, and for a single-ended signal passing through a via, it is the PDN that acts as the return current path for that signal.

III. PI Analysis

In the PI analysis, energy is distributed through transmission planes that make the analysis more complex than basic SI, since energy is moving in x and y directions, as opposed to just one direction down the transmission line. The PI performance of power distribution networks (PDNs) is evaluated using SIPro/PIPro simulation tool. Two analyzes below are carried out on complete power system.

- PI DC (PI-DC) Analysis
- PI AC (PI-AC) Analysis

The workflow of PI analysis is shown in Fig. 2.

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A. DC Simulation

PI-DC analysis computes the voltage, IR drop (voltage drop), current, and power loss density in the power supply nets. Using this analysis, it is identified how much current is drawn by IC and connector pins or stitching vias at DC operating conditions. Due to excessive voltage drop, the power supply voltage at the IC might fall below the recommended minimum voltage. This can cause malfunctioning of the IC.

Excessive current density in the perforated power supply rails can generate excessive heat, which might lead to board failures due to delamination or fusing. Also, excessive current in the stitching vias can lead to failures losing connection. Any number of power supply nets with source and sink models can be simulated together. The simulated DC IR drop result of 1.8 V VCAUX power plane is shown in Fig. 3. The maximum voltage from VRM to sink (ICs) is 60 mV. Similarly, all PDNs are simulated to get the max voltage drop in power plane as listed in Table I.

TABLE I
MAX VOLTAGE DROP IN ALL POWER PLANES

Sr. No	Power Plane	VRM Voltage	Max Voltage Drop
1	VCINT Regulator	1.0 V	0.98 V
2	SYS_1V0 Regulator	0.95 V	0.92 V
3	VCBRAM Regulator	5.0 V	4.80 V
4	MGTVT Regulator	1.0 V	0.96 V
5	VADJ_1V8 Regulator	1.8 V	1.73 V
6	VC1V2 Regulator	1.2 V	1.14 V
7	MGAVC Regulator	0.9 V	0.87 V
8	VCAUX	1.8 V	1.72 V
9	UTIL_3V3 Regulator	1.0 V	0.95 V
10	VC1V8 Regulator	1.8 V	1.71 V

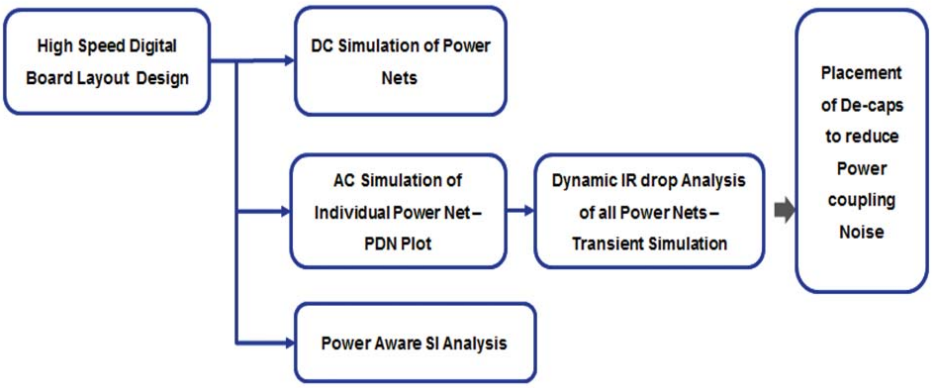


Fig. 2 Workflow of PI analysis

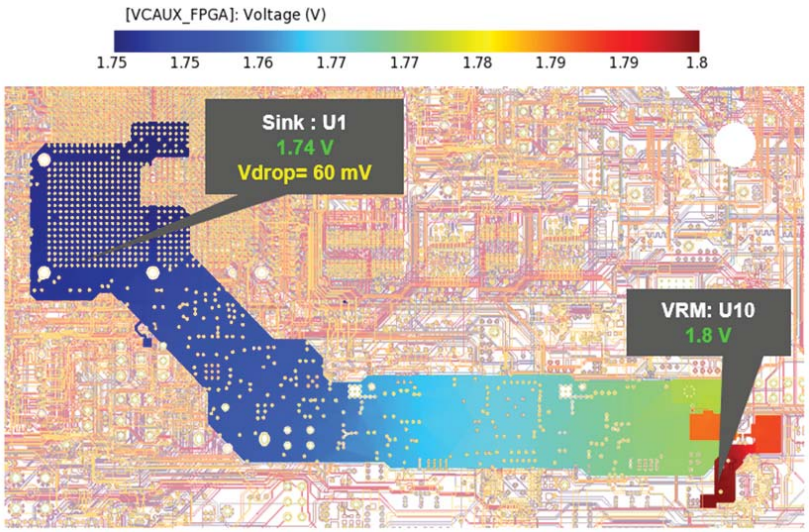


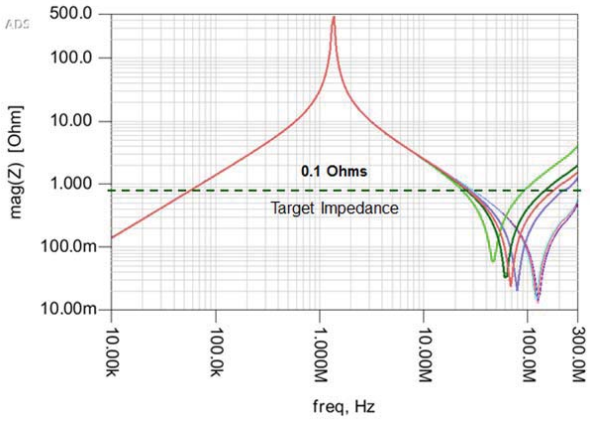
Fig. 3 DC simulation Result of VCAUX 1.8V Power Plane showing voltage distribution on power plane

B. AC Simulation

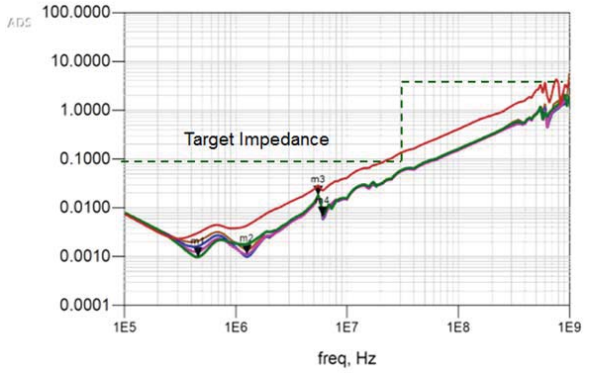
At DC, modeling is relatively simple so that the series resistance of traces, plane shapes, and vias need to be calculated. But, for high frequencies, analyzing the impedance between power and ground at various locations on the PDN requires complex calculations. PI-AC analysis computes the impedance for the IC current loads over a broad frequency

range. It helps to identify whether the PDN provides a low impedance path from the VRM to the IC. AC analysis is carried out to find out the PDN impedance seen from the IC. The VRMs provides 0.9 V to 5 V, the IC pulls 0.1 to 6 A, and a 5% tolerance on the supply voltage is allowed up to around 300 MHz.

The result and target impedance is shown for VCAUX power plane in Fig. 4. Target impedance 0.1 Ω is the green line. At higher frequency, the target impedance specification is more relaxed and rises with frequency. Excessive impedance in a certain frequency range can generate excessive voltage noise, which is also called dynamic IR drop, when the IC power supply pins draw large amounts of transient current required for I/O or core logic switching at rates that fall into that frequency range.



(a)



(b)

Fig. 4 PND impedance profile of 1.8V VCAUX power plane (a) without de-caps (b) with de-caps

The target impedance is not met above 10 kHz and this will produce voltage ripples. The voltage ripple can be reduced by placing decoupling capacitors. Decoupling capacitors can be mounted near the VRM and ICs. It is difficult to get de-caps quantity only by experience. AC simulation gets an effective power solution by iterating capacitor quantity and distribution. After placing seven decoupling capacitors, the result of target impedance 0.1 Ω is achieved.

IV.PI of Power Delivery System

As shown in Fig. 5, electromagnetic (EM) extracted model of 10 PDNs are combined for transient simulation to know PDN profile of 70 ICs in this HSD board.

The simulated impedance profiles of complete PDN and individual power planes are shown in Fig. 6. After pacing de-caps, PDN impedance is below target impedance.

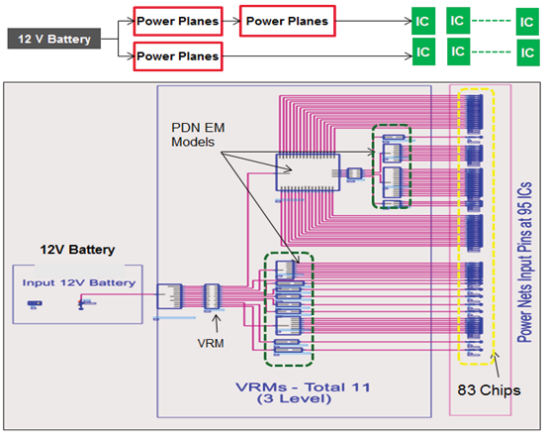
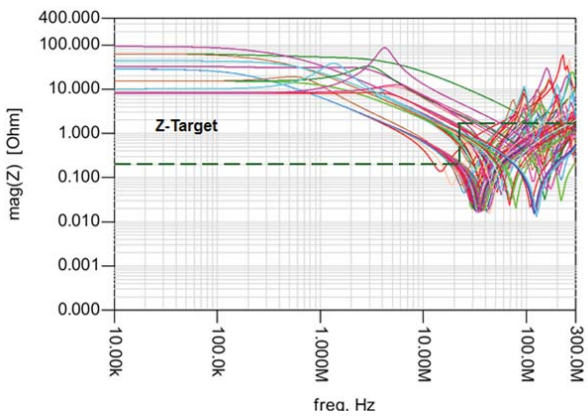


Fig. 5 Schematic diagram of transient simulation setup of complete power system using electromagnetic simulation model of PDNs

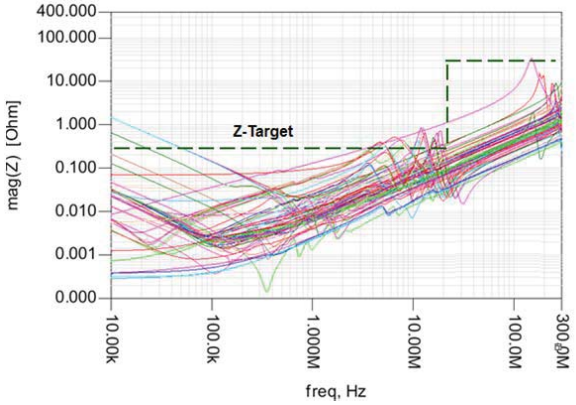
V. Dynamic IR Drop Simulation and Result

Since VRMs switch at kHz frequencies as compared to HSD chips, which switch at multi-gigahertz frequencies, the VRMs are unable to respond to the transient current surges. In addition, the physical separation between the VRM and the chip increases the time delay for the charge to reach the switching circuits within the available time window. Due to the finite inductance of the interconnections, the difficulty of the VRM to respond quickly to current surges leads to a loss of voltage regulation causing the voltage at the transistor terminals to vary wildly with time. Since transistors operate well within an allowed ripple around the dc level of the power supply, a voltage surge above the maximum voltage will limit chip reliability, while a voltage drop below the minimum voltage can lead to reduced operating frequency.

Transient simulation is carried out to know maximum voltage ripples (Dynamic IR drop) of PDN system. As shown in Fig. 7 (a), without any decoupling capacitor voltage ripples, they are very high and it is not within allowed 5% voltage ripple margin. This will cause significant power plane coupling noise to high-speed signals. To reduce the impedance at one of the anti-resonance points, decoupling capacitors with its SRF close to the anti-resonance point are placed. 224 decoupling capacitors are placed between different power and ground planes to reduce this coupling noise and voltage ripple as this can be seen in Fig. 7 (b).

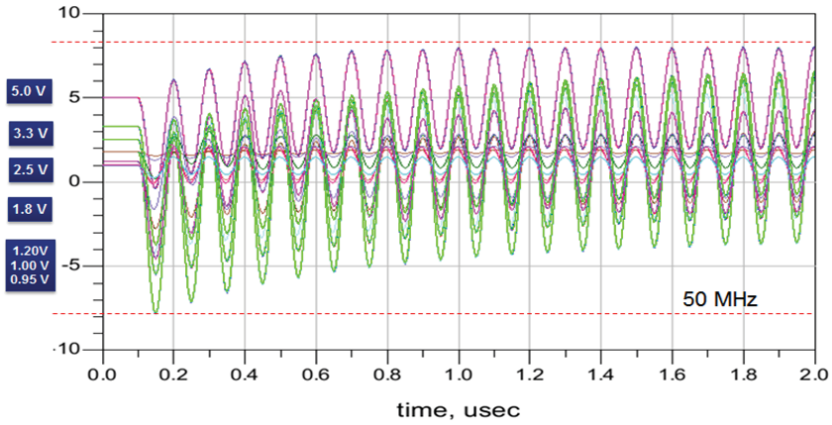


(a)

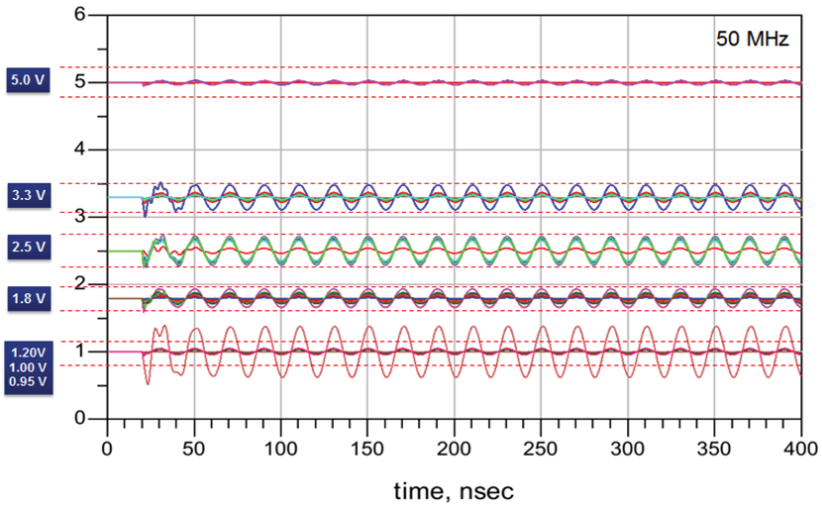


(b)

Fig. 6 (a) Impedance profile of complete PDN without placing de-caps (b) Impedance profile of complete PDN after placing de-caps



(a)



(b)

Fig. 7 (a) Dynamic IR drop (Transient simulation) of all power planes without any decoupling capacitor (b) Dynamic IR drop of all power planes after placing 224 decoupling capacitors between power plane and ground

VI. Conclusion

In this work, complete PDN of a 12-layer, high-speed FPGA board is analyzed to find out the impact of power plane noise on signal nets. DC and AC simulation are performed in SIPro/PIPro to know the maximum voltage drop and voltage ripples, and based on analysis result, 224 decoupling capacitors are placed between power and ground planes to reduce the power plane coupling noise.

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