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Modeling and Simulation of PSM DC-DC Buck Converter

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Abstract—A DC-to-DC converter for applications involving a source with widely varying voltage conditions with loads requiring constant voltage from full load down to no load is presented. The switching regulator considered is a Buck converter with Pulse Skipping Modulation control whereby pulses applied to the switch are blocked or released on output voltage crossing a predetermined value. Results of the study on the performance of regulator circuit are presented. The regulator regulates over a wide input voltage range with slightly higher ripple content and good transient response. Input current spectrum indicates a good EMI performance with crowding of components at low frequency range.

Keywords—DC/DC Converter, Pulse Skipping Modulation, Buck regulator, Modulation Factor, Electromagnetic Interference

I. INTRODUCTION

APPLICATIONS requiring regulated direct current (DC) voltages are mostly supplied from an available voltage source having a higher voltage value, regulated or unregulated. It may be required to maintain, the voltage supplied to the load, constant from no load to full load. DC-to-DC buck converters are direct converters employed for stepping down DC voltage to a desired lower level. These are employed, due to their inherent high efficiency, in places where losses due to their linear counterparts are not tolerated. A buck regulator is a suitably controlled buck converter that can maintain its output voltage at the desired level during constant load with varying input voltage conditions, constant input voltage with varying load conditions or both. A voltage mode PWM controller, in which the duty cycle is altered, based on error between set voltage and measured output voltage such that the output voltage of the converter is very nearly equal to the desired value is well documented and widely used [1] - [4]. These converters are mostly based on circuits in which a pulse width modulated (PWM) signal is filtered with an LC network [5]-[7]. Apart from maintaining the line and load regulations low, it is also desirable to retain the losses low especially in applications involving energy limited sources. It is required that the efficiency is kept high throughout the operating range. Efficiency of PWM switching regulators is in general high compared to linear regulators but not constant over the entire load range. Efficiency of a PWM regulator at light loads is significantly less compared to that at near full load conditions. The problem is pronounced at low voltage portable applications. Various topologies and methods of control were suggested and synchronous buck topology with ZVS technique is suggested for minimizing switching losses [8] - [10]. The low side MOSFET device with integrated Schottky diode can further improve the efficiency of synchronous converter even though there is slight increase in ON resistance [11]. The converter, which operates with high efficiency at light loads during stand by mode, in which portable equipment operate most of the time when not in use, demanded considerable attention of the researchers and several techniques including improved controllers with digital PWM, PFM with reduced switching and conduction losses were proposed [12] - [14]. Pulse Skipping Modulated Converters operate with higher efficiency at light loads with reduced switching loss due to pulse skipping [15]. A pulse skipping modulated dc-dc converter is studied in this paper for its performance under varied supply and load conditions.

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II. PULSE SKIPPING MODULATED BUCK CONVERTER

A. Description

A pulse skipping modulated buck converter is shown in Fig.1. It essentially consists of a MOSFET switch, a diode, an inductor L, a capacitor C. L and C filter out the ripple and designed suitably so that the LC filter cut off frequency is well below the switching frequency. The feedback circuit consists of a PSM control logic, which allows the pulse generated by the clock if actual voltage is below the reference voltage and skips pulses if the actual voltage exceeds the reference voltage vref. The clock pulse generated is a constant frequency constant width (CFCW) pulse . MOSFET switch is ON when

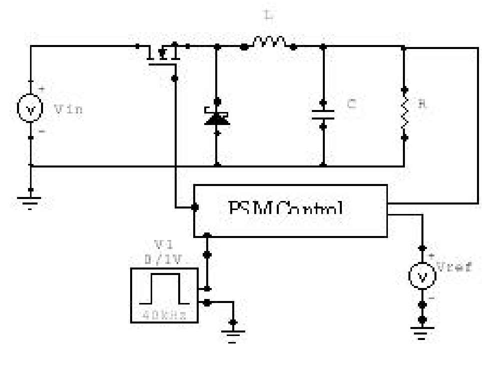

Fig. 1. Pulse Skipping Modulated Buck Converter

the clock pulse is applied over a fixed duration of time equal to duty cycle of the clock and the inductor current rises linearly. The switch is OFF for the remaining period of the cycle and the current drops to a lower value but higher than the initial

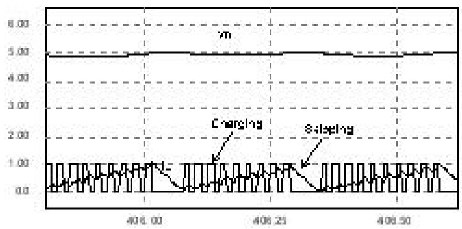

Fig. 2. Waveforms of output voltage, Inductor current and gate pulses for a PSM converter

value of the cycle. It drops to a value lower than the initial value if the next pulse is skipped and so on. Thus by alternately permitting p pulses and skipping q pulses the output voltage is maintained at a value close to reference value. The waveforms are shown in Fig.2.

III. PSM Control Logic

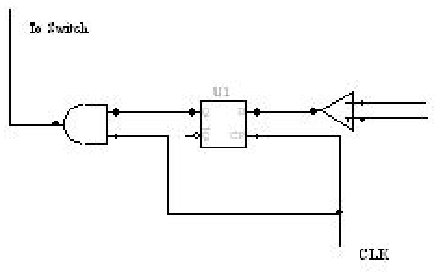

Fig. 3. PSM Control Logic

As shown in Fig 3 a comparator compares v_0 and v_{ref} and its output is given as D input to a D flip flop. Q output of D flip flop is ANDed with CLK and the AND gate output is applied to the MOSFET switch. On $v_{ref} > v_0$ comparator output is HIGH and D is HIGH which will also be the output of the flip flop as long as D is high throughout the clock cycle. This makes the output of AND gate equal the CLK and hence clock cycles are applied to the switch. This is known as charging period. On $v_{ref} < v_0$ comparator output is LOW and D flip flop output goes LOW at the rising edge of the CLK. This makes Q output of the flip flop turn LOW and hence the AND gate output is LOW irrespective of the CLK. The clock pulses are not applied to the switch and are skipped.. This is known as skipping period.

IV. Modeling of PSM Converter

Let for p cycles the clock pulses are applied and for q cycles the pulses are skipped for a particular load resistance R and input voltage V_{in}. The duration pT is known as charging period and the duration qT is known as skipping period.During the charging period, in each cycle the switch is ON for duration equal to DT and during the skipping period the switch is OFF throughout as the pulses are not applied and skipped. The converter is modeled [16] using state space averaging method and the state space equations, assuming continuous conduction mode, are obtained.

During charging period,

$$For \quad 0 \le t \le DT$$

$$\dot{x} = A_1 x + B_1 v_{in} \tag{1}$$

$$y = C_1 x \tag{2}$$

$$For \quad DT \le t \le T$$

$$\dot{x} = A_2 x + B_2 v_{in} \tag{3}$$

$$y = C_2 x \tag{4}$$

During skipping period,

$$For \quad 0 \le t \le T$$

$$\dot{x} = A_2 x + B_2 v_{in} \tag{5}$$

$$y = C_2 x \tag{6}$$

where

$$A_1 = A_2 = A = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix}$$

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix}, \ y = v_0$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}, \ B_2 = 0, \ C = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

After State Space Averaging,

$$\dot{x} = Ax + \frac{p}{p+q} BDv_{in} \tag{7}$$

Defining Modulation Factor M,

$$M = 1 - \frac{f_a}{f}$$

$$\frac{f_a}{f} = \frac{p}{p+q}$$

Where,
f_a - actual frequency of switch
f - Clock Frequency
Therefore

$$\dot{x} = Ax + (1 - M)BDv_{in} \tag{8}$$

M, the modulation factor is a measure of the number of skipping. When v_{in} goes higher for the same V_0 with constant D, M increases increasing the number of skipped pulses to maintain the voltage. Similarly when load decreases M increases decreasing the number of switching. When no pulses are skipped then M is zero and the equation reduces to that of a buck converter at steady state.

V. Simulation

Simulation of the PSM DC-DC buck converter was carried out with the following parameters. $v_{in} = 12V\ to\ 20V, V_0 = 5V, L = 156\mu H, C = 200\mu F, f = 40KHz$. Pulses are

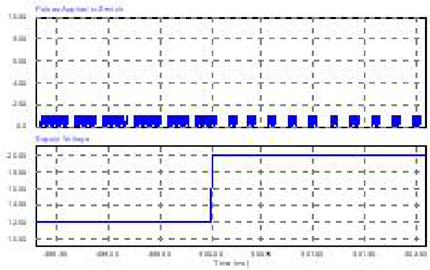

Fig. 4. Increased Pulse Skipping with input voltage increase

skipped to regulate the output voltage with increase in input voltage as shown in Fig 4. Input voltage is stepped from 12V to 20V and the output voltage is plotted. Output voltage waveform for a constant load with a step increase in input voltage is shown in Fig.5. Response showed that PSM

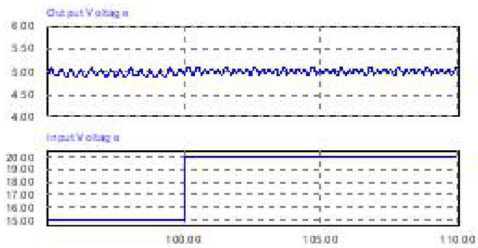

Fig. 5. Output voltage for step increase in input voltage

converter can accept wide variations in input voltage and its response speed was good as seen from step response and the output voltage was regulated over the entire range. Modulation Factor increases with increase in voltage increasing the pulses skipped Load was decreased by a step and the output voltage is shown in Fig.6 Pulses skipped increased, as load was decreased to regulate the voltage. The ripple of the output voltage was higher as input voltage was increased. A similar response was observed when the load was decreased.

Input current harmonic spectrum of the PSM converter is shown in Fig 7. Spectrum of the converter with PWM control is also shown in Fig 8 for comparison purpose for the same input voltage and load.In the case of PSM converter harmonic components are spread over a wide band of frequencies lowering the average value of the peaks of currents. Individual peaks are smaller than those of PWM converter. Hence PSM converter has better EMI performance [16]. Due to reduction in average frequency with pulse skipping at light loads there

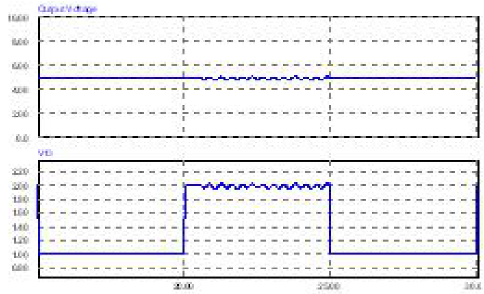

Fig. 6. Output voltage for step decrease in load current

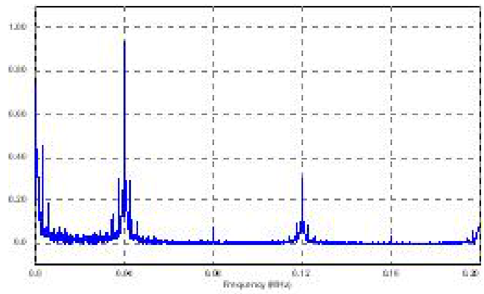

Fig. 7. Input Current Harmonic Spectrum - PSM Converter

may be components entering into audio frequency range which may result in audible noise interference, which can be avoided by selecting the switching frequency suitably.

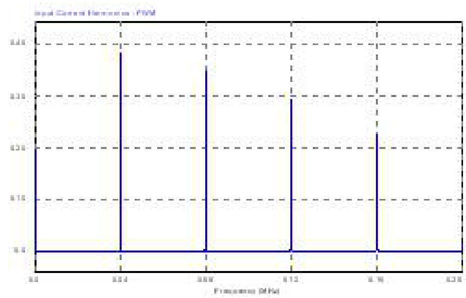

Fig. 8. Input Current Harmonic Spectrum - PWM Converter

VI. Conclusion

Pulse Skipping Modulated Buck converter was modeled and simulated. Response of the converter for input voltage and load step variation was studied. The converter response to changes was quick and the PSM controlled converter regulated the output voltage over the entire range of input voltage intended for operation. Input current harmonic spectrum was studied and compared with that of PWM controlled Converter. PSM converter has a well spread out spectrum, with individual component peak values less in amplitude, making its EMI performance better than that of PWM controlled converter. But there are frequency components entering into audio frequency range due to the average frequency of switching being lower with pulse skipping.

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