

Minimization of Switching Losses in Cascaded Multilevel Inverters Using Efficient Sequential Switching Hybrid-Modulation Techniques

P. Satish Kumar, K. Ramakrishna, Ch. Lokeshwar Reddy, G. Sridhar

Abstract—This paper presents two different sequential switching hybrid-modulation strategies and implemented for cascaded multilevel inverters. Hybrid modulation strategies represent the combinations of Fundamental-frequency pulse width modulation (FFPWM) and Multilevel sinusoidal-modulation (MSPWM) strategies, and are designed for performance of the well-known Alternative Phase opposition disposition (APOD), Phase shifted carrier (PSC). The main characteristics of these modulations are the reduction of switching losses with good harmonic performance, balanced power loss dissipation among the devices with in a cell, and among the series-connected cells. The feasibility of these modulations is verified through spectral analysis, power loss analysis and simulation.

Keywords—Cascaded multilevel inverters, hybrid modulation, power loss analysis, pulse width modulation.

I. INTRODUCTION

THE multilevel inverters are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation [1]. Various multilevel inverter (MLI) structures are reported in the literature, and the cascaded MLI (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI) [2]. The CMLI synthesizes a medium voltage output based on a series connection of power cells that use standard low-voltage component configurations [3].

Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition) or with horizontal

displacements (phase-shifted carrier) [4]. Space-vector modulation (SVM) [5] is also extended for the MLI operation, which offers good harmonic performance [6]. This paper addresses the issue to reduce the switching loss of multilevel sinusoidal-modulation (MSPWM) schemes with low computational overhead. Also, it covers the methodology for equal power dissipation among the power devices, and the power modules. Architecture for Complex Programmable Logic Device (CPLD) implementation with only logical elements is presented adopting sequential switching hybrid-modulation (SSHM) algorithm with PWM circulation. Although only the five-level case is presented here, the proposed method can be equally applied to any number of voltage levels, any number of phases, and switching transitions.

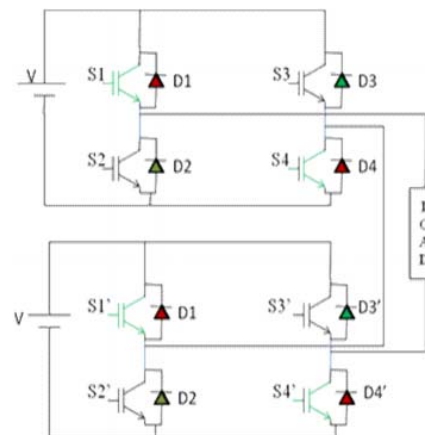


Fig. 1 Schematic diagram of the inverter topology used to verify the proposed hybrid modulations.

II. BASIC ANALYSIS OF MSPWM TECHNIQUES

Unipolar carrier-based N-level PWM operation consists of $(N - 1)/2$ different carriers, same as the number of full bridge inverter cells ($K = (N - 1)/2$). The carriers have the same frequency f_c , the same peak-to-peak amplitude A_c , and are disposed. The modulation index for multiple sinusoidal pulse width modulation is defined as $m = A_m / K A_c$. The modulation frequency ratio is given as $m_f = f_c / f_o$, where f_o is fundamental frequency. For APOD, all carriers are phase opposition by 180° from its adjacent carrier.

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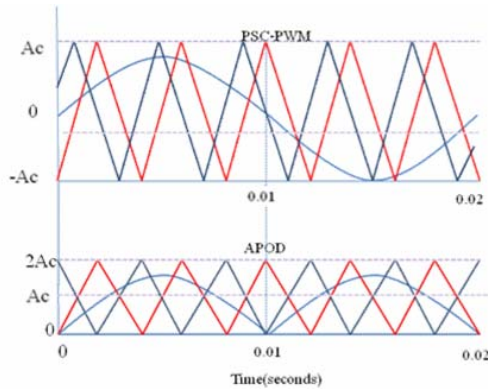


Fig. 2 Sinusoidal reference and carriers of MSPWM operation

The PSC modulation is to retain sinusoidal reference waveforms for the two phase legs of each FBI that are phase shifted by 180° and to then phase shift the carriers of each bridge to achieve additional harmonic side band cancellation around the even carrier multiple groups.

III. PROPOSED SEQUENTIAL SWITCHING HYBRID MODULATION

A. Basic Principle of Modulation

Hybrid modulation is the combination of FFPWM and MSPWM for each inverter cell operation, so that the output inherits the features of switching-loss reduction from FFPWM, and good harmonic performance from MSPWM. In this modulation technique, the two switches of each inverter cell are operated at two different frequencies; two being commutated at FFPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses, and therefore, differential heating among the power devices [7]. A simple base PWM circulation scheme is also introduced here to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules [8]. Fig. 3 shows the general structure of the proposed SSHM scheme. It consists of modulation base generator, base PWM circulation module, and hybrid-modulation controller (HMC) to generate the new modulation pulses.

B. Base Modulation Design

In this modulation strategy, three base-modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse 'A' is a square-wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM and FFPWM sequentially to equalize the power losses among the devices. The fundamental-frequency pulse width modulation 'B' is a square-wave signal synchronized with the modulation waveform; $B = 1$ during the positive half cycle of the modulation signal, and $B = 0$ during negative half cycle. The

SSP and FFPWM pulses are same for all inverter cells. MSPWMs ('C' or 'D') for each cell, differs depends upon the type of carrier and modulation signals used. The block diagram representation of base modulator design is shown Fig. 4. The APOD modulation pulses for cell-I 'C' is obtained from the comparison between unipolar modulation waveform and carrier, while APOD for cell-II 'D' is generated from the comparison between modulation waveform and carrier with dc bias of $-V_c + 2A_c$. The PSC pulses are based on the comparison of modulation waveform with the corresponding PSC waveform for every cell in a CMLI.

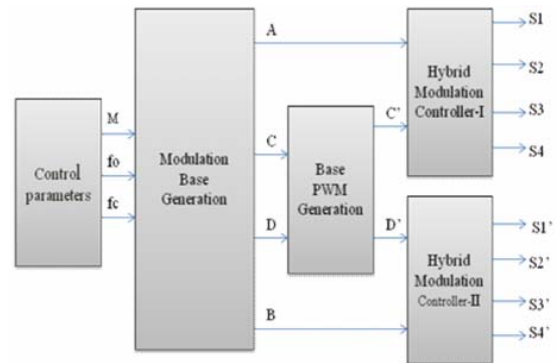


Fig. 3 Scheme of proposed sequential switching hybrid modulation

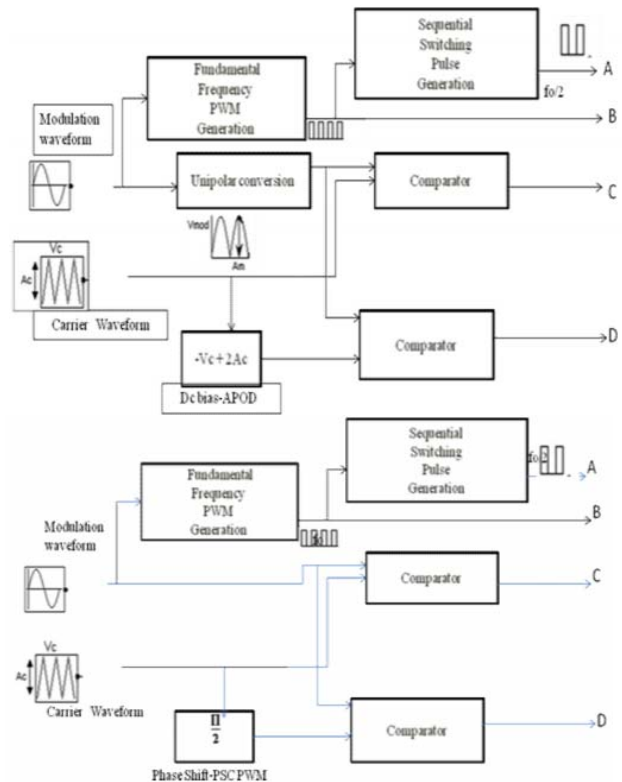


Fig. 4 Block diagram of five-level base modulator for: (a) HAPOD and (b) HPSC Scheme

C. Base PWM Circulation

For long operating-time expectancy, it is important to share the power loss among every module, and furthermore, to every power device in the cell. This is one of the key issues the modulation should cover [9]. A simple base PWM circulation scheme introduced here to get resultant HPWM circulation among the power modules.

The scheme of five-level base PWM circulation is shown in Fig. 5, consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is $f_o/4$, makes the time base for PWM circulation from one module to another [10]. After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module becomes the first appropriate PWM channel. This PWM circulation is based on simple multiplexer logic circuits, which makes the applicability of the algorithm very effective in a CPLD.

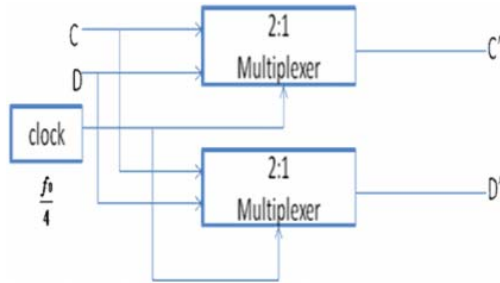


Fig. 5 Scheme of base PWM circulation for five-level

IV. SIMULATION RESULTS AND ANALYSIS

A. Hybrid Modulation Controller

The HMC combines SSP, FPWM and MSPWM that produces SSHM pulses. It is designed by using a simple combinational logic and the functions for a five-level HPWM are expressed as

$$\begin{aligned} S1 &= ABC' + \bar{A}B & S1' &= ABD' + \bar{A}B \\ S2 &= \bar{A}BC + \bar{A}\bar{B} & S2' &= \bar{A}BD' + \bar{A}\bar{B} \\ S3 &= \bar{A}BC' + A\bar{B} & S3' &= \bar{A}BD' + A\bar{B} \\ S4 &= \bar{A}BC' + AB & S4' &= \bar{A}BD' + AB \end{aligned}$$

where A is an SSP, B is an FFPWM, C' is an MSPWM for cell-I and D' is an MSPWM for cell-II. In Fig. 6, it is shown that each gate pulse is composed of both FPWM and MSPWM. If $A = 1$, then $S1, S2, S1',$ and $S2'$ are operated with MSPWM, while $S3, S4, S3',$ and $S4'$ are operated at FFPWM. If $A = 0$, then $S1, S2, S1'$ and $S2'$ are operated at FFPWM, while $S3, S4, S3',$ and $S4'$ are operated with MSPWM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. The voltage stress and current stress of power switches in each cell is inherently equalized with this modulation. After every two fundamental periods, the HPWM pattern is changed so that the first module ($S1, S2, S3,$ and $S4$) becomes the second module ($S1', S2',$

$S3',$ and $S4'$), and the second one shifts to the first, and is shown in Fig. 6. It can be observed from the waveforms of V_{h1} and V_{h2} that the implementation of HPWM circulation makes the inverter modules operate at same average switching frequency with the same conduction period. As a result, all inverter cells operate in a balanced condition with the same power-handling capability and switching losses. As it is concluded from Fig. 6, the resultant inverter switching is same as the type of MSPWM used.

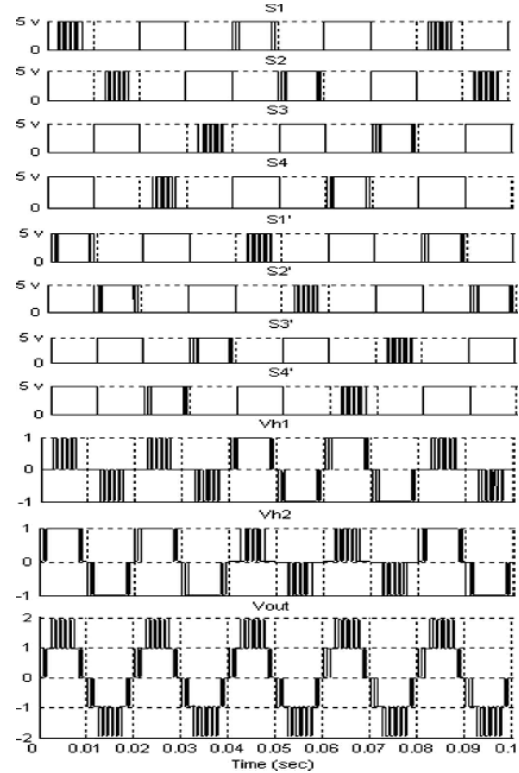


Fig. 6 Five-level sequential switching HAPOD pulses and its output voltage wave form

B. Power loss Analysis

The semiconductor power losses can be estimated from the characteristic curves, which are presented in the datasheets of each power device [11]. Only conduction and switching losses are considered here for power-loss estimation. The insulated gate bipolar transistors (IGBTs) selected are IRG4BC20SD, in which their maximum ratings are a forward current of 19A and a direct voltage of 600V. The carrier frequency f_c is 1.5 kHz and each cell is connected to 100V dc supply.

The characteristics curves are $[V_{sat}(\theta) \times I_l(\theta)]$ and $[E(\theta) \times I_l(\theta)]$, where V_{sat} is the ON-state saturation voltage and $E(\theta)$ represent the energy losses in one commutation and the $E_{ON}(\theta)$ is a turn-ON commutation, $E_{OFF}(\theta)$ is a turn-OFF commutation, and $E_{rec}(\theta)$ is for diode reverse recovery process. The switching losses are generating during the turn-ON and turn- OFF switching processes. The switching loss for every power

device (P_{sw}) is obtained by identifying every turn-ON and turn OFF instants during one reference period as

$$P_{sw} = I/T (E_{ON} + E_{OFF} + E_{rec})$$

The conduction losses are those that occur while the semiconductor device conducts current [12]. It is computed by multiplying the ON- state voltage by ON-state current. The power loss is [13] the sum of switching losses and conduction losses as shown in Fig. 7 (a), for the full range of modulation index and the relative angle of the load currents, the switching-loss ratio of hybrid alternative phase opposition disposition (HAPOD) versus the conventional APOD techniques. It is noted that the surface is always below one, which means that the switching losses are significantly reduced. Fig. 7 (b) shows that the conduction losses are higher. This is because of increased conduction period due to mixing of a FPWM, which is clearly shown in Fig. 6. Lastly, Fig. 7 (c) shows the power-loss ratio between these two methods. Since the switching losses are predominant [14], the power losses of the proposed modulations are less than those conventional one. The mean value of the power-loss ratio surface is 0.718 approximately, which means the power-loss reduction is about 28.2%. The best case is produced for a unity power factor and modulation index as one in which the loss saving is about 31%. Even though the power-loss ratio between HAPOD and its own APOD operations are presented, the other proposed modulations make similar power-loss saving with respect its own modulation techniques. In a practical high-power system, switching losses are higher than conduction losses [15]. Therefore, saving switching losses becomes important to improve the efficiency of the system [16].

C. Spectrum Analysis of Output Voltage Waveform

To evaluate the quality of the output voltage waveforms, the values of total harmonic distortion (THD) and weighted THD (WTHD) are calculated up to 50th order of harmonics, as suggested in the IEEE standard 519.

$$THD = \frac{\sqrt{\sum_{n=2}^{50} V_n^2}}{V_1} \quad \text{and} \quad WTHD = \frac{\sqrt{\sum_{n=2}^{50} \left(\frac{V_n}{n}\right)^2}}{V_1}$$

where V_1 is the rms value of the fundamental component voltage, n is the order of harmonics, and V_n is rms value of the n^{th} harmonic. It is found that the proposed modulations offer lower THD compared to the conventional one, thus the superiority. Furthermore, it is noted that higher the value of modulation index (M), lower the value of THD. Also, WTHD values are lower when the modulation index is closer to unity and when the carrier frequency increases. Throughout its linear modulation range, hybrid phase shifted carrier (HPSC) has the least harmonic distortion among SSHM schemes. In order to show the feasibility of the proposed modulations, the spectral analysis was performed by using MATLAB/Simulink is shown in Fig. 8.

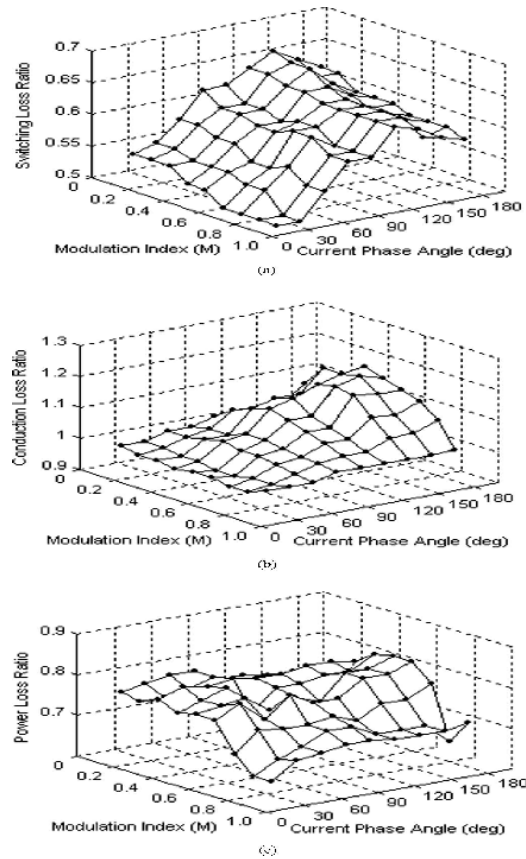


Fig. 7 Loss-ratio analysis of HAPOD and APOD fed five-level inverter. (a) Switching loss. (b) Conduction loss. (c) Power loss

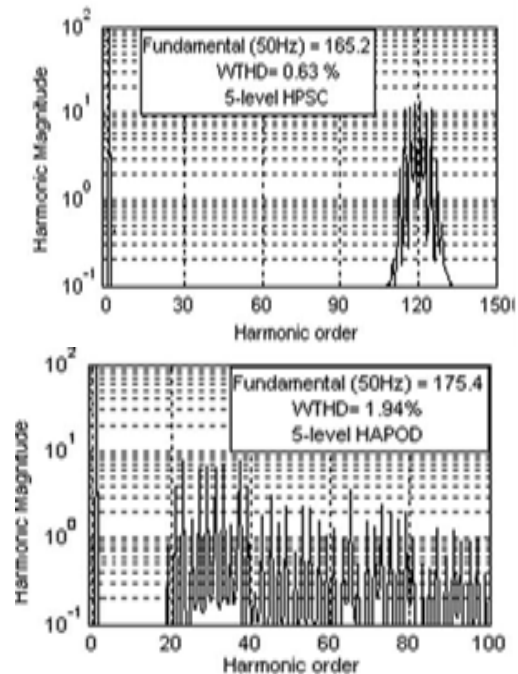


Fig. 8 Harmonic spectrum of the output voltage waveform

The load resistance and inductance are $10\ \Omega$ and 15mH respectively, and the dc-bus voltage is set at 100 V . The frequency of modulated wave and carrier wave are 50Hz and 1500 Hz respectively and the inverter is operated with linear modulation region ($M=0.85$). The harmonic cancellation up to the sidebands around the carrier frequency is achieved in the voltage waveform and the first significant harmonic is the 19^{th} as predicted for HAPOD operation. The lower order harmonics are absent and the fundamental is controlled at the predefined value. This inverter when operated with odd frequency ratio, it produces even sideband harmonics and when operated with even frequency ratio, it produces odd sideband harmonics. Furthermore, harmonics at the carrier and the multiples of carrier frequency do not exist at all. From the voltage spectrum the amplitude of the lower order harmonics is very low and same fundamental value is achieved.

V. CONCLUSIONS

In this paper, a new family of SSHM techniques for CMLI, operating at a lower switching frequency is proposed. The proposed technique is applied to well-known MSPWM schemes APOD and PSC. Compared to conventional MSPWM schemes, less number of commutations and considerable switching-loss reduction is obtained while achieving the same fundamental voltage tracking. The harmonic performance of the SSHM schemes are analyzed in the entire range of modulation index and it seems to be good. An efficient sequential switching and PWM circulation techniques are embedded with these hybrid modulations for balanced power dissipation among the power devices within a cell and for series-connected cells. Combinational logic-based HMC is compact and easily realized with CPLD. These modulations can be easily extended to higher voltage level through the generalization process and implementation possible with existing CMLI Structures. The published simulation results have been good agreement with the proposed work.

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