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Low Power Low Voltage Current Mode Pipelined A/D Converters

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Abstract**—**This paper presents two prototypes of low power low voltage current mode 9 bit pipelined a/d converters. The first and the second converters are configured of 1.5 bit and 2.5 bit stages, respectively. The a/d converter structures are composed of current mode building blocks and final comparator block which converts the analog current signal into digital voltage signal. All building blocks have been designed in CMOS AMS 0.35μm technology, then simulated to verify proposed concept. The performances of both converters are compared to performances of known current mode and voltage mode switched capacitance converter structures. Low power consumption and small chip area are advantages of the proposed converters.

Keywords**—**Pipelined converter; a/d converter; low power; low voltage; current mode.

I. Introduction

A number of high resolution and high speed monolithic pipelined a/d converters have been realized in the past few years [1÷7]. The pipelined structure is very attractive, because it effectively overcomes the limitations of the flash structure. Proposed pipelined a/d converter (ADC) converts the analog current input signal into digital voltage representation. The current mode conversion is used to optimize a power consumption of the circuit. As shown in figure 1, the $M=N*k$ bit pipelined ADC consists of a series of identical k bit stages that are isolated by track and hold (T/H) buffers. Each stage of the N stages pipelined ADC is composed of a track and hold T/H buffer, a k-bit a/d subconverter (SADC), a k-bit d/a subconverter (SDAC), an amplifier with gain coefficient equal 2^k. The use of T/H buffers allow each of the stages to operate concurrently on N samples simultaneously, thus giving very high speed conversion of the pipelined ADC. The first stage operates on the most recent current sample, while the following stages operate on analog remainder currents, called residues from previous samples. In each stage T/H buffer samples and holds the output current from the previous stage. The held input current is converted into k bit digital code and then back to analog by the k-bit SDAC. The k-bit SDAC output current is subtracted from the held input current, and the difference is amplified by 2^k to produce an output residue current that is passed to the next stage. The held signal is passed along from stage to stage until reaches the final stage in the pipelined ADC [1].

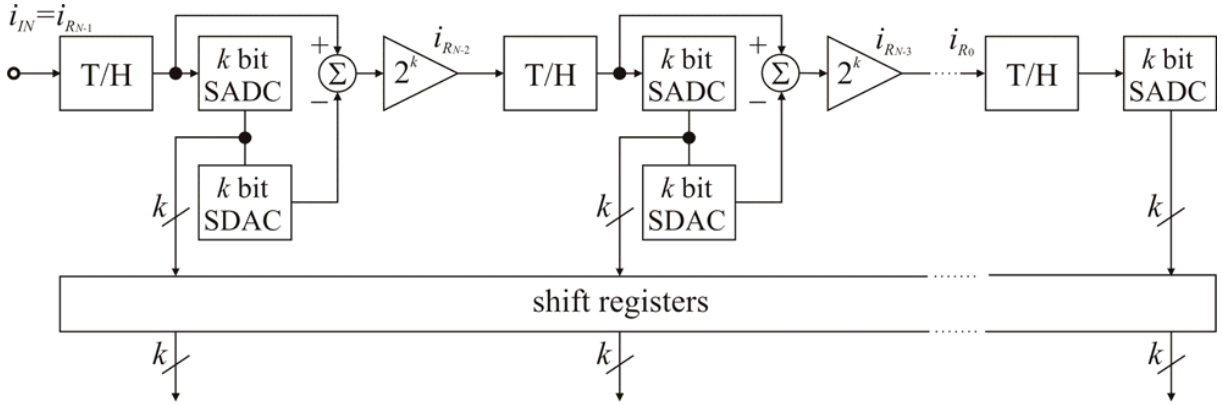

Fig. 1 Basic pipelined $M=N*k$ bit ADC

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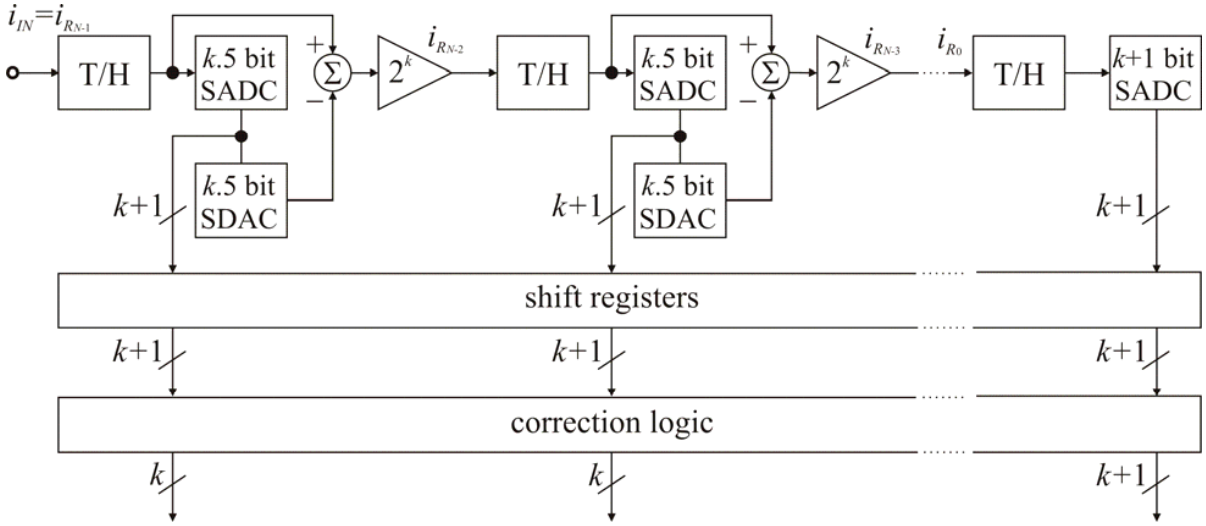

Fig. 2 Basic pipelined $M=N*k+1$ bit ADC with correction logic

The simplest ADC structure is composed of 1-bit SADCs, 1-bit SDACs and amplifiers with gain coefficients equal 2. Unfortunately this structure similarly to general ADC structure shown in figure 1 suffers from comparators offset errors. A digital correction logic is used to eliminate comparators offset as shown in figure 2. The correction structure uses additional comparators in each stage, to add an extra bit in each stage to configure k.5 stages, except of the last k+1 bit stage. The k.5 bit stage is k bit stage into which some redundancy is built to provide a large tolerance for component imperfections. Then the overall voltage output digital data is stored in the appropriate number of shift registers so that the digital data arriving at the correction logic corresponds to the same sample. Finally, the digital data is corrected in a logic correction structure in which a digital correction algorithm eliminates the redundancy. This makes the $M=N*k+1$ bit pipelined ADC almost insensitive to comparators offsets. The simplest structure, in which k=1 [4], is composed of 1.5 bit stages. Each stage of the N stages pipelined ADC is composed of the T/H buffer, a 1.5 bit SADC, a 1.5 bit SDAC, a substracter and an amplifier with gain coefficient equal 2, except of the last stage which is composed of the T/H buffer and the 2 bit SADC, only. The next more complex structure, in which k=2 [5], is built of 2.5 bit stages. Each stage of the N stages pipelined ADC is composed of the T/H buffer, a 2.5 bit SADC, a 2.5 bit SDAC, a substracter and an amplifier with gain coefficient equal 4, except of the last stage which is composed of the T/H buffer and the 3 bit SADC, only.

II. Pipelined 1.5 bit Stages ADC

In each of N-1 1.5 bit stages of the ADC, the residue current is converted by the 1.5 bit SADC into 2 bit 3 states digital code (00, 01 and 10) and then back to analog by the 1.5 bit SDAC. The 1.5 bit SDAC output current is subtracted from the held input current, and the difference is amplified by 2 to produce an output residue current that is passed to the next stage. In the last 2 bit stage, the residue current is converted by the 2 bit SADC into 2 bit 4 states digital code (00, 01, 10, 11).

A. 1.5 bit and 2 bit SADCs

The 1.5 bit current SADC is based on window comparator structure. Each 1.5 bit stage uses two symmetrical comparison current levels $-I_{FS}/4$ and $I_{FS}/4$, where I_{FS} and $-I_{FS}$ denote positive and negative full scale currents, respectively. Choice of current levels is not critical. The operating current range is divided into three subranges and the 1.5 bit SADC output consists of two bits. This is the initial digital output, before code conversion and error correction. The SADC output codes $B_i = b_{i1}b_{i0}$ are:

$$B_i = \begin{cases} 00 & \text{when} \quad i_{R_i} \le \frac{-I_{FS}}{4} \\ 01 & \text{when} \quad \frac{-I_{FS}}{4} \le i_{R_i} \le \frac{I_{FS}}{4} \\ 10 & \text{when} \quad \frac{I_{FS}}{4} \le i_{R_i} \end{cases} \tag{1}$$

$$i = N-1, \ldots, 1$$

where N denote number of stages.

In the last stage, the 2 bit stage uses three symmetrical comparison current levels $-I_{FS}/2$, 0 and $I_{FS}/2$. The SADC output codes $B_0 = b_{01}b_{00}$ are:

$$B_0 = \begin{cases} 00 \text{ when} \quad i_{R_0} \le \frac{-I_{FS}}{2} \\ 01 \text{ when} \quad \frac{-I_{FS}}{2} \le i_{R_0} \le 0 \\ 10 \text{ when} \quad 0 \le i_{R_0} \le \frac{I_{FS}}{2} \\ 11 \text{ when} \quad \frac{I_{FS}}{2} \le i_{R_0} \end{cases} \tag{2}$$

The output codes B_i described by (1) and (2) are the initial digital outputs, before code conversion and error correction.

B. 1.5 bit SDAC

The 1.5 bit SDAC structure is used to generate reference currents $-I_{FS}/2$, 0 and $I_{FS}/2$. So, the 1.5 bit SDAC current outputs are $-I_{FS}/2$, 0, $I_{FS}/2$ for the input codes 00, 01 and 10, respectively.

C. Current multiply by two circuit

In each stage, the 1.5 bit SDAC output current is subtracted from the residue current of the previous stage, and the difference is multiplied by 2 to produce a residue current that is passed to the next stage This residue current is expressed as follows.

$$i_{R_{i-1}} = \begin{cases} 2i_{R_i} + I_{FS} & \text{for} \quad B_i = 00 \\ 2i_{R_i} & \text{for} \quad B_i = 01 \\ 2i_{R_i} - I_{FS} & \text{for} \quad B_i = 10 \end{cases} \quad (3)$$

$$i = N-2, \dots, 0$$

III. Pipelined 1.5 bit Stages A/D Converter

In each of *N*-1 2.5 bit stages of the ADC, the residue current is converted by the 2.5 bit SADC into 3 bit 7 states digital code (000, 001, 010, 011, 100, 101 and 110) and then back to analog by the 2.5 bit SDAC. The 2.5 bit SDAC output current is subtracted from the held input current, and the difference is amplified by 4 to produce an output residue current that is passed to the next stage. In the last 3 bit stage, the residue current is converted by the 3 bit SADC into 3 bit 8 states digital code (000, 001, 010, 011, 100, 101, 110 and 111).

A. 2.5 bit and 3 bit SADCs

The 2.5 bit current SADC is based on comparator structure. Each 2.5 bit stage uses six symmetrical comparison current levels $-5I_{FS}/8$, $-3I_{FS}/8$, $-I_{FS}/8$, $I_{FS}/8$, $3I_{FS}/8$ and $5I_{FS}/8$, where I_{FS} and $-I_{FS}$ are positive and negative full scale currents, respectively. Choice of current levels is not critical. The operating current range is divided into seven subranges and the 2.5 bit SADC output consists of three bits, depending on the input residue currents. The SADC output codes $B_i = b_{i2}b_{i1}b_{i0}$ are:

$$B_i = \begin{cases} 000 & \text{when} \quad i_{R_i} \le \frac{-5I_{FS}}{8} \\ 001 & \text{when} \quad \frac{-5I_{FS}}{8} \le i_{R_i} \le \frac{-3I_{FS}}{8} \\ 010 & \text{when} \quad \frac{-3I_{FS}}{8} \le i_{R_i} \le \frac{-I_{FS}}{8} \\ 011 & \text{when} \quad \frac{-I_{FS}}{8} \le i_{R_i} \le \frac{I_{FS}}{8} \\ 100 & \text{when} \quad \frac{I_{FS}}{8} \le i_{R_i} \le \frac{3I_{FS}}{8} \\ 101 & \text{when} \quad \frac{3I_{FS}}{8} \le i_{R_i} \le \frac{5I_{FS}}{8} \\ 110 & \text{when} \quad \frac{5I_{FS}}{8} \le i_{R_i} \end{cases} \quad (4)$$

$$i = N-1, \dots, 1$$

where *N* denote number of stages.

In the last stage, the 3 bit stage uses seven symmetrical comparison current levels $-3I_{FS}/4$, $-I_{FS}/2$, $-I_{FS}/4$, 0, $I_{FS}/4$, $I_{FS}/2$ and $3I_{FS}/4$. The SADC output codes $B_0 = b_{02}b_{01}b_{00}$ are:

$$B_0 = \begin{cases} 000 & \text{when} \quad i_{R_0} \le \frac{-3I_{FS}}{4} \\ 001 & \text{when} \quad \frac{-3I_{FS}}{4} \le i_{R_0} \le \frac{-I_{FS}}{2} \\ 010 & \text{when} \quad \frac{-I_{FS}}{2} \le i_{R_0} \le \frac{-I_{FS}}{4} \\ 011 & \text{when} \quad \frac{-I_{FS}}{4} \le i_{R_0} \le 0 \\ 100 & \text{when} \quad 0 \le i_{R_0} \le \frac{I_{FS}}{4} \\ 101 & \text{when} \quad \frac{I_{FS}}{4} \le i_{R_0} \le \frac{3I_{FS}}{2} \\ 110 & \text{when} \quad \frac{I_{FS}}{2} \le i_{R_0} \le \frac{3I_{FS}}{4} \\ 111 & \text{when} \quad \frac{3I_{FS}}{4} \le i_{R_0} \end{cases} \quad (5)$$

The output codes B_i described by (4) and (5) are the initial digital outputs, before code conversion and error correction.

B. 2.5 bit SDAC

The 2.5 bit SDAC structure is used to generate reference currents $-3I_{FS}/4$, $-I_{FS}/2$, $-I_{FS}/4$, 0, $I_{FS}/4$, $I_{FS}/2$ and $3I_{FS}/4$. So, the 2.5 bit SDAC current outputs are $-3I_{FS}/4$, $-I_{FS}/2$, $-I_{FS}/4$, 0, $I_{FS}/4$, $I_{FS}/2$ and $3I_{FS}/4$ for the input codes 000, 001, 010, 011, 100, 101 and 110, respectively.

C. Current multiply by four circuit

In each stage, the 2.5 bit SDAC output current is subtracted from the previous stage residue current, and the difference is multiplied by 4 to produce a residue current that is passed to the next stage This residue current is expressed as follows

$$i_{R_{i-1}} = \begin{cases} 4i_{R_i} + 3I_{FS} & \text{for} \quad B_i = 000 \\ 4i_{R_i} + 2I_{FS} & \text{for} \quad B_i = 001 \\ 4i_{R_i} + I_{FS} & \text{for} \quad B_i = 010 \\ 4i_{R_i} & \text{for} \quad B_i = 011 \\ 4i_{R_i} - I_{FS} & \text{for} \quad B_i = 100 \\ 4i_{R_i} - 2I_{FS} & \text{for} \quad B_i = 101 \\ 4i_{R_i} - 3I_{FS} & \text{for} \quad B_i = 110 \end{cases} \quad (6)$$

$$i = N-1, \dots, 1$$

IV. Correction Logic

The correction logic is presented for the case of 1.5 bit stages pipelined ADC. An analogous procedure is applied to any *k*.5 bit stages pipelined ADC. Unfortunately, 1 bit pipelined architecture is sensitive to comparator offset. Offset errors in i^{th} stage SADC resulting in missing codes are shown on the plot in figure 3. An error correction can be added to the simple 1 bit stage by adding single extra comparator in each stage resulting in 1.5 bit stage except of last in which two extra comparators are added resulting in 2 bit stage.

Each 1.5 bit stage produces a 2 bit code. The digital outputs $B_i = b_{i1}b_{i0}$ of all stages in the pipeline must be stored in the appropriate number of shift registers so that the digital data arriving at the correction logic corresponds to the same sample.

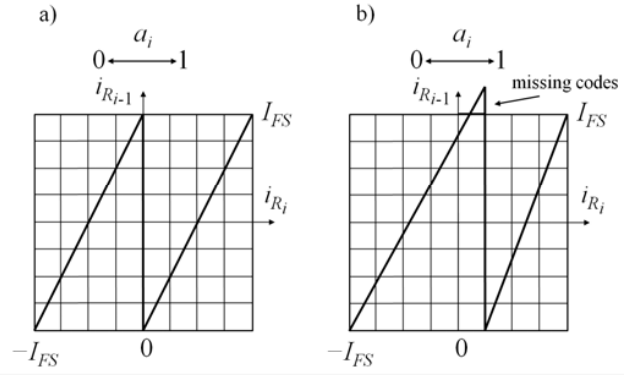

Fig. 3 Residue waveforms for 1 bit per stage converter
a) ideal i^{th} stage, b)offset error in the i^{th} stage.

Once the error correction algorithm is applied, 2 bit per stage code is reduced to the final one bit per stage code. Even in absence any errors at all, the two bit per stage code must be converted to 1 bit per stage. The correction logic structure is shown in figure 4. To generate the final error corrected N bit output code from the 2 bit codes, the two digital outputs from each adjacent stages are added together with 1 bit overlapped between adjacent stages as follows

$B_{N-1}=\quad b_{N-1\,1}\ b_{N-1\,0}$

$\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots$

$B_2=\quad b_{21}\ b_{20}$

$B_1=\quad b_{11}\ b_{10}$

$B_0=\quad b_{01}\ b_{00}$

$A=\quad a_{M-1}\ \ \ldots\ \ a_3\ a_2\ a_1\ a_0$

The correction procedure is illustrated on the last 2 stages: 1.5 bit and 2 bit stages, respectively. The procedure to determine codes in two different ranges with no offset error is illustrated in figure 5. The codes for those ranges are 010 and 101. The procedure to determine codes in two different ranges for error offset is illustrated in figure 6. The codes for those ranges still are 010 and 101.

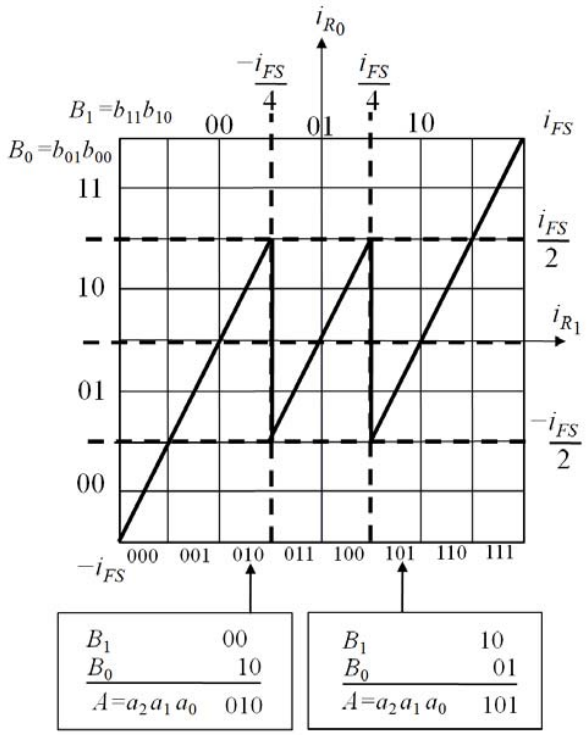

Fig. 5 Procedure to determine digital codes with no offset error.

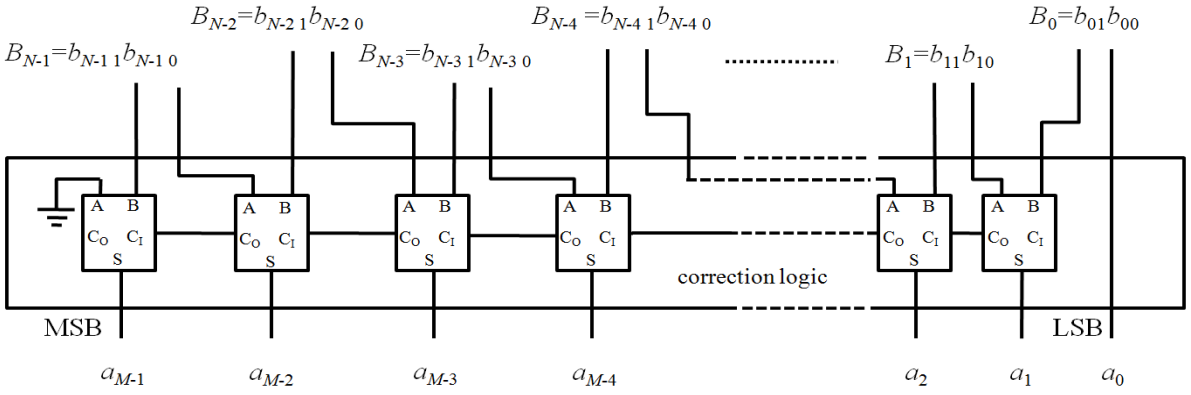

Fig. 4 Correction logic structure

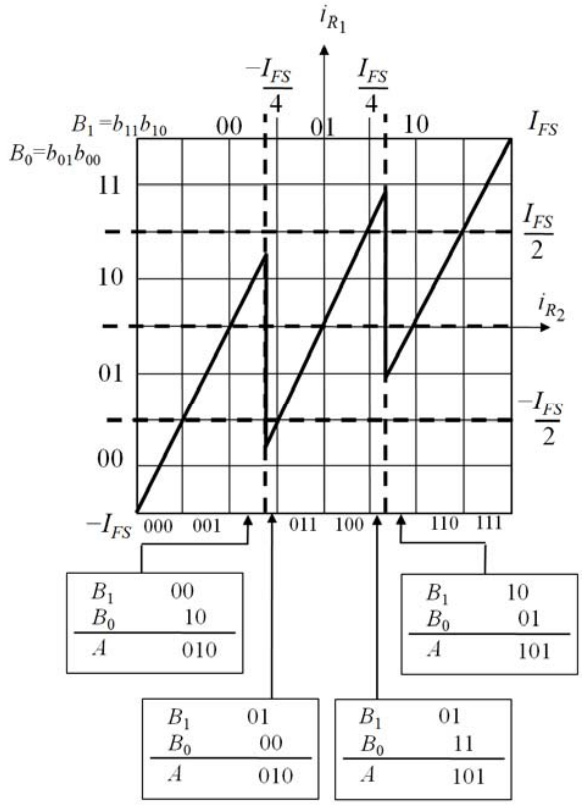

Fig. 6 Procedure to determine digital codes with offset error correction.

V. Experimental Results And Concluding Remarks

To verify proposed two current mode pipelined ADC structures, the ASIC experimental circuit shown in figure 7 have been designed. The circuit contains plenty of current mode building blocks to configure 1.5 bit and 2.5 bit stages converters. All building blocks have been designed in CMOS AMS 0.35µm technology simulated, fabricated and measured. Those building blocks have been used to configure two 9 bit resolution prototype pipelined ADCs composed of 8 1.5 bit stages and 4 2.5 bit stages, respectively. Performances of both ADCs have been measured and compared to performances of ADC structures known in literature [2, 3, 6, 7]. The static linearity of the ADC have been measured using a low-frequency (10 kHz) tone and analyzing over 10^5 output codes. The code density have been used to determine maximum differential nonlinearity (DNL) and maximum integral nonlinearity (INL) errors. The dynamic linearity of ADC has been measured by analyzing a Fast Fourier Transform of the output codes for a single input tone at Nyquist rate. The FFT of the ADC output has been used to determine a peak signal-to-noise-and-distortion ratio (SNDR) at Nyquist rate. Measured performances of both ADCs are summarized in Table 1 in the 2nd and 3rd columns, respectively. Performances of both ADCs are very similar. The differences result in lower power consumption and chip area of 1.5 stages ADCs, only.

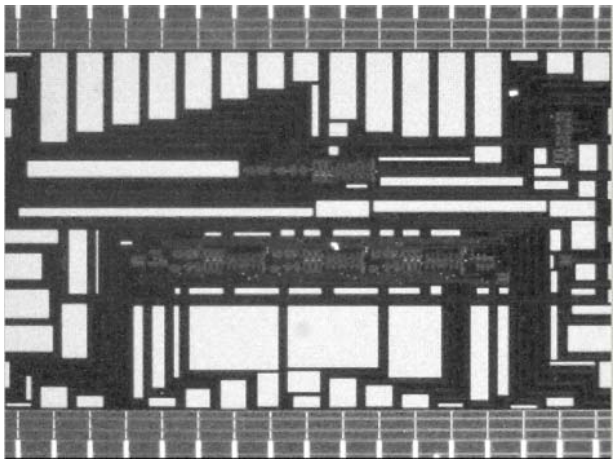

Fig. 7 The die-photo of experimental circuit in 0.35µm technology.

TABLE I
Comparison of Performances of Proposed SI and Known SC ADCs

Performances	presented 1.5 bit stages	presented 2.5 bit stages	[2] 1.5 bit stages	[3] 2.5 bit stages
Technology	0.35µm	0.35µm	0.8µm	1.0µm
Resolution	9 bit	9 bit	10 bit	8 bit
Sampling rate	50MHz	50MHz	40MHz	85MHz
Power supply	±1.5V	±1.5V	5.0V	±3.3 V
Power dissip.	10 mW	12 mW	36 mW	1100mW
SNDR at NR	52 dB	53 dB	56.7 dB	49 dB
DNL	0.7 LSB	0.7 LSB	0.6 LSB	0.8 LSB
INL	0.9 LSB	0.8 LSB	0.75 LSB	1.0 LSB
Active area	0.55mm x 0.35mm	0.85mm x 0.25mm	3.3mm x 3.2mm	3.9mm x 6.3mm

Measured performances of both ADCs have been compared to the performances of two switched capacitor voltage mode ADCs presented in literature [2, 3]. The first converter is composed of 1.5 bit stages , and the second of 2.5 bit stages, respectively. Their performances are shown in Table 1, in 4th and 5th columns, respectively.

TABLE II
Comparison of Performances of Proposed SI Converters and Known SI Converters

Performances	presented 1.5 bit stages	presented 2.5 bit stages	[6] 1.5 bit stages	[7] 3.5 bit stages
Technology	0.35µm	0.35µm	0.8µm	0.5µm
Resolution	9 bit	9 bit	10 bit	12 bit
Sampling rate	50MHz	50MHz	20MHz	5MHz
Power supply	±1.5V	±1.5V	3.0V	1.8 V
Power dissip.	10 mW	12 mW	82.5 mW	-
SNDR at NR	52 dB	53 dB	40.8 dB	71.6 dB
DNL	0.7 LSB	0.7 LSB	0.9 LSB	0.3 LSB
INL	0.9 LSB	0.8 LSB	0.9 LSB	0.6 LSB
Active area	0.55mm x 0.35mm	0.85mm x 0.25mm	2.7mm^2	0.8 x 0.5mm^2

The following performances: sampling rate, resolution, SNDR at Nyquist, DNL and INL are comparable to performances of the switched capacitor ADC structures. Power consumption, active area and power supply are lower. Low power consumption is a result of low power supply,

which has no influence on input current range and finally resolution. Small chip area is a result of small MOS capacitances used in switched current technique.

Additionally, performances of proposed ADCs are compared to performances of known SI ADC structures [6, 7]. Their performances are shown in Table 2 in 4th and 5th columns, respectively. Proposed structures results in the lower power consumption and the smaller active area. Most of the performances of ADC structure [6] are worse than performances of proposed ADC structures, while converter [7] results in better resolution only, but worse the other performances, respectively. Having examined results presented in Tables 1 and 2 we can conclude that the proposed ADCs function correctly and satisfy input requirements. The advantages of the proposed current mode converters are low power consumption and small active area. The other performances are similar to performances of known SC and SI pipelined ADCs.

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