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Low Power Capacitance-to-Voltage Converter for Magnetometer Interface IC

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***Abstract*—**This paper presents the design and implementation of a fully integrated Capacitance-to-Voltage Converter (CVC) as the analog front-end for magnetometer interface IC. The application demands very low power solution operating in the frequency of around 20 KHz. The design adapts low power architecture to create low noise electronic interface for Capacitive Micro-machined Lorentz force magnetometer sensor. Using a 0.18-µm CMOS process, simulation results of this interface IC show that the proposed CVC can provide 33 dB closed loop gain, 20 nV/√Hz input referred noise at 20 KHz, while consuming 65 µA current from 1.8-V supply.

***Keywords*—**Analog front end, Capacitance-to-Voltage Converter, Magnetometer, MEMS, Recycling Folded Cascode.

I. Introduction

THE growing interest in consumer electronics is to add more features and integrate them in one multipurpose device. Part of this trend, the inclusion of a magnetometer to serve as an electronic compass thereby facilitating navigation and location-based services, is expected to dramatically increase magnetometer demand [1]. Silicon MEMS magnetic field sensors, based on Lorentz force principle, are attractive because, unlike magneto resistive sensors they require no special magnetic materials, and they are much more sensitive than silicon Hall effect sensors [2]. MEMS Lorentz force sensors have the additional advantage of easy integration with other MEMS inertial sensors such as accelerometers, gyroscopes etc.

II. System Description

A. Lorentz Force Magnetometer

Fig. 1 shows a generic diagram of Lorentz force magnetometer sensor. If a current "I" is applied in the –y direction of the magnetometer any applied magnetic field, B in the ±z direction will create a force in the x-axis of the shuttle mass. This force is called Lorentz force is given by (1).

$$F_L = (I \times B) L_{mass} \quad (1)$$

where, F_L is the force applied to the structure, I is the current, B is the out-of-plane magnetic field and L_{mass} is the effective beam length (Fig. 1). The frequency of the current "I" is intentionally selected to be equal to the mechanical resonance frequency of the mechanical structure to maximize the mechanical response of the sensor. To enhance the total system resolution the quality factor of the sensor structure is kept reasonably high. This approach can be adopted easily as the magnetic field to be measured has bandwidth less than 10 Hz.

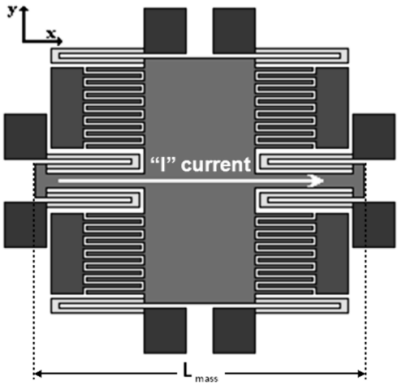

Fig. 1 Lorentz force sensor

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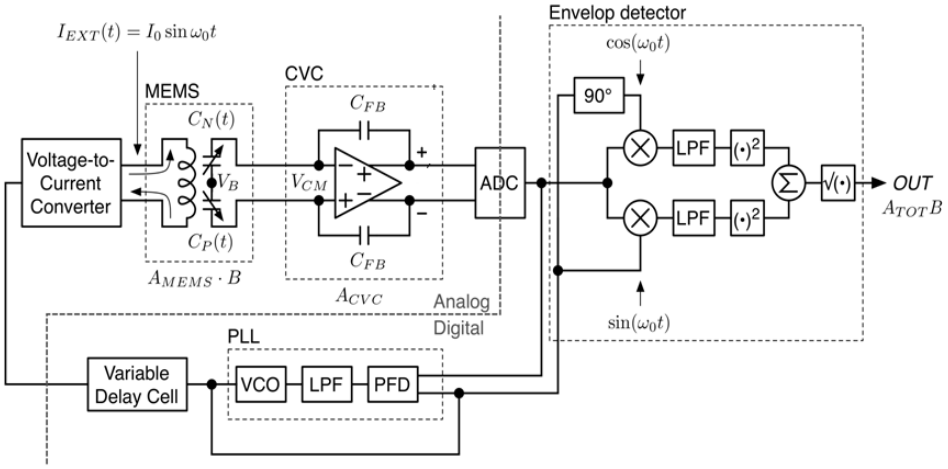


Fig. 2 Magnetometer System

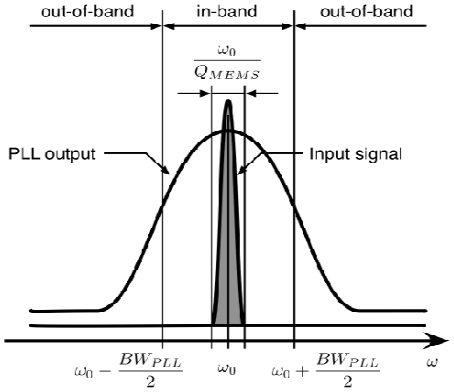


Fig. 3 PSD of PLL input and output

B. System Operation

Fig. 2 shows the system diagram adopted for this design. In order to drive the MEMS with an excitation having frequency same as the MEMS resonant frequency, a closed loop system has been conceptualized. Under the influence of an external magnetic field (B), the proof mass deflects, causing a differential capacitance change, which is converted by a capacitance-to-voltage converter (CVC) to a proportional voltage signal by charge integration. The CVC output is an AM modulated B field, with the MEMS resonance frequency as a carrier. An in-phase/quadrature-phase demodulation method is suggested to obtain a signal proportional to B field.

A phase locked loop (PLL) has been proposed to track the CVC output frequency. The variable delay cell block provides flexibility to search for the desired resonance frequency. The PLL loop bandwidth is chosen to be much higher than MEMS bandwidth (few Hz in this case) and much lower than the MEMS resonant frequency (20 KHz in this case). Under this condition, quality factor of MEMS determines the in-band noise performance. Under lock condition PLL out of band noise becomes less critical. Fig. 3 shows the power spectral density (PSD) of PLL input and output signal under steady state. In order to achieve robust and flexible performance signal detection and frequency tracking operation takes place in digital domain. An ADC is employed following CVC to convert the signal to digital domain. In this literature we are going to focus on design and implementation of the CVC pertaining to this system.

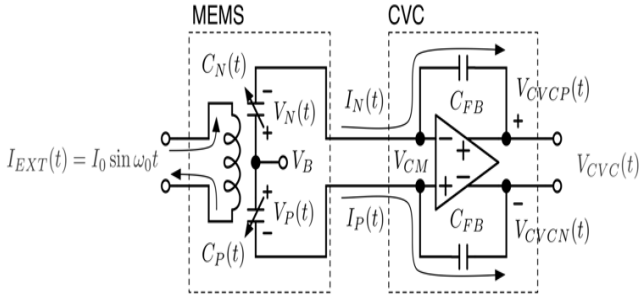


Fig. 4 CVC with MEMS Model

III. CVC Circuit Analysis and Specification

The capacitance-to-voltage converter (CVC) along with the sensor model is shown in Fig. 4. The operating principle has been qualitatively explained in previous section. This section will focus on quantitative formulation of capacitance to voltage conversion in this analog front end. Instantaneous position of the moving comb, measured from the quiescent point (Fig. 5) is given by (2).

$$d(t) = \frac{F_L(t)}{k} = \frac{LN_{coil}}{k} I_{EXT}(t)B = A_{d0} I_{EXT}(t)B \qquad (2)$$

Here,
$F_L(t)$: Lorentz force
k : spring constant of the MEMS moving comb
L : length of comb that intersects with magnetic field
$I_{EXT}(t)$: excitation current to the coil

B : intensity of the magnetic field
N_{COIL} : number of turns of the coil

As per Fig. 5, $d_P(t)$ and $d_N(t)$ denote distance from the moving comb to the positive or negative stationary comb, respectively (3).

$$d_P(t) = d_0 - d(t)$$
$$d_N(t) = d(t) + d_0 \quad (3)$$

Now the current $I_N(t)$ (Fig. 4) flowing to CVC can be calculated as given in (4).

$$I_N(t) = C_N(t)\frac{dV_N(t)}{dt} + V_N(t)\frac{dC_N(t)}{dt}$$
$$= (V_B - V_{CM})\frac{dC_N(t)}{dt} \quad (4)$$

Here, $C_N(t)$, instantaneous capacitance of one half of the sensor (Fig. 4), is given by (5).

$$C_N(t) = \frac{\varepsilon_0 \bullet area}{d_0 + A_{d0} I_0 B \sin(\omega_0 t + \phi_{MEMS})} \quad (5)$$

where, Φ_{MEMS} is the phase delay due to MEMS.

The voltage after charge integration at one output of CVC can be found as shown in (6).

$$V_{CVCP}(t) = V_{CM} - \frac{1}{C_{FB}}\int_{-\infty}^{t} I_N(\tau)d\tau$$
$$= V_{CM} - \frac{V_B - V_{CM}}{C_{FB}}(C_N(t) - C_N(\infty)) \quad (6)$$

Here, $C_N(\infty)$ is rest capacitance, C_0. Similarly, we can deduce for $V_{CVCN}(t)$ and assuming symmetry final CVC output, $V_{CVC}(t)$, can be approximated as follows.

$$V_{CVC}(t)$$
$$\approx 2\left[\frac{\varepsilon_0 .area}{d_0}\right]\left[\frac{A_{d0} I_0 B}{d_0}\right]\left[\frac{V_B - V_{CM}}{C_{FB}}\right]\sin(\omega_0 t + \phi_{MEMS} + \phi_{CVC})$$
$$= 2C_0\frac{d_{\max}}{d_0}A_{CVC}\sin(\omega_0 t + \phi_{MEMS} + \phi_{CVC}) \quad (7)$$

Here, A_{CVC} and Φ_{CVC} denote CVC gain and CVC phase delay respectively. Finally, d_{max}/d_0signifies normalized MEMS comb displacement with respect to quiescent displacement. Thus it is justified in (7) that the CVC output is an AM modulated B field, with the MEMS resonance as a carrier.

So far the amplifier in CVC has been assumed to be ideal. Due to finite gain bandwidth of the amplifier CVC gain reduces from its ideal value described in (7). Incorporating the gain error, non-ideal CVC gain is shown in (8).

$$A_{CVC} = \frac{V_B - V_{CM}}{C_{FB}}\left[1 - \frac{C_T}{C_{FB}A_0}\right] \quad (8)$$
$$C_T = C_{FB} + C_0 + C_{par}$$

Here, A_0 and C_{par} denote amplifier open loop gain (at f_0) and parasitic capacitance at input node. Considering the parameter values from sensor model, C_0=2.5 pF, C_{par}=2 pF, V_B=0, V_{CM}=0.9 V, f_0= 20 KHz, we plot CVC gain for different gain-bandwidth (GBW) of amplifier in Fig. 6. Negative value in this plot does not occur physically. In physical world it means transduction operation completely fails. From this plot, we target GBW of more than 5 MHz for C_{FB} in the range of 50fF-100 fF to achieve CVC gain of 8 pF/V. This translates to around 30 dB of closed loop voltage gain to be achieved from the amplifier.

The amplifier noise plays a significant role in system resolution. The input referred noise power $\overline{v_n^2}$ is transformed to output noise power following the relation (9).

TABLE I
CVC SPECIFICATION

Symbol	Quantity	Value
GBW	Amplifier Open loop Gain Bandwidth	5 MHz
A_0	Amplifier Open Loop Gain at 20 KHz	48 dB
v_n	Input Noise Density at 20 KHz	20 nV/√Hz
A_{CVC}	CVC Gain	8pF/V
P	Power Consumption	125 µWatt
A	Area	400 um X 400 um

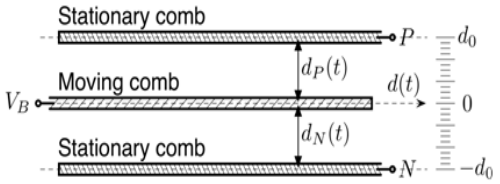


Fig. 5 Measurement in MEMS sensor

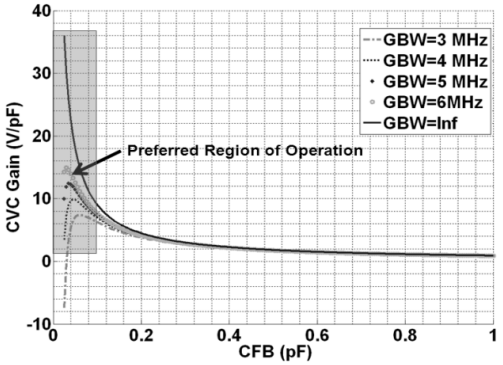


Fig. 6 CVC Gain versus C_{FB} for different GBW of amplifier

$$\overline{v_{no}^2} = \left(\frac{C_T}{C_{FB}}\right)^2 \overline{v_n^2} \quad (9)$$

The equivalent magnetic force noise corresponding to this electronic noise should satisfy the specification of 160 nT/√Hz at f_0=20 KHz. Through careful system analysis this specification has been translated to amplifier input referred noise of 20 nV/√Hz at 20 KHz. Table I shows the target specification for the CVC.

IV. Circuit Design

As the CVC is supposed to operate at around 20 KHz, it is possible to achieve flicker noise corner below this frequency by device sizing only. So we don't need to resort to any special flicker noise removal circuit technique such as chopping or correlated double sampling. This results in the circuit shown in Fig. 7. The dc common mode at output is defined by common mode feedback circuit. The bias resistor R_b helps define dc common mode for the input of CVC. Now value of this bias resistor has to be chosen in such a way that the resistive path offers much higher impedance than the capacitive path through C_{FB} at f_0. The minimum desired value for R_b is defined in (10).

$$R_b \geq \frac{10}{2\pi f_0 C_{FB}} \tag{10}$$

This suggests that the bias resistor should be in the order of tens of giga ohm. This can be achieved in area efficient manner by using pseudo resistor implemented by MOS devices in deep sub-threshold region. The pseudo resistor structure, discussed in [3], has been widely used in different similar applications with varied degree of success. However, it suffers from huge signal dependent non-linearity issue. In this paper, we propose to connect two series of diode connected PMOS devices in anti-parallel fashion as shown in Fig. 7. This offers more symmetrical impedance for both negative and positive signal swing at output. Thus signal dependency of the impedance is alleviated in this structure. However, to offer good linearity and high resistance value these devices tend to be of large dimension – W/L=5µm/20µm in this case. The parasitic capacitance, especially drain-to-bulk capacitance (C_{DB}), associated with these large PMOS devices increases the total feedback capacitance undesirably. To address this issue we insert device of smaller dimension, W/L=0.25µm/0.25µm in this case, in same diode connected fashion in the chain. Insertion of smaller capacitor in the series helps reduce the effective capacitance from the pseudo-resistor to negligible value. Additionally, to decrease the parasitic seen at the input of CVC we prefer to insert this smaller size device at both ends of the transistor chain (Fig. 7). Fig. 8 shows that incremental resistance of the proposed pseudo resistor structure mains fairly linear with respect to terminal voltage. For same device size the result has also been compared with the structure reported in [3] (Fig. 8).

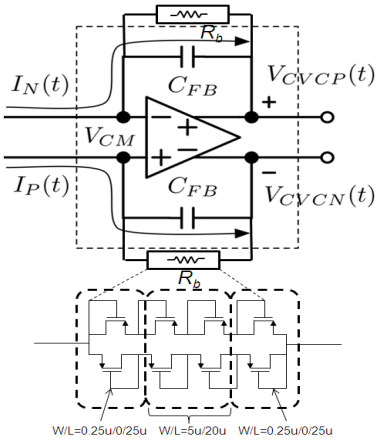


Fig. 7 CVC Circuit Diagram

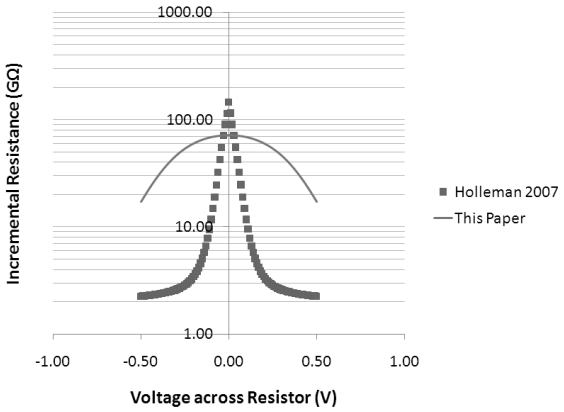


Fig. 8 Incremental Resistance of pseudo resistor

According to specification in table I, the amplifier has to be very much power efficient. Folded cascode (FC) operational amplifier (OPAMP) appears to be a potential choice (Fig. 9). Here transistors *M3* and *M4* are the two transistors in the signal path that conduct the most current, and in many designs have the largest trans-conductance. However, their role is strictly limited to providing a folding node for the small signal current generated by the input differential pair *M1* and *M2*.

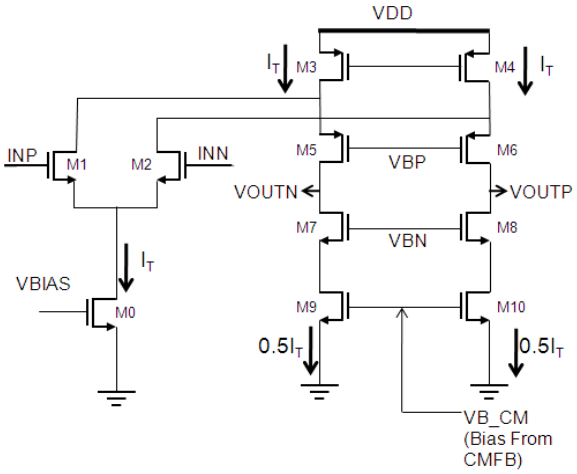
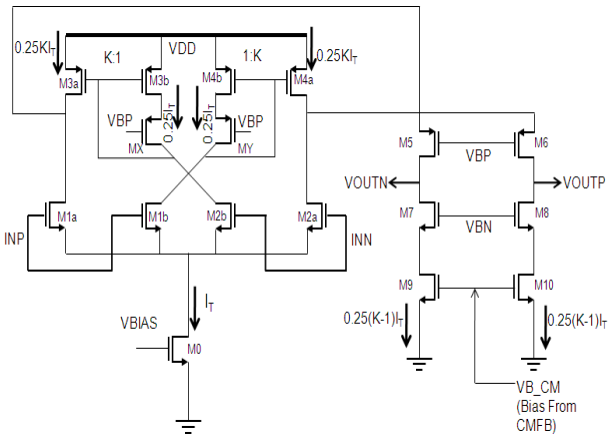
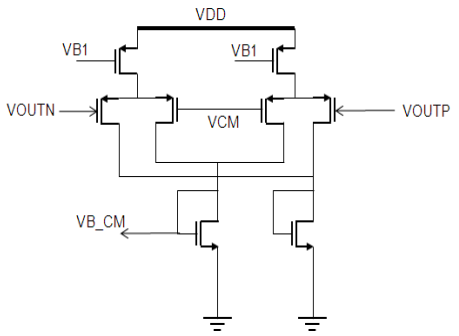


Fig. 9 Folded Cascode OPAMP



(a)



(b)

Fig. 10 CVC Amplifier (a) RFC (b) DDA CMFB

This inefficiency has been addresses by proposing recycling folded cascode (RFC) topology in [4] (Fig. 10 (a)). Here the input differential pair, *M1* and *M2* (Fig. 10 (a)), are split in half to produce transistors *M1a, M1b, M2a,* and *M2b* (Fig. 10 (a)). Next, *M3* and *M4* are split to form the current mirrors *M3a:M3b* and *M4a:M4b* with a ratio of *K:1*, where *K* is chosen to be 3 *strictly* to maintain the same current consumption as the FC in Fig. 9. Intuitively, *K* has to be *greater than* 1 to maintain current in the output devices *M5-M10*. The diode connected transistors, *M3b* and *M4b*, are cross-coupled with the input transistors, *M2b* and *M1b*. This arrangement ensures that the small signal currents added at the sources of *M5* and *M6* are in phase. Finally, cascode devices (*MX, MY*) are added inside the diode connection of *M3b* and *M4b* to improve matching in the current mirrors.

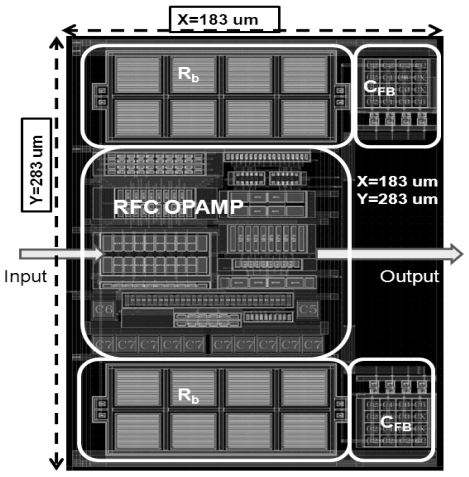


Fig. 11 CVC Lay-out

As revealed in [4] selecting *K=3*, RFC provides twice effective trans-conductance compared to FC consuming exactly same current. In comparison with FC the RFC has the same poles, but also an additional pole-zero pair, *ωp2* and*ωz1*, associated with the current mirrors *M3a*:*M3b* (and*M4a*:*M4b*). The choice of *K* plays a significant role in determining the positions of this additional pole. *K* is chosen such that *ωp2* > *3GBW*, which can be used to place an upper boundary on *K* .In this design, we have decided to use K=3.

Fig. 10 (b) shows differential difference amplifier (DDA) used to generate common-mode feedback (CMFB) for the output.

V. Simulation Results

The design has been carried out using Global foundry 0.18-µm CMOS 1P6M PDK. All circuit simulations are done with Cadence-Spectre simulator. Fig. 11 shows the final layout of the proposed CVC circuit. During simulation the board and package parasitic have been considered.

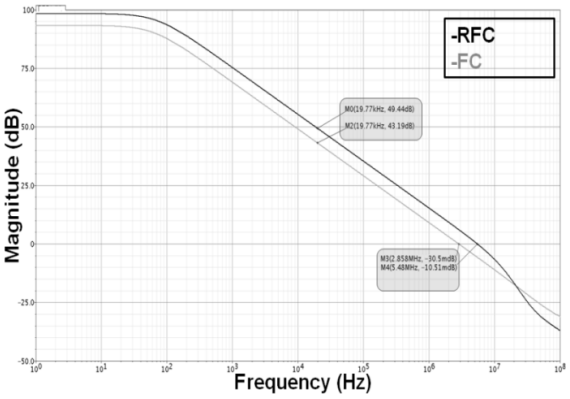
Fig. 12 shows open loop frequency response of RFC OPAMP. It can achieve 5.5 MHz GBW while burning 65 µA current from 1.8 V supply. The open loop gain 20 KHz appears to be ~50 dB. A similar FC OPAMP has also been designed. Under same power consumption FC OPAMP can only achieve a GBW half of achieved by RFC topology (Fig. 12 (a)). Fig. 13 shows spectral density of input referred noise for both the topologies. In terms of noise both appears to have comparable performance. Table II summarises relevant

parameters pertaining to RFC and FC OPAMP under same power consumption. This justifies the use of RFC OPAMP in the current design.

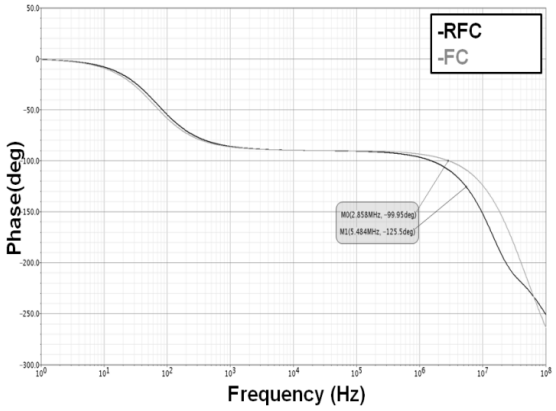
TABLE II
RFC AND FC COMPARISON

Parameter	RFC	FC
GBW (MHz)	5.5	2.85
A_0 (dB)	49.4	43.4
v_n (nV/√Hz)	17.5	18
Phase Margin (Deg)	55	80

Finally, the CVC frequency response is characterized with MEMS model. Fig. 14 shows the frequency response for both pre-layout and post-layout simulation. Approximately 33 dB of closed loop gain at 20 KHz appears in line with our specification.



(a)



(b)

Fig. 12 Amplifier AC response (a) magnitude (b) phase

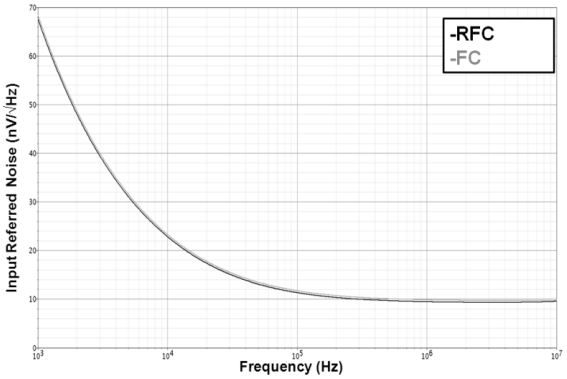


Fig. 13 Amplifier Input Noise spectral density

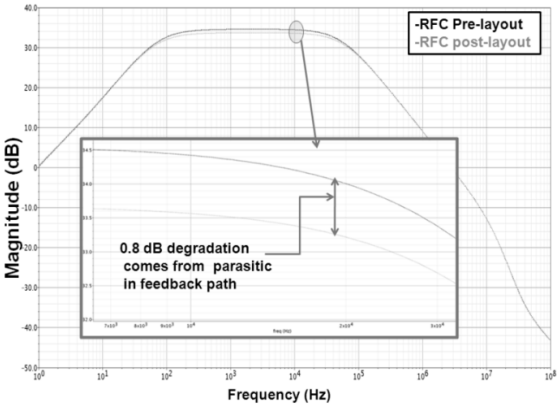


Fig. 14 CVC frequency response

VI. CONCLUSION

We present the design and implementation of a fully integrated capacitance-to-voltage converter dedicated to interface Lorentz force magnetometer sensor using 0.18-µm CMOS technology from Global Foundries. New fully integrated low power low noise CVC has been described. Simulation results validate its ability to meet the specifications. The proposed circuit has been sent for fabrication and measurements will be done when the prototypes are ready.

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