International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:4, No:8, 2010

Linear Pocket Profile based Threshold Voltage Model for sub-100 nm n-MOSFET

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Abstract—This paper presents a threshold voltage model of pocket implanted sub-100 nm n-MOSFETs incorporating the drain and substrate bias effects using two linear pocket profiles. Two linear equations are used to simulate the pocket profiles along the channel at the surface from the source and drain edges towards the center of the n-MOSFET. Then the effective doping concentration is derived and is used in the threshold voltage equation that is obtained by solving the Poisson's equation in the depletion region at the surface. Simulated threshold voltages for various gate lengths fit well with the experimental data already published in the literature. The simulated result is compared with the two other pocket profiles used to derive the threshold voltage models of n-MOSFETs. The comparison shows that the linear model has a simple compact form that can be utilized to study and characterize the pocket implanted advanced ULSI devices.

Keywords—Linear pocket profile, pocket implantation, nMOSFET, threshold voltage, short channel effect (SCE), reverse short channel effect (RSCE).

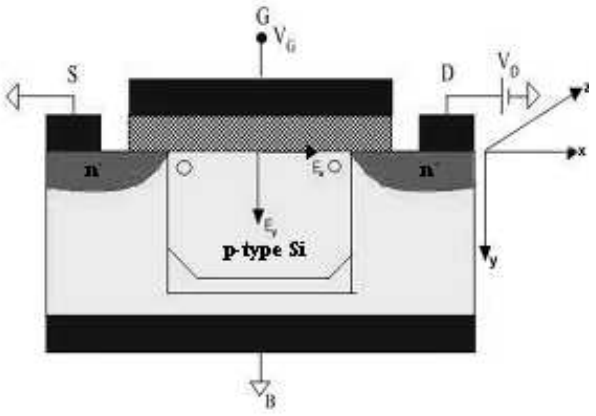

Fig. 1. Pocket implanted n-MOSFET Structure

I. Introduction

THE conventional threshold voltage model is derived for the homogeneous doping concentration [1]. As the channel length of MOSFETs is scaled down to deep-submicrometer or sub-100 nm regime, short-channel effects, such as, steep threshold voltage roll-off, increased off-state leakage current and bulk punch through have been observed [2]. The short channel effects arise as results of two dimensional potential distribution and high electric fields in the channel region. Thus two-dimensional modeling is required for short channel MOS transistors. The two dimensional analytical model of I-V characteristics of short channel MOS transistor has been developed earlier [3]. Lateral channel engineering utilizing halo-pocket implant [4], [5], [6], [7], [8] surrounding drain and source regions is effective in suppressing short channel effects. An extension of the homogeneous model to the non-homogeneous impurity pileup in the vertical direction has been reported previously [2], [4], [9]. However, the reported model cannot be extended further to the pocket implantation, where inhomogeneity along the channel is the main cause for the reverse short channel effect (RSCE) [10]. A strong reverse short channel effect suppresses the short channel effect on threshold voltage of the MOSFET [11]. Threshold voltage model for pocket implanted MOSFETs for circuit simulation does not describe the sub-100 nm case [11]. In this work, we propose a threshold voltage model capable of describing the threshold voltage for the gate length down to 50 nm.

Advanced MOSFETs are non-uniformly doped as a result of complex process flow. Therefore, one of the key factors to model threshold voltage (V_{th}) accurately is to model its non-uniform doping profile. Here the lateral 1-D pocket profile across the channel has been transformed to an effective doping concentration expression that can be applied directly to the V_{th} expression incorporating V_{th} shift due to short channel effect to suppress this effect. Besides, drain and substrate bias effects have also been incorporated. Here a short channel threshold voltage equation is used for the case of pocket implanted n-MOSFET where exponential dependence on channel length and a linear dependence on drain and substrate biases is observed [12] for various device and pocket profile parameters. Gaussian profile [13] and hyperbolic cosine profile [14] found in the literature for the threshold voltage model, are compared with the linear model. Simulation results using these two profiles along with the proposed linear profile show that the threshold voltage model is better for the linear profile. Besides, experimental data already published in the literature [5] fits well with our simulated data for various gate lengths. It proves the validity and usefulness of our proposed model.

II. Pocket Doping Profile

The pocket implanted n-MOSFET structure shown in Fig. 1 is considered in this work and assumed co-ordinate system

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Manuscript received February 19, 2010; revised March 11, 2010.

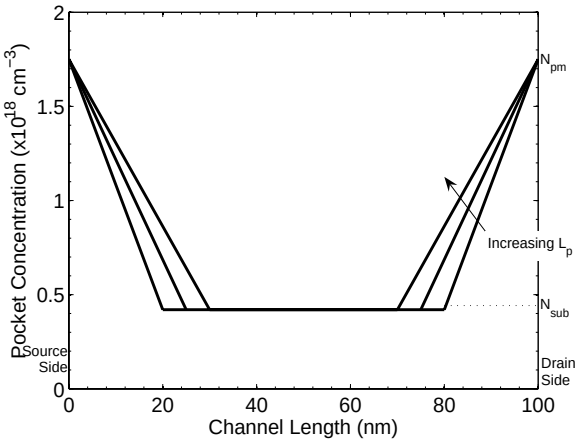

Fig. 2. Simulated pocket profiles at the surface for different pocket lengths, L_p = 20, 25 and 30 nm; peak pocket concentration, $N_{pm} = 1.75{\times}10^{18}$ cm^{-3} with substrate doping concentration, $N_{sub} = 4.2{\times}10^{17}$ cm^{-3}

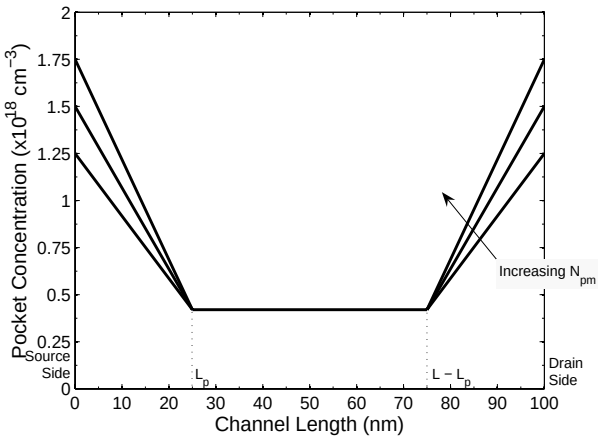

Fig. 3. Simulated pocket profiles at the surface for various peak pocket concentrations, $N_{pm} = 1.25 \times 10^{18}, 1.5 \times 10^{18}$ and 1.75×10^{18} cm^{-3}; pocket length, $L_p = 25$ nm with substrate doping concentration, $N_{sub} = 4.2{\times}10^{17}$ cm^{-3}

is shown at the right side of the structure.

All the device dimensions are measured from the oxide-silicon interface. In the structure, the junction depth (r_j) is 25 nm. The oxide thickness (t_{ox}) is 2.5 nm, and it is SiO_2 with fixed oxide charge density of 10^{11} cm^{-2}. Uniformly doped p-type Si substrate is used with doping concentration of $N_{sub} = 4.2{\times}10^{17}$ cm^{-3} with pocket implantation both at the source and drain side with peak pocket doping concentration of $1.5{\times}10^{18}$ cm^{-3} and pocket lengths from 20 to 30 nm, and source or drain doping concentration of $9.0{\times}10^{20}$ cm^{-3}. The model of the conventional bulk n-MOSFET exhibits drastic reduction of the threshold voltage (V_T) from the long channel value beyond 100 nm. This is known as short channel effect. A group of analytical models, known as "charge-sharing" models, are found in the literature. But their accuracy is limited [12]. In [12], a model is presented that solves the two-dimensional Poisson equation analytically, and predicts V_T accurately as a function of drain bias (V_D), substrate bias (V_{BS}), channel length (L), oxide thickness (t_{ox}) and substrate concentration (N_{sub}). This model is then transformed to short channel n-MOSFET assuming the step doping profile along the vertical direction of the channel.

To preserve the long channel threshold voltage behavior for the short channel device, pocket implantation, which causes reverse short channel effect (RSCE), is done by adding donor atoms both from the source and drain edges. The peak pocket doping concentration (N_{pm}) gradually decreases towards the substrate level concentration (N_{sub}) with pocket length (L_p) from both the source and drain edges. The basis of the model of the pocket is to assume two linear doping profiles from both the source and drain edges across the channel as shown in Figs. 2-3. The pocket parameters, N_{pm} and L_p, play important role in determining the RSCE.

At the source side, the pocket profile is given as:

$$N_s(x) = -\frac{N_{pm} - N_{sub}}{L_p}x + N_{pm}$$

$$N_s(x) = N_{sub}\frac{x}{L_p} + N_{pm}\left(1 - \frac{1}{L_p}x\right) \quad (1)$$

At the drain side, the pocket profile is given as:

$$N_d(x) = \frac{N_{pm} - N_{sub}}{L_p}\left[x - (L - L_p)\right] + N_{sub}$$

$$N_d(x) = N_{sub}\left(\frac{L}{L_p} - \frac{1}{L_p}x\right) + N_{pm}\left(1 - \frac{L}{L_p} + \frac{1}{L_p}x\right) \quad (2)$$

where x represents the distance across the channel. Since the pile-up profile is due to the direct pocket implant at the source and drain side, it is assumed symmetric at both sides.

With these two conceptual pocket profiles, the profiles are integrated mathematically along the channel length and then divided by it to derive an average effective doping concentration as in equation (3).

$$N_{eff} = \frac{1}{L}\int_0^L \Big[N_s(x) + N_d(x) + N_{sub}\Big]\mathrm{d}x \quad (3)$$

Putting the expressions of $N_s(x)$ and $N_d(x)$ from equations (1) and (2) in equation (3) the effective doping concentration is obtained as in equation (4).

$$N_{eff} = N_{sub}\left(1 - \frac{L_p}{L}\right) + \frac{N_{pm}L_p}{L} \quad (4)$$

When $L_p \ll L$ for long channel device then pocket profile has very little effect on V_{th}, But when L_p is comparable with L then pocket profile affects V_{th}.

III. Threshold Voltage Model

In [15], the threshold voltage model was obtained by solving the 1-D Poisson equation and then applying Gauss's law, but that model did not incorporate the effect of substrate and drain biases. The threshold voltage model derived in

[12] incorporated the effects of substrate and drain biases on threshold voltage for vertically non-uniform doping profile. Based on that concept, we derived a threshold voltage model for our proposed pocket doping profile along the channel. This model incorporates the effective doping concentration of our linear pocket profiles given in equation (4) to derive the threshold voltage equations and hence we obtain the V_{th} expression as given in equation (5).

$$V_{th} = V_{th,L} + \gamma_B \left[\frac{N_{sub}}{N_{eff}}(2\varphi_F) - V_{BS}\right]^{\frac{1}{2}} - \gamma_A \frac{N_{sub}}{N_{eff}}(2\varphi_F)^{\frac{1}{2}} - \frac{6t_{ox}}{d_1}\left[2(\phi_{bi} - V_{BS}) + V_{DS}\right]\exp\left(-\frac{\pi L}{4d_1}\right) \quad (5)$$

where $V_{th,L}$ is the long channel threshold voltage, the second and the third parts include the threshold voltage due to both the effect of substrate bias and effective doping concentration, the fourth part incorporates the effects of drain and substrate biases as well as the short channel effect.

The long channel threshold voltage, $V_{th,L}$ for the pocket implanted n-MOSFET is given by the equation (6).

$$V_{th,L} = V_{FB} + 2\varphi_F + \gamma_A(2\varphi_F)^{\frac{1}{2}} \quad (6)$$

where V_{FB} is the flat band voltage. From simulation it is found as -0.9316 V. φ_F, γ_A and γ_B are Fermi potential due to pocket implantation, threshold sensitivity due to back bias for effective doping concentration along the channel and body factor corresponding to bulk doping respectively and are given in equations (7)-(9).

$$\varphi_F = \frac{kT}{q}\ln\frac{N_{eff}}{n_i} \quad (7)$$

$$\gamma_A = \frac{\sqrt{2q\epsilon_{Si}N_{eff}}}{C_{ox}} \quad (8)$$

$$\gamma_B = \frac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}} \quad (9)$$

The depth (where band bending of $2\varphi_F$ occurs) of the pocket doping vertical to the channel (d_1) and the built-in potential (ϕ_{bi}) at the source or drain to channel junction are given by the equations (10) and (11) respectively.

$$d_1 = \left(\frac{2\epsilon_{Si}}{qN_{eff}}\right)^{\frac{1}{2}}(2\varphi_F)^{\frac{1}{2}} \quad (10)$$

$$\phi_{bi} = \frac{kT}{q}\ln\frac{N_{sd}N_{eff}}{n_i^2} \quad (11)$$

where N_{sd} is the source or drain doping concentration and n_i is the intrinsic carrier concentration of Si.

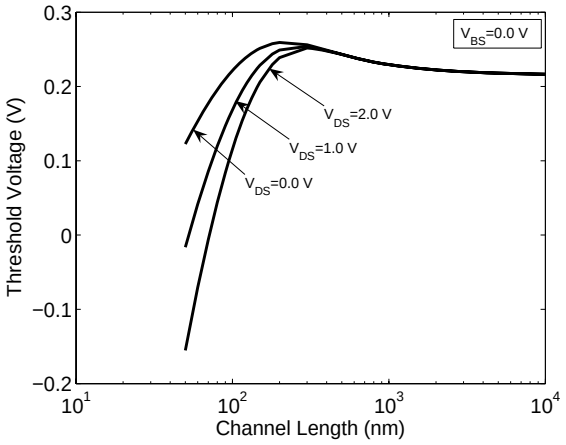

Fig. 4. Threshold voltage vs. gate length curves for various drain biases at zero substrate bias

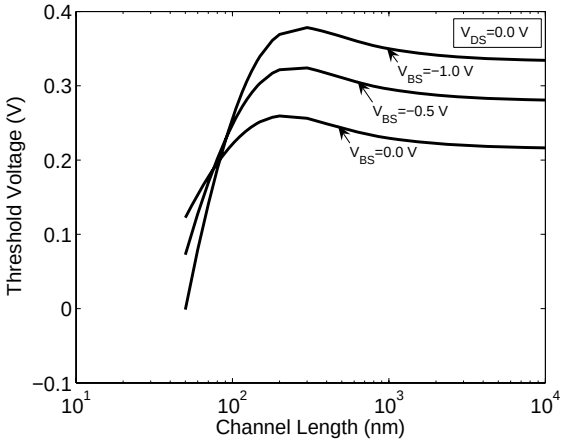

Fig. 5. Threshold voltage vs. gate length curves for various substrate biases at zero drain bias

IV. Results and Discussions

The simulated V_{th} vs. L curve has been drawn for this new model is shown in Figs. 4-5 for different drain and substrate biases. It was shown in [15] that with the increasing pocket lengths and peak pocket concentrations, the peak of this curve increases and the onset of threshold voltage (V_{th}) roll-up happens at a longer channel length and also the onset of V_{th} roll-off happens at a shorter channel length. This result exhibits strong RSCE with the increased L_p and N_{pm}. If these are increased further by keeping the other parameters constant then V_{th} roll-off starts to vanish exhibiting only reverse short channel effect.

From Fig. 4, it is observed that as the drain bias increases, both RSCE and SCE occur at longer channel length due to the drain induced barrier lowering (DIBL). As channel length becomes shorter DIBL effect is more pronounced. Higher drain bias makes the threshold voltage negative. Since at shorter channel length, electric field is very high and it lowers

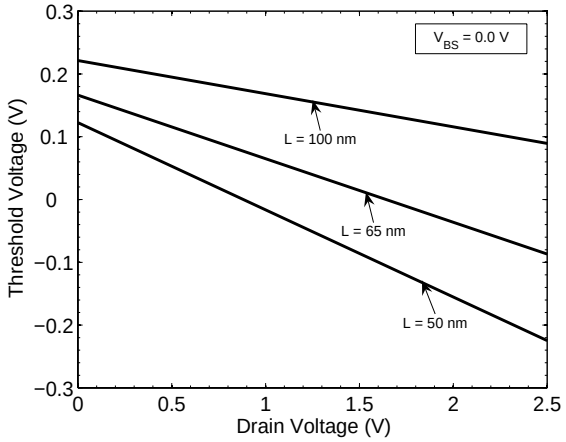

Fig. 6. Threshold voltage vs. drain voltage curves for various gate lengths with $V_{BS} = 0.0$ V

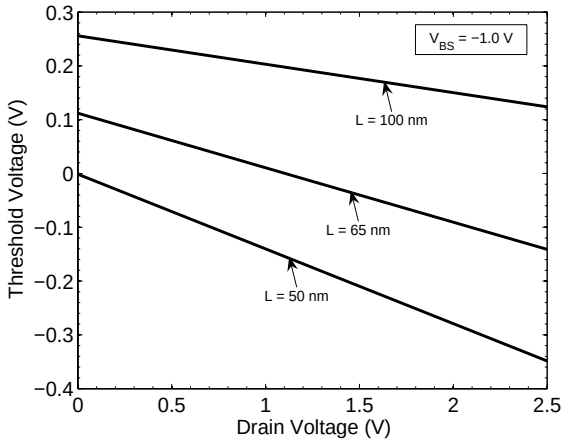

Fig. 7. Threshold voltage vs. drain voltage curves for various gate lengths with $V_{BS} = -1.0$ V

the potential barrier that separates it from the adjacent diffused junction. Therefore, due to the presence of high channel doping even at negative gate voltage drain current starts to flow.

From Fig. 5, it is found that as the substrate bias increases in the negative direction the threshold voltage increases. This is due to the increment of depletion charge under the gate. Also, with increasing magnitude of V_{BS}, RSCE occurs at longer channel length (L), threshold voltage (V_{th}) roll-off becomes steeper and V_{th}-L curve crosses the zero-substrate bias curve at shorter channel length. This is because of the linear dependence of V_{DS} and V_{BS} on V_{th} and exponential dependence of L on V_{th}. As V_{BS} becomes more negative RSCE starts to diminish.

Figs. 6-7 show the variation of threshold voltage with the drain bias for different substrate biases of $V_{BS} = 0.0$ V and $-$ 1.0 V respectively with channel length as a parameter. It is observed that as the drain bias increases threshold voltage

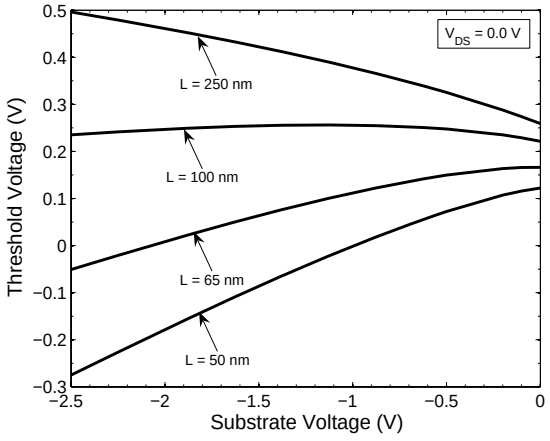

Fig. 8. Threshold voltage vs. substrate voltage curves for various gate lengths with $V_{DS} = 0.0$ V

decreases. As the channel length shrinks, this effect becomes more prominent. For longer channel device, lateral electric field is less than the transverse electric field. Thus for low drain bias diffusion current dominates over drift current. Hence threshold voltage does not deviate too much from low drain bias to high drain bias. But for shorter channel device, lateral electric field becomes stronger at low drain bias too. Hence drift current increases at low drain bias thereby larger threshold voltage deviation is observed from low to high drain bias.

Fig. 8 shows the variation of threshold voltage with the substrate bias for different channel lengths at zero drain bias. It is seen that as V_{BS} increases in the negative direction threshold voltage increases for long channel lengths and decreases for short channel lengths, i.e. in the sub-100 nm regime, and near 100 nm channel lengths threshold voltage is insensitive to substrate bias. This phenomenon happens due to the pocket implantation. When substrate bias increases in the negative direction in the long channel device, depletion layer charge increases due to the increase of depletion layer width that causes the threshold voltage to increase. But in the short channel device, threshold voltage decreases due to the increment of minority carriers at the surface when the substrate bias increases in the negative direction.

Fig. 9 shows that our model based on linear pocket profile exhibits better result of suppressing short channel effect in comparison with the other models for the pocket profiles based on Gaussian [13] and hyperbolic cosine functions [14]. This can be explained using the Fig. 10 where we show the effective carrier concentration variation with the channel length. Here, we see that the effective carrier concentration increases very smoothly for the linear pocket profile as the channel length shrinks. But in case of hyperbolic cosine function, it does not start to increase until 200 nm. But the SCE starts before 100 nm [15]. Therefore, for hyperbolic cosine model, at first SCE starts and then again RSCE becomes stronger below 100 nm.

On the other hand, in case of Gaussian function, the effective carrier concentration increases more rapidly than that

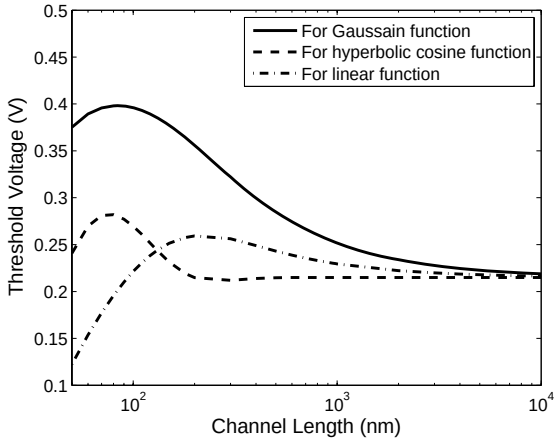

Fig. 9. Threshold voltage vs. gate length curves for three different pocket profiles based on linear, Gaussian and hyperbolic cosine functions for $N_{pm} = 1.75 \times 10^{18}$ cm^{-3}, L_p = 25 nm and $N_{sub} = 4.2 \times 10^{17}$ cm^{-3}

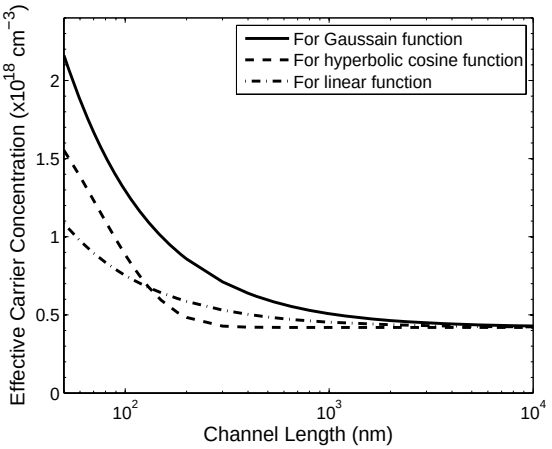

Fig. 10. Effective carrier concentration with channel lengths for three different pocket profiles based on linear, Gaussian and hyperbolic cosine functions for $N_{pm} = 1.75 \times 10^{18}$ cm^{-3}, L_p = 25 nm and $N_{sub} = 4.2 \times 10^{17}$ cm^{-3}

in the linear model. Therefore, in Fig. 9, we observe that RSCE is stronger. Thus in this case, threshold voltage increases until 40 nm. But in sub-100 nm regime our purpose is to suppress the SCE only by the RSCE by implanting the pockets. Besides, simulation time taken to calculate threshold voltage by using our model is less than that by using Gaussian function and hyperbolic cosine function models.

In Fig. 11, we tried to fit experimental data from [5] with our simulated data for the device parameters given in [5]. The parameter values are- substrate concentration, $N_{sub} = 1.0 \times 10^{17} cm^{-3}$, peak pocket concentration, $N_{pm} = 5.5 \times 10^{17} cm^{-3}$, pocket length along the channel, $L_p = 60 \times 10^{-7}$ cm either from source or drain side, oxide thickness, $t_{ox} = 6 \times 10^{-7}$ cm, junction depth, $r_j = 80 \times 10^{-7}$ cm, substrate bias, $V_{BS} = 0.0$ V and drain bias, $V_{DS} = 0.05$ V. Flat band voltage obtained by simulation is $V_{FB} = -0.9$ V. From Fig. 11, it is clear that

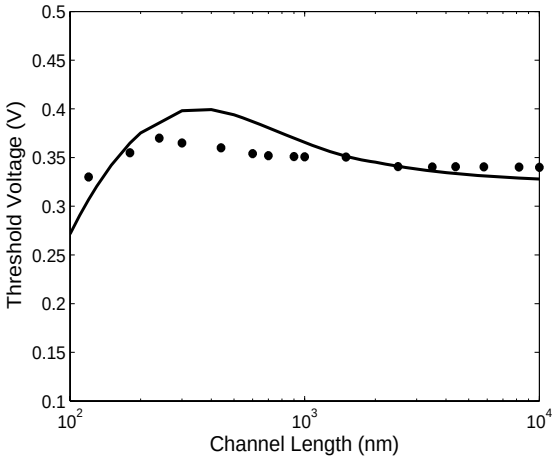

Fig. 11. Fitting experimental data (dots) already published in the literature [5] with the simulated results of our proposed model (solid line)

our simulated data almost agrees well with the experimental data in [5]. In the short channel device, our model shows better results. By changing the process conditions, it is possible to adjust the experimental results with the simulated data. Because, we only adjusted the flat band voltage to fit the experimental data.

V. Conclusion

A threshold voltage model for ultra thin oxide and sub-100 nm pocket implanted n-MOSFET has been developed incorporating the substrate and drain bias dependence. The well-known reverse short channel effect has been observed through the proposed model. The model is developed assuming two linear pocket profiles along the channel at the surface of the MOS device from the source and drain edges. The proposed model along with the other two models of threshold voltage has been simulated using the same values for the different parameters and compared for V_{th} vs. L characteristics. Experimental results already published in the literature have also been compared with our simulated results and fit very well. It is found that our model efficiently determines the threshold voltages of scaled n-MOSFETs having channel lengths in sub-100 nm regime and shows better performance than the other two models. Therefore, this model is very useful for circuit simulation.

References

[1] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York, USA: John Wiley & Sons, 1981, ch. 8.
[2] M. Miura-Mattausch, M. Suetake, H. J. Mattausch, S. Kumashiro, N. Shigyo, S. Oganaka, and N. Nakayama, "Physical modeling of the reverse short channel effect for circuit simulation," *IEEE Transactions on Electron Devices*, vol. 48, pp. 2449–2452, Oct. 2001.
[3] H. E. Ghitani, S. Sadik, and A. H.Shousha, "Two dimensional analytical modeling of short channel MOS transistors," *International Journal of Electronics*, vol. 81, pp. 517–524, 1996.
[4] K. Y. Lim and X. Zhou, "Modeling of threshold voltage with non-uniform substrate doping," in *Proceedings of the IEEE International Conference on Semiconductor Electronics (ICSE 1998)*, Malaysia, 1998, pp. 27–31.

[5] B. Yu, C. H. Wann, E. D. Nowak, K. Noda, and C. Hu, "Short channel effect improved by lateral channel engineering in deep-submicrometer MOSFETs," *IEEE Transactions on Electron Devices*, vol. 44, pp. 627–633, Apr. 1997.
[6] B. Yu, H. Wang, O. Millic, Q. Xiang, W. Wang, J. X. An, and M. R. Lin, "50 nm gate length CMOS transistor with super-halo: Design, process and reliability," *IEDM Technical Digest*, pp. 653–656, 1999.
[7] K. M. Cao, W. Liu, X. Jin, K. Vasant, K. Green, J. Krick, T. Vrotsos, and C. Hu, "Modeling of pocket implanted MOSFETs for anomalous analog behavior," *IEDM Technical Digest*, pp. 171–174, 1999.
[8] Y. S. Pang and J. R. Brews, "Models for subthreshold and above subthreshold currents in 0.1 μm pocket n-MOSFETs for low voltage applications," *IEEE Transactions on Electron Devices*, vol. 49, pp. 832–839, May 2002.
[9] Y. Cheng, T. Sugii, K. Chen, and C. Hu, "Modeling of small size MOSFETs with reverse short channel and narrow width effects for circuit simulation," *Solid State Electronics*, vol. 41, pp. 1227–1231, 1997.
[10] M. K. Khanna, M. C. Thomas, R. S. Gupta, and S. Haldar, "An analytical model for anomalous threshold voltage behavior of short channel MOSFETs," *Solid State Electronics*, vol. 41, pp. 1386–1388, 1997.
[11] Y. Taur and E. J. Nowak, "CMOS devices below 0.1 μm; how high will go?" *IEDM Technical Digest*, pp. 215–218, 1997.
[12] K. N. Ratnakumar and J. D. Meindl, "Short-channel MOST threshold voltage model," *IEEE Journal of Solid State Circuits*, vol. 17, pp. 937–948, Oct. 1982.
[13] X. Zhou, K. Y. Lim, and D. Lim, "Physics-based threshold voltage modeling with reverse short channel effect," *Journal of Modeling and Simulation of Microsystems*, vol. 2, no. 1, pp. 51–56, 1999.
[14] ——, "A general approach to compact threshold voltage formulation based on 2-D numerical simulation and experimental correlation for deep-submicron ulsi technology development," *IEEE Transactions on Electron Devices*, vol. 47, no. 1, pp. 214–221, Jan. 2000.
[15] M. H. Bhuyan, F. Ferdous, and Q. D. M. Khosru, "A threshold voltage model for sub-100 nm pocket implanted NMOSFET," in *Proceedings of the 4th IEEE International Conference on Electrical and Computer Engineering (ICECE 2006)*, Dhaka, Bangladesh, Dec. 2006, pp. 522–525.

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