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Investigation of 5,10,15,20-Tetrakis(3’,5’-Di-Tert-Butylphenyl)Porphyrinatocopper(II) for Electronics Applications

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Abstract**—**In this work, an organic compound 5,10,15,20-Tetrakis(3,5-di-tertbutylphenyl)porphyrinatocopper(II) (TDTBPPCu) is studied as an active material for thin film electronic devices. To investigate the electrical properties of TDTBPPCu, junction of TDTBPPCu with heavily doped n-Si and Al is fabricated. TDTBPPCu film was sandwiched between Al and n-Si electrodes. Various electrical parameters of TDTBPPCu are determined. The current-voltage characteristics of the junction are nonlinear, asymmetric and show rectification behavior, which gives the clue of formation of depletion region. This behavior indicates the potential of TDTBPPCu for electronics applications. The current-voltage and capacitance-voltage techniques are used to find the different electronic parameters.

Keywords**—**P-type, organic semiconductor, Electrical characteristics

I. INTRODUCTION

THE motivation of using organic materials in electronic devices arose from their easily tunable properties, low cost, low temperature processing, reel-to-reel printing, and compatibility with flexible substrates [1-3]. Organic materials have the ability to be modified in such a way that could directly impact their chemical properties [4]. These materials provide a diversity of interesting features, making the realization of organic devices with advantages over the conventional inorganic technology [5-7].

The knowledge of processes like injection, transport and recombination is required to understand the electronic devices. Metal/organic junctions are the basic structures to investigate these processes. By studying electrical characteristics of these junctions, we can extract the parameters that control the device performance.

Many authors [8-11] investigated the properties of porphyrin derivatives. Their results show that porphyrins have great potential for electronics applications. However, a stable junction could not be fabricated successfully from organic semiconductors because p and n-type doping cannot be separately introduced to adjacent layers. This problem can be overcome by attempting the fabrication of organic-inorganic semiconductor hybrid junctions. Hybrid organic-inorganic structures present an interesting alternative to all inorganic and all organic electronic devices, allowing association of stability and efficiency of inorganic semiconductors with tunability of band level energies of organic semiconductors. Efficient hetero-junction can be realized by this approach.

In the present work, an organic semiconductor TDTBPPCu has been investigated to explore its potential for electronics applications. An inorganic semiconductor substrate is used for growing organic molecules.

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II. EXPERIMENTAL PROCEDURE

The organic semiconductor 5,10,15,20-Tetrakis(3’,5’-di-tert-butylphenyl) porphyrinatocopper(ll) (TDTBPPCu) and heavily doped n-silicon<110> wafer are used for fabrication of the junction. The molecular structure of TDTBPPCu is shown in Figure 1. The silicon wafer was cleaned using acetone in ultrasonic cleaner at room temperature for 10 min. Then the substrate was plasma cleaned for 5 min. On the polished surface of n-Si, TDTBPPCu was deposited by spin coating. Thickness of TDTBPPCu was 150 *nm*. The contacts on TDTBPPCu and back side of n-Si were made by Al. The area of each contact was $2.58 x 10^{-3}$ cm^2. The deposition was done at growth rate of 0.1 nms^{-1} under $5.5x10^{-6}$ *mbar* chamber pressure. Figure 2 shows the schematic diagram of Al/TDTBPPCu/n-Si/Al device. Current-voltage and capacitance-voltage characteristics were performed by current-voltage analyzer *MDC CSM/Win Systems-Quiet CHUCK* of Material Corporation.

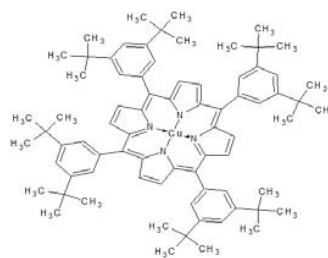

Fig. 1 Molecular structure of TDTBPPCu

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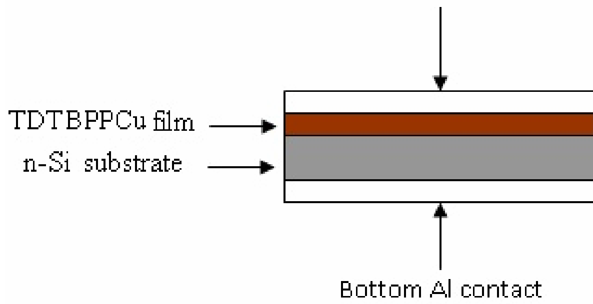

Fig. 1 Cross-sectional view of Al/TDTBPPCu/n-Si/Al hetero-junction

III. Results and discussion

The current-voltage characteristics of Al/TDTBPPCu/n-Si/Aljunction are shown in Figure 3. The forward bias corresponds to the positive potential at top Al electrode. The current-voltage characteristics of the junction are nonlinear, asymmetric and show the rectification behavior, which gives the clue of formation of the depletion regions at interfaces of the Al/TDTBPPCu/n-Si/Al junction. This behavior is due to the fact that a space charge layer is formed at the Al/TDTBPPCu/n-Si/Al interfaces. The current-voltage characteristics of Al/TDTBPPCu/n-Si/Al junction under the forward bias condition show the exponential increase in current at low voltage due to decrease in the depletion layer width at the interfaces. At higher voltages the current-voltage characteristics are almost linear because the depletion layer is minimized at the interfaces and TDTBPPCu film act as series resistance. While in the reverse bias the depletion layer width increases and almost all the current is due to the minority carriers of TDTBPPCu. The junction shows good rectifying behavior. The rectification ratio (RR) is determined as the ratio of the forward current to the reverse current at a certain applied voltage (I_F/I_R). The equation, which describes the current as a function of the applied voltage of the junction can be expressed as:

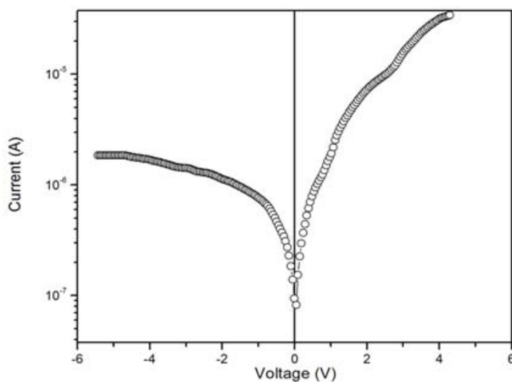

Fig. 2 I-V characteristics of Al/TDTBPPCu/n-Si hetero-junction

$$I = I_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

Where, I_o is the reverse saturation current and is given as:

$$I_o = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \quad (2)$$

The I-V characteristics show an increase in the forward current with applied voltage for the junction at low voltage range. This increase can be attributed to the formation of depletion layer. From Figure 3, the junction parameters are calculated. The value of reverse saturation current is found 5.8×10^{-7} A. The Richardson's constant (A*) for n-Si is 112±6 $Am^{-2}K^{-2}$. The barrier height is found 0.39 *eV*. The value of ideality factor of Al/TDTBPPCu/n-Si/Al surface type Schottky diode is calculated as 24.5 from the current-voltage characteristics by using the following equation [12]:

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \quad (3)$$

Where, V is the applied voltage, T is the temperature in Kelvin. Forward bias current-voltage characteristic at low voltage are linear in semi-logarithmic scale, but at higher voltages the characteristics deviate from linear behavior. For non-ideal diodes, the characteristics often present a more complex behavior than the ideal diodes due to the presence of various conduction mechanisms [13]. For such non-ideal diodes the following modified Schottky equation can be used [14]:

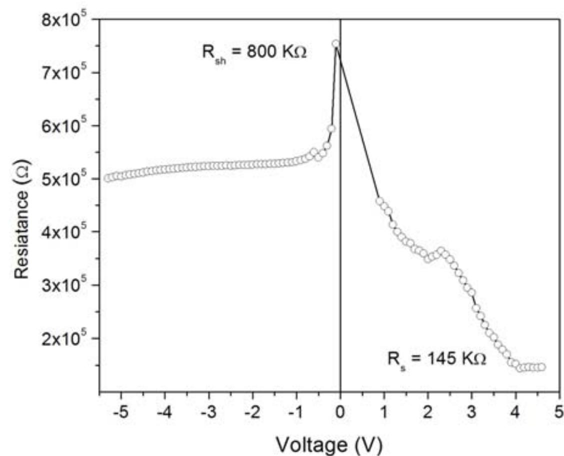

Fig. 3 Graph of junction resistance vs. voltage for TDTBPPCu/n-Si hetero-junction

$$I = I_{o1}\left[\exp\left(\frac{qV - IR_s}{n_1 kT}\right) - 1\right] + I_{o2}\left[\exp\left(\frac{qV - IR_s}{n_2 kT}\right) - 1\right] + \frac{V - IR_s}{R_{sh}} \quad (4)$$

Where, R_s is the series resistance and R_{sh} is the shunt resistance. This equation also includes the effects of parasitic series and parallel resistance, which can obscure the intrinsic parameters of the device. The values of R_s, and R_{sh}, are found from the junction resistance (RJ) vs. voltage (V) plot where RJ = $\delta V/\delta I$. A plot of RJ vs. V is shown in Figure 4. It is

observed that at higher voltage in forward bias the junction resistance approaches about to a constant value, this value is taken as R_s while in reverse bias the maximum value of junction resistance is equal to junction R_{sh}. The values R_s and the R_{sh} are found $8.0x10^5$ *Ω* and $1.45x10^2$ *Ω*, respectively.

Capacitance-voltage measurement is one of the most important methods for obtaining information about the rectifying junctions. Some times the capacitance under forward bias exceeds the space-charge capacitance predicted by theory. The excess capacitance is due to traps at the junction interface. These traps can be created by dangling bonds, inter-diffusion of atoms and crystal defects at the metal/semiconductor or organic materials/inorganic semiconductor interfaces. The capacitance-voltage measurements of the junction were performed at different frequencies. The capacitance-voltage measurements of the heterojunction at 1.0 *MHz* is shown in Figure 5. It is observed that the value of capacitance of the device is greater at low frequencies as compared to higher frequencies. At lower frequencies, the higher capacitance is due to excess capacitance resulting from the interface states which are in equilibrium with the organic semiconductor. At low frequency the interface states follow the AC signal gives the excess capacitance. Therefore, the total capacitance will be equal to space charge capacitance and interface capacitance. It is also observed that at higher frequency the capacitance remain almost constant. This effect may be due to reason that interface states can not follow AC signal and do not contribute to the diode capacitance. This will occur when the time constant is too long to permit the charge to move in and out of the traps in response to an applied signal [15, 16]. The value of the capacitance increases in forward bias till a point where it reaches a maximum value and then decreases. The accumulation capacitance for the junction is found 4.96 *nF*. This capacitance comes from native oxide layer between Si and organic semiconductor. The relation between voltage and capacitance can be expressed as [17]:

$$1/C^2 = 2(V_{bi} + V)/A^2 \varepsilon_s q N_D \tag{5}$$

Where, is the dielectric constant of semiconductor is built in potential and is the donor concentration. The value of barrier height can be obtained by using following relation.

$$q\phi_b = qV_{bi} + kT\ln(N_c / N_D) \tag{6}$$

Where, is the effective density of states in the conduction band of silicon (= 2.8x1019 *cm* $^{-3}$) is calculated from the slope of C^{-2}-V plot (Figure 6), from C-V measurements of the heterojunction at 1.0 *MHz* and is found 1.17x1018 *cm* $^{-3}$. The value of V_{bi} = 0.58 *V* is calculated from the x-intercept of Figure 6. The barrier height can be obtained from the C-V measurements using Eq. (6). Its value is found as 0.50 eV. This value is greater than the value obtain from I-V. This is probably due to the barrier inhomogeneity. It is seen that the barrier heights deduced from two techniques are not always the same. The discrepancy between barrier height obtained from C-V and barrier height from I-V can be explained by distribution of barrier height due to the in homogeneities such as non-uniformity of the interfacial layer thickness and distributions of the interfacial charges.

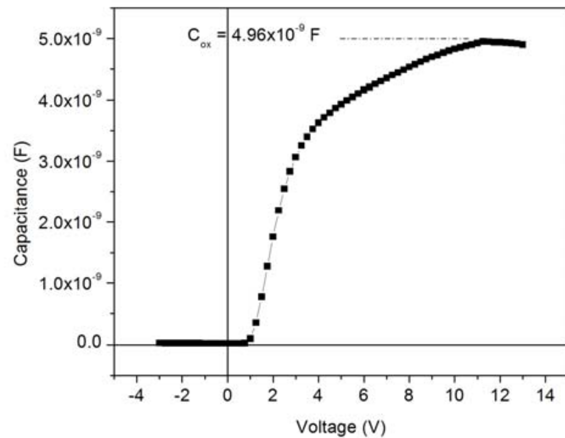

Fig. 4 Capacitance-voltage measurements of Al/TDTBPPCu/n-Si hetero-junction at 1.0 MHz

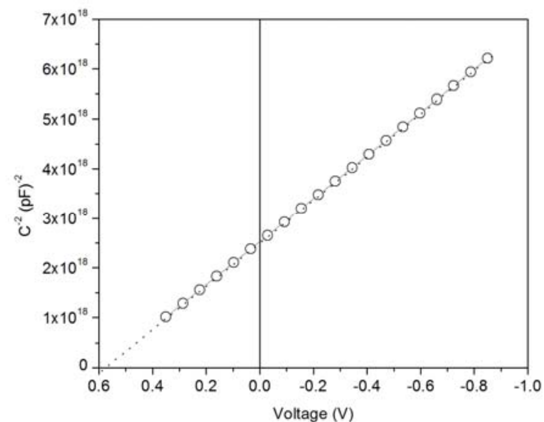

Fig. 5 C^{-2} vs. V plot of Al/TDTBPPCu/n-Si/Al hetero-junction

IV. Conclusions

In conclusion, we have successfully fabricated Al/TDTBPPCu/n-Si/Al junction diode. The different electronic parameters have been calculated by current-voltage and capacitance-voltage measurements. The characteristics of the junction show good rectifying behavior which indicates the potential of TDTBPPCu for electronics applications.

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