

Influence of Measurement System on Negative Bias Temperature Instability Characterization: Fast BTI vs Conventional BTI vs Fast Wafer Level Reliability

Vincent King Soon Wong, Hong Seng Ng, Florinna Sim

Abstract—Negative Bias Temperature Instability (NBTI) is one of the critical degradation mechanisms in semiconductor device reliability that causes shift in the threshold voltage (V_{th}). However, thorough understanding of this reliability failure mechanism is still unachievable due to a recovery characteristic known as NBTI recovery. This paper will demonstrate the severity of NBTI recovery as well as one of the effective methods used to mitigate, which is the minimization of measurement system delays. Comparison was done in between two measurement systems that have significant differences in measurement delays to show how NBTI recovery causes result deviations and how fast measurement systems can mitigate NBTI recovery. Another method to minimize NBTI recovery without the influence of measurement system known as Fast Wafer Level Reliability (FWLR) NBTI was also done to be used as reference.

Keywords—Fast vs slow BTI, Fast wafer level reliability, Negative bias temperature instability, NBTI measurement system, metal-oxide-semiconductor field-effect transistor, MOSFET, NBTI recovery, reliability.

I. INTRODUCTION

IN recent years, NBTI has been known as a major reliability concern in silicon integrated circuits due to the result of device scaling and increased chip operating temperatures [1]. This degradation mechanism occurs whenever a pMOSFET is biased with negative gate voltages, or in inversion, at elevated temperatures. The implication of this damaging mechanism is a negative V_{th} shift which makes the device much more difficult to be switched on as well as the degradation of its trans-conductance [2]. However, to successfully describe or measure the NBTI performance of a device is not straight-forward due to a regaining mechanism known as NBTI recovery.

NBTI recovery had always been a challenging roadblock in a device's NBTI characterization. The implication of recovery results in failure to accurately quantify the NBTI performance of a particular device. To date, the correlation between recovery and total V_{th} shift is still at a controversial point which demands for unambiguous explanation so as to formulate a reliable recovery model [3]. Therefore, it is of absolute importance to suppress NBTI recovery effect so as to effectively compute device NBTI reliability. From previous

Vincent King Soon Wong, Hong Seng Ng, and Florinna Sim are with the Quality Reliability Engineering Department, X-FAB Sarawak Sdn. Bhd. 1, Silicon Drive, Sama Jaya Free Industrial Zone, 93350, Kuching, Sarawak, Malaysia. (Phone: +60 82-354 888; fax: +60 82-363 330; e-mail: Vincent.Wong@xfab.com, HongSeng.Ng@xfab.com, Florinna.Sim@xfab.com).

studies, it was found that NBTI recovery is directly proportional to the delays in the measurement system [13], so one of the right solutions is to employ fast measurement system. Fast systems minimize the hardware switching delays, thereby providing instantaneous or as-quick-as-possible measurement results which are much more closer to the actual performance and with the slightest influence of NBTI recovery.

The following part of this paper shows a brief introductory to NBTI and the severe implications of NBTI recovery. Next the paper highlights one particular methodology of subduing NBTI recovery impact in NBTI investigation which is the minimization of measurement system delays. A comparison was done in between conventional and fast NBTI measurement systems to demonstrate the severity of system delays and recovery. Lastly FWLR NBTI was also included as a reference and contrast from a non-measurement system related approach.

II. WHAT IS NBTI?

NBTI is a significant reliability phenomenon that is concerned with the gate insulator of a pMOSFET. Discovered in the 1960s, it was only then recognized as a prevailing reliability matter in the late 1990s when scaled CMOS technologies are at its peak [1].

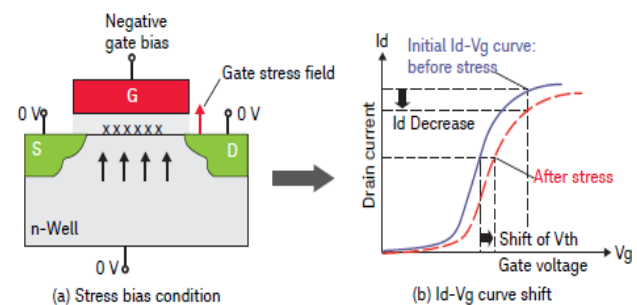


Fig. 1 NBTI degradation in PMOSFETs [4]

To this day the exact physical mechanism of NBTI behavior is still debatable and not entirely clear. It is almost universally ascribed to the creation of interface trapped and oxide charges by the applied negative bias at the gate oxide of the pMOSFET along with elevated temperature [1].

The phenomenon is prevalently attributed to the Reaction-Diffusion (R-D) NBTI model. The combination of electric field, temperature and holes break the Si-H bonds at the silicon dioxide (SiO_2) gate oxide and the silicon (Si) substrate

interface which results in a dangling bond of Si thereby creating an interface state (reaction of R-D model) in addition to a positive oxide charge of hydrogen ion (H^+) [5]. The generated positive ion diffuses into the oxide (diffusion of R-D model) and interferes with the carriers which lead to the decreasing of drain current (I_d) and shifting V_{th} as shown in Fig. 1.

Experimental results also concluded that NBTI degradation severity is directly proportional to the temperature while in chorus inversely proportional to the gate oxide thickness. This means that the latest or advanced semiconductor processes nowadays which targets mainly high temperature applications and scaling down to the submicron levels are intensely impacted by this mechanism [4].

III. NBTI RECOVERY

Conventionally NBTI investigation comprises the repetition of two main stages which is the stressing stage and the measurement stage. Stressing stage involves transistor gate terminal stressing with certain voltage sources for a specified period before moving into the measurement stage which removes the gate stressing during the stressing stage to initiate the voltage sweep so as to obtain the device characteristic or IV curve and extract the V_{th} at constant current [6]. The process is repeated until the targeted stressing period was achieved. However the delay during the transition between these two stages causes a regaining phenomenon known as NBTI recovery [7].

NBTI measurement recovers almost instantaneously once the stress is lifted. The magnitude of recovery is directly proportional to the delay induced from the transition which is also known as the relaxation period. Therefore, longer relaxation periods or larger recovery tends to form underestimation of the NBTI degradation during electrical measurements [8], causing the particular device characterization to overestimate its lifetime or reliability. Ershov et al. [9] suggest that NBTI degradation involves two elements: a permanent element that remains after the stress had been lifted and a reversible element that recovers after lifted stress. Huard et al. [10], on the other hand, found partial recovery while Rangan et al. [11] obtained complete recovery with the device back to its original state after removed stress. Nonetheless all of them attributed interface trap generation plus positive ion or hole trapping to NBTI degradation phenomena and that NBTI recovery to be resulted from the hole trapping.

Fig. 2 depicts an investigation on NBTI recovery demonstrating the influences of relaxation periods on device degradation. Relaxation period infers to the period of time whereby the gate bias stressing was removed. The experiment involves two different lengths of relaxation period which is 10 seconds and 100 seconds. It can be observed that the longer the relaxation period, the greater the "drop" in the V_{th} degradation percentage. Hence it can be comprehended that different relaxation periods induce different extent of recovery; with longer relaxation period experiencing greater recovery in measured NBTI degradation. Consequently, the larger the delay or relaxation period within a measurement system, the smaller it is the measured device NBTI degradation; thus

overestimating the lifetime as well as device reliability and ultimately projecting incorrect perception of a robust technology.

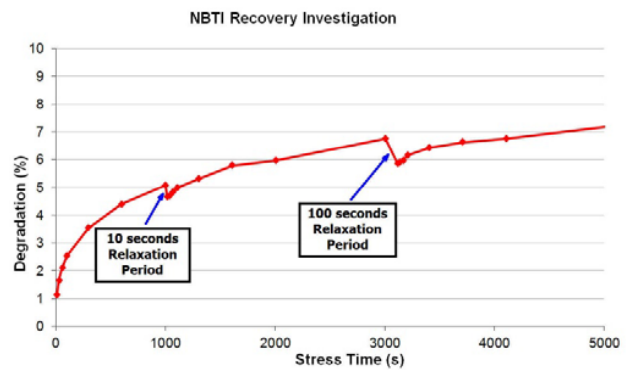


Fig. 2 Impact of relaxation period on NBTI degradation

IV. NBTI MEASUREMENT SYSTEM

Referencing to the Jecdec Standards [12], minimizing the interim off-stress time ($T_{off-stress}$) measurement between the termination of the NBTI stress and the beginning of device parameter measurements is recommended to reduce the effect of NBTI recovery. Therefore, the speed of NBTI measurement system is the utmost vital aspect to be emphasized. Fast measurement systems are preferable so as to clearly understand the NBTI capability of a device. Fast measurement system minimizes the transition period when the switching between stressing and measuring stage happens, thereby subduing the relaxation period and hence the recovery effect. This results in better quantifying the NBTI characteristic of the particular device as near as possible to its actual performance.

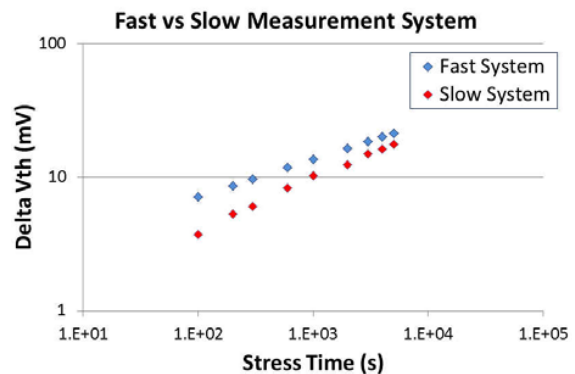


Fig. 3 Measurement system differences

Fig. 3 shows the contrast in between fast and slow measurement systems. Fast system simply implies minimum delay and NBTI recovery effect, and so produces contrastingly higher NBTI degradation reading compared to slow conventional system. These readings also deviate less than the actual device performance compared to slow measurement results. For that reason in order to successfully characterize a technology as close as possible to its original performance, it is

important to employ fast measurement systems to suppress NBTI recovery. However, one of the trade-off of fast measurement system is they tend to incur much more cost than conventional systems. Moreover applying conventional slow systems also does not directly imply totally inaccurate or inefficient measurement. This is because by prolonging the testing period on a slow system, the slope of the V_{th} degradation will approach towards the resolution of a fast measurement system as demonstrated in Fig. 4 [13]. In Fig. 4, the fast measurement system plot has a slope of 0.28 whereas the slow measurement system has a slope of 0.27. Such phenomenon occurs due to the severity of NBTI recovery mechanism in the earlier stages of a slow measurement system. By extending the testing period in a slow system up until the degradation slope saturates or does not further change as shown in Fig. 4, the slope resolution of a fast system can also be achieved. Nonetheless, as shown in Fig. 4, a slow system takes approximately 360,000 seconds measurement in order to reach the resolutions of a 5,000 seconds measurement done by a fast system. Therefore, it is definitely unfeasible unless testing capacity can be compromised.

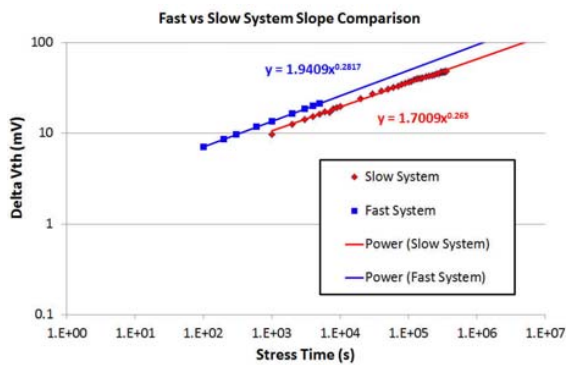


Fig. 4 Slope comparison in between fast and slow measurement systems

V. FWLR NBTI

FWLR NBTI refers to wafer level NBTI reliability investigations done at a rapid manner without the need of fast measurement system. There are a number of techniques to execute FWLR NBTI for instances “On-the-fly” (OTF) method, “fast V_{th} ” method and Recovery Correction Method (RCM). OTF method is one of the most popular techniques for NBTI measurement without recovery due to its equipment simplicity [14]. No interruption happens but V_{th} degradation has to be determined through modelling. The underside of OTF method is the initial pre-stress measurement is also taken at an already degraded device under the high gate voltage and the V_{th} shift after the subsequent stress is underestimated [15]. “Fast V_{th} ” method on the other hand is an improved version of the OTF method with the capability of very fast measurement of initial V_{th} down to 1 μ s. This is done by measuring the pre-stress drain current (I_d) and V_{th} through fast I_d - V_g measurement technique [15]. However interruption of stress happens and it is very difficult to be implemented due to it

special hardware requirements.

Alternatively a different technique that was implemented in this investigation is the RCM method which has been developed internally at X-FAB Semiconductor Foundries. Through this method, interruption of stress still occurs but the unrecovered V_{th} is extrapolated using the recovery function obtained via curve fitting. This method can be easily implemented with any standard reliability test system and special hardware is unnecessary. Using similar silicon wafer material, an investigation was done to demonstrate the influence of measurement system with reference to FWLR RCM method. Pre-measurements were done in order to obtain the necessary data needed for the FWLR RCM curve-fitting. Results are as shown in Fig. 5.

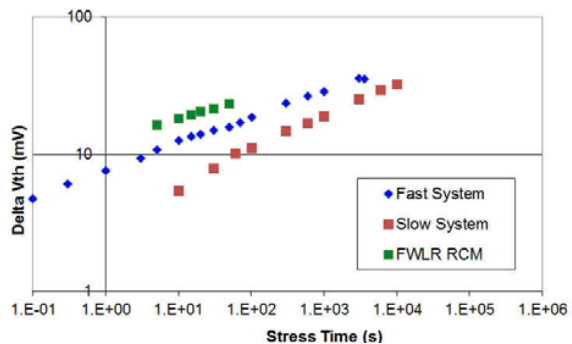


Fig. 5 Fast vs slow system with reference to FWLR RCM

It can be observed from Fig. 5 that fast measurement systems still acquires contrastingly different readings compared to normal slow systems. On the other hand, FWLR RCM method obtained even higher degradations compared to fast measurement systems. It cannot be concluded either fast measurement system or FWLR RCM acquired the correct or the closest to actual device NBTI degradation since recovery still happens in fast systems and FWLR RCM might have overestimated the degradation. However with further fine-tuning, the non-measurement system related approach of curve-fitting to acquire the unrecovered V_{th} , proved to be able to subdue the impact of NBTI recovery even with conventional NBTI test systems.

VI. CONCLUSION

As a conclusion, NBTI degradation mechanism is an acute reliability concern to date, especially with the chip-shrinking trend as well as the 2D to 3D integration density scaling in the near future. Therefore it is vital to be able to successfully characterize the NBTI performance of a device so as to discern its reliability in the application field. This paper illuminates the vast differences in between slow conventional and fast NBTI measurement systems, with the latter demonstrated to significantly influence the end result of a successful device NBTI characterization. The key point is to suppress the effect of NBTI recovery mechanism which can be done through the employment of fast measurement systems as well as FWLR NBTI. Even so, slow measurement systems can still produce

comparable results although there is a need of compromising effort and resources.

REFERENCES

- [1] Schroder, D. K. (2007). Negative bias temperature instability: What do we understand?. *Microelectronics Reliability*, 47(6), 841-852.
- [2] Rauch, S. E. (2002). The statistics of NBTI-induced V_T and β mismatch shifts in pMOSFETs. *IEEE transactions on device and materials reliability*, 2(4), 89-93.
- [3] Aichinger, T., Nelhiebel, M., & Grasser, T. (2009, April). Unambiguous identification of the NBTI recovery mechanism using ultra-fast temperature changes. In 2009 IEEE International Reliability Physics Symposium (pp. 2-7). IEEE.
- [4] Agilent Technologies, "Agilent B1500A Semiconductor Device Analyzer - Ultra-Fast 1 μ s NBTI Characterization Using the Agilent B1500A's WGFMU Module," Application Note B1500-10, 5989-9963EN, 2008.
- [5] Nishimura, T. (2013). Solve MOSFET characteristic variation and reliability degradation issues. *Electronic Design News (EDN)*, 177-180.
- [6] Jeduc Standard JESD241 "Procedure for Wafer-Level DC Characterization of Bias Temperature Instabilities"
- [7] Chiu, J. P., Liu, Y. H., Hsieh, H. D., Li, C. W., Chen, M. C., & Wang, T. (2013). Statistical Characterization and Modeling of the Temporal Evolutions of Distribution in NBTI Recovery in Nanometer MOSFETs. *IEEE Transactions on Electron Devices*, 60(3), 978-984.
- [8] Yang, J. B., Chen, T. P., Tan, S. S., & Chan, L. (2006, July). A novel empirical model for NBTI recovery with the modulated measurement time frame. In 2006 13th International Symposium on the Physical and Failure Analysis of Integrated Circuits (pp. 33-36). IEEE.
- [9] Ershov, M., Saxena, S., Karbasi, H., Winters, S., Minehane, S., Babcock, J.,... & Shibkov, A. (2003). Dynamic recovery of negative bias temperature instability in p-type metal-oxide-semiconductor field-effect transistors. *Applied physics letters*, 83(8), 1647-1649.
- [10] Huard, V., Denais, M., & Parthasarathy, C. (2006). NBTI degradation: From physical mechanisms to modelling. *Microelectronics Reliability*, 46(1), 1-23.
- [11] Rangan, S., Mielke, N., & Yeh, E. C. C. (2003, December). Universal recovery behavior of negative bias temperature instability [PMOSFETs]. In *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International* (pp. 14-3). IEEE.
- [12] Jeduc Standard JESD90 "A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities"
- [13] WONG, V. K. S., NG, H. S., & Sim, P. C. (2015, December). Impact of NBTI Recovery, Measurement System and Testing Time on NBTI Lifetime Estimation. In 2015 International Conference on Advanced Manufacturing and Industrial Application. Atlantis Press.
- [14] Aono, H., Murakami, E., Shiga, K., Fujita, F., Yamamoto, S., Ogasawara, M.,... & Kubota, K. (2008, April). A study of SRAM NBTI by OTF measurement. In 2008 IEEE International Reliability Physics Symposium (pp. 67-71). IEEE.
- [15] Shen, C., Li, M. F., Foo, C. E., Yang, T., Huang, D. M., Yap, A., ... & Yeo, Y. C. (2006, December). Characterization and physical origin of fast V_{th} transient in NBTI of pMOSFETs with SiON dielectric. In 2006 International Electron Devices Meeting (pp. 1-4). IEEE.