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Highly Optimized Novel High Speed Low Power Barrel Shifter at 22nm Hi K Metal Gate Strained Si Technology Node

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***Abstract*—**This research paper presents highly optimized barrel shifter at 22nm Hi K metal gate strained Si technology node. This barrel shifter is having a unique combination of static and dynamic body bias which gives lowest power delay product. This power delay product is compared with the same circuit at same technology node with static forward biasing at 'supply/2' and also with normal reverse substrate biasing and still found to be the lowest. The power delay product of this barrel sifter is .39362X10-17J and is lowered by approximately 78% to reference proposed barrel shifter at 32nm bulk CMOS technology. Power delay product of barrel shifter at 22nm Hi K Metal gate technology with normal reverse substrate bias is 2.97186933X10-17J and can be compared with this design's PDP of .39362X10-17J. This design uses both static and dynamic substrate biasing and also has approximately 96% lower power delay product compared to only forward body biased at half of supply voltage. The NMOS model used are predictive technology models of Arizona state university and the simulations to be carried out using HSPICE simulator.

***Keywords*—**Dynamic body biasing, highly optimized barrel shifter, PDP, Static body biasing.

I. Introduction

RESEARCHERS are exploring low power and high speed areas including subthreshold regions [1]

A barrel sifter is a circuit, digital by nature. It can shift data word by given or specified number of bits in single cycle. This is implemented as a sequence of multiplexer (Mux). In this implementation, the input of next multiplexer is connected to output of one multiplexor. All this connected in such way that is dependent on shift distance.

It has n data inputs, and n data output. Also it has set of inputs which are control input that tells how to shift the data in input and output. If a barrel sifter is a part of a microprocessor CPU, it can tell the direction of a shift (left or right), the type of shift weather logical, arithmetic or circular. Also it can tell, the amount of shift, be it 0 to n -1 bits or 0 to n bits [2].

Barrel shifter is required in many applications e.g. floating point adder, variable length coding and bit indexing. Barrel shifters are very common in both digital signal processor and general purpose processor. Mux tree is designed with the help of 2:1 mux as a basic building block. Shifter is an important module in DSP and graphics [3]. New approach has been presented for synthesis of a fast barrel shifter, which is useful with reduced delay but not much increased area [4].

In many important operations from address decoding to computer arithmetic with basic operation of rotations and data shifting, barrel shifter is one of the primary data path. In [3] 0.6 μm technology is used to design and implement mux based barrel shifter. In this N well CMOS process is used, which uses three different logic design style. The styles are static cmos, transmission gate (TG) cmos and dual rail domino cmos logic. In this [3] paper, the barrel shifter shows a lowered propagation delay while average power remaining the same. A comparison is done using three logic design styles for different characteristics parameters like circuit delay, average power, maximum-minimum instantaneous power etc. etc.

II. Review

According to this patent, Fig. 1 [5], high speed barrel shifter is having or shifter array which has a matrix of transistor located at intersection of rows and columns of the matrix. Alternatively the rows and columns work as source and destination terminals. Within the shifter array, the barrel shifter can perform till instruction, which are data dependent and so barrel shifter avoids extra clock attached with post array processing. Top right portion of the matrix is separated from the bottom left portion alongside a diagonal, by isolation portion in one embodiment. Transistors in bottom left portion which are for rotates and fills get isolated by isolation portion. It gets isolated from top right portion. This is associated with shifts in accordance to the direction of shift.

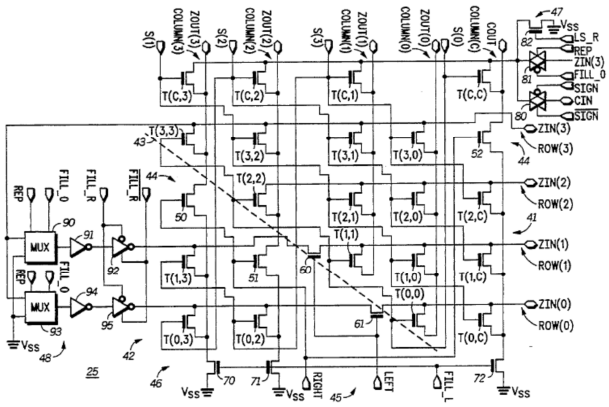

Fig. 1 Dang and Anderson patent circuit

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According to another invention, Fig. 2 [6], a bidirectional shifter has MXN matrix of selector. In MXN selector, M is arranged in the direction of column, according to shift amount and N in the row direction in accordance to the length of data which can perform a right (or left) shift in accordance to the data indicating right shift amount. With this a barrel shifter of a right shift is able to shift the data in right and left as desired.

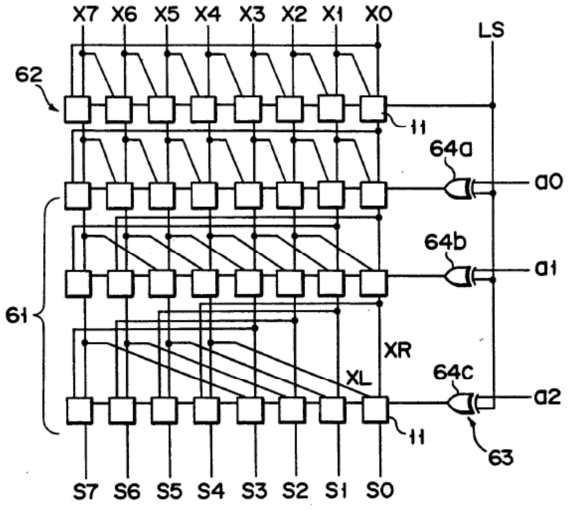

Fig. 2 Yamaguchi patent circuit

Multiply or divide IC or barrel shifter, Fig. 3 [7] comprises of plurality of serial stages. Number of bits determines the number of stages in an input digital data word. Digital data word at the input if chosen, then each stage in sequence given for a different power of two rotary or multiply/divide shift. In accordance to shift amount select command, a mux in each stage chooses as an output either digital shifted data word or input data word (digital) for output to the next stage. In each stage logic could be included to know if the shift operation is rotary or multiply or divide operation.

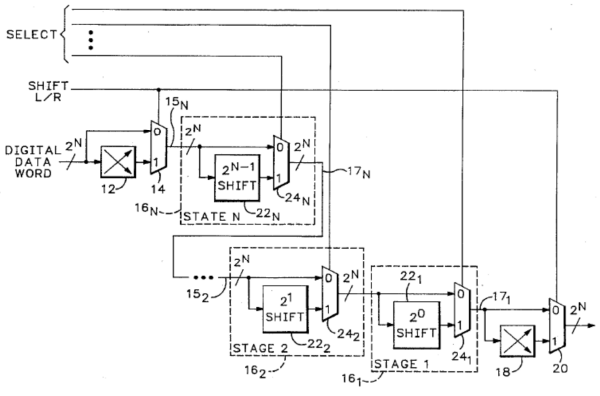

Fig. 3 Seckora patent circuit

In [8], Fig. 4, an invention to control an N bit barrel shifter to shift the input word's bits by a shift value is presented. The method involves performing 1's complement of M bit binary representation of a shift value in order to generate and input when first direction is taken by shift direction. And this binary representation of shift value is passed on as input when shift direction gets second direction. It involves decoding the input in to 2^m control signals. With this it generates many groups of control signals from 2^m control signal, it's control activation for the barrel shifter is done by selecting one of the many groups of control signal.

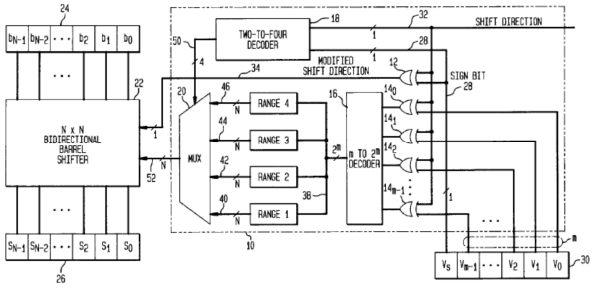

Fig. 4 Diamond Stein, Sriniwas patent circuit

III. Working

Circuit in [2] is taken as the experimental circuit and the results are compared with the 32nm mosfet bulk technology. In this setup the circuit was simulated with traditional reverse body bias, static Forward body bias and also simulated with combination of static and dynamic body bias. In dynamic body bias the substrate is connected with the input control signal. In all the cases the results were compared with each other.

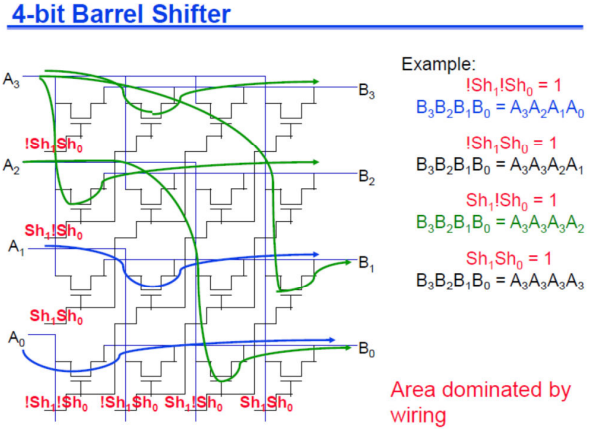

Fig. 5 Barrel shifter

All the transistors were given dynamic body bias except M21, M12, M1, M03, M02, M01 transistor where they were given static forward body biasing of Vdd/2(Vdd at 0.9 V).M21 means 2nd row and 1st column transistor, M12 means 1st row and 2nd column transistor etc etc. 0th row is the bottom most row and 0th column is the left most column.

Following is the waveform of the barrel shifter with combination of dynamic and static body biasing, in which A3

is given high voltage. According to the control signals SH1 SH0, output signals B3, B2 etc go high one by one.

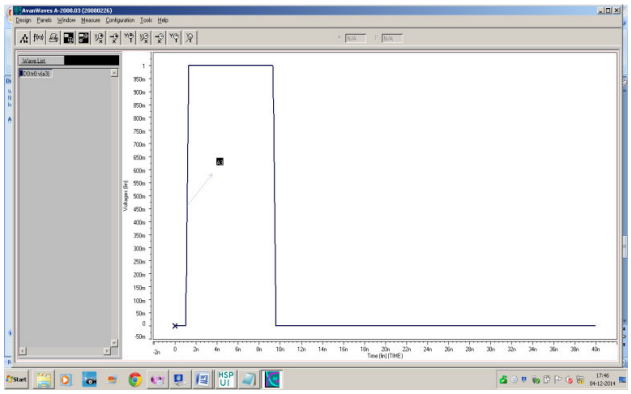

Fig. 6 A3 input signal goes high

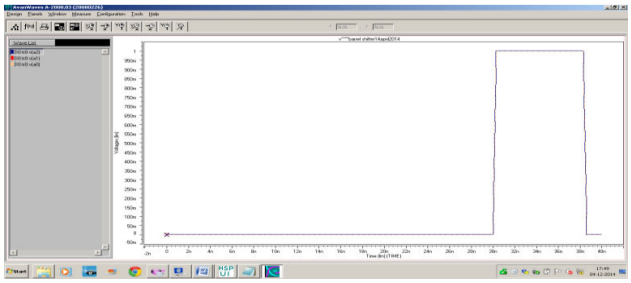

Fig. 7 A2, A1, A0 input waveforms

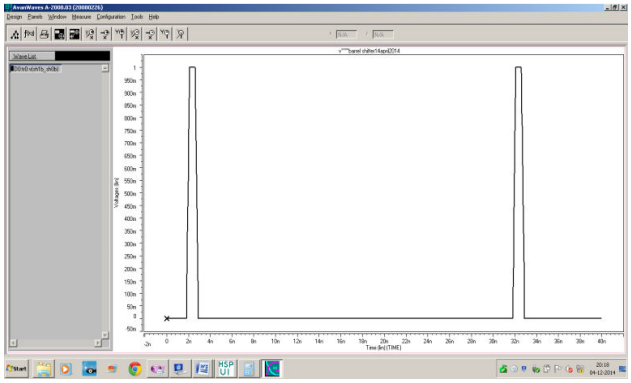

Fig. 8 SH1bar SH0bar going high

Figs. 8 to 11 show the four control signal SH1 SH0 going high one by one, starting with sh1Bar sh0bar high, thenSh1bar Sh0high and so on.

The first row of the Table I shows the results of the experimental circuit of this research paper. In this, the combination of dynamic and static body bias is used. All the transistor being NMOS, the output high of B3, B2 etc is not VDD (or supply voltage) but near to the threshold voltage of NMOS transistor. The delay in Sec is the propagation delay and is smallest compared to all the delays. Also the power, which is the average power of this research paper's proposed circuit, with combination bias is higher compared to reverse body bias in total. Dynamic and static body bias, both are responsible for the increased average power of row1 of the Table I.

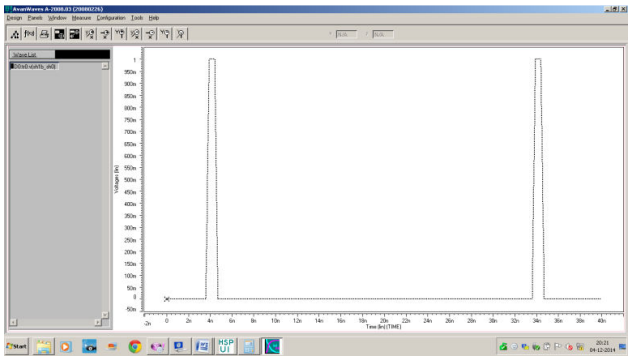

Fig. 9 SH1bar SH0 going high

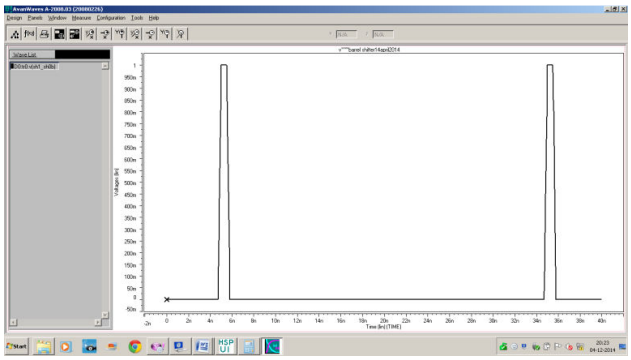

Fig. 10 SH1 SH0bar going high

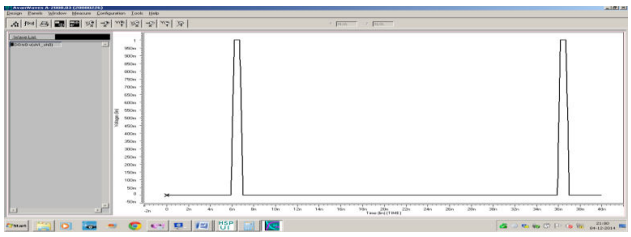

Fig. 11 SH1 SHO going high

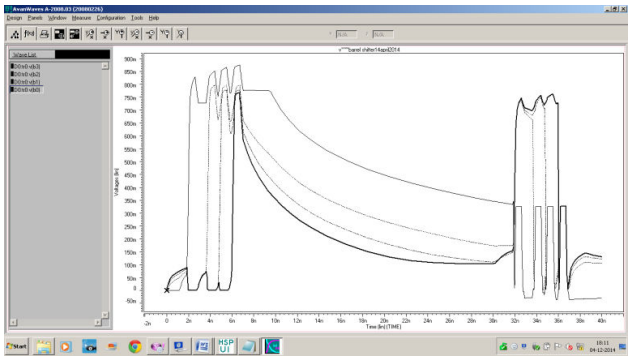

Fig. 12 The output waveforms B3, B2, B1, B0 going high in response to control signals and A3 being high

TABLE I
POWER DELAY PRODUCTS AT 22NM AND 32NM TECHNOLOGY NODES

Delay Sec[1]		Power W[2]	PDP(J[3])
Self proposed 22nm mosfet optimized barrel shifter with Dynamic Body Biasing n Static Body Biasing combination	3.8431E-12	1.0244E-06	l.39362X10-17
Self barrel shifter at 22nm technology. With static FBB=.45V	6.545X10-12	1.1756X10-6	.769912X10-17
Self barrel shifter at 22nm technology with normal reverse Body Biasing	3.1973X10-11	9.3137X10-7	2.9779X10-17
proposed[4]32nm barrel shifter	10X10-12	0.845X10-6	.84X10-17
barrel shifter 32nm[4] mosfet-existing	40.4X10-12	3.04X10-6	12.2816X10-17

[1] sec=second, [2]W=watts, [3]J=joule

The second row is the static forward biased barrel shifter and it's results of delay and average power happen to fall between the first row of novel combination circuit and third row of normal reverse body biased circuit's result. All first three rows are at 22nm High-K Metal gate strained Si Technology node.

The last two rows are at 32nm CMOS bulk Technology nodes and hence for obvious reasons of being at 32nm technology node , their results are bad compared to 22nm Technology node results of 'power delay product' as either delay gets reduced or power gets reduced with advanced technology node.

IV. CONCLUSION

The highly optimized barrel shifter with unique combination of static substrate forward biasing and dynamic substrate biasing has smallest power delay product. It's value of Power delay product is .39362X10-17 against the power delay product of the same circuit at 22nm Hi K metal gate strained Si technology, with normal reverse biased substrate, which is 2.9779X10-17. It was also compared with referenced proposed [4] Barrel Shifter at 32nm cmos bulk technology and found to be less by 78%. The combinational set up power delay product is less by 96% as compared to static forward body biased at 22nm Hi K Metal gate technology in which 0.45V(half of 0.9Vdd –supply voltage) of static bias was applied.

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Shobha Sharma has done her Master of Engineering from B.I.T.S Pilani. She is an associate member of IEEE and published 16 research papers in international and national journals and conferences. Her main area of research is low power and high speed VLSI circuits.

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