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High Level Characterization and Optimization of Switched-Current Sigma-Delta Modulators with VHDL-AMS

A. Fakhfakh, N. Ksentini, M. Loulou, N. Masmoudi, and J. J. Charlot

***Abstract*—**Today, design requirements are extending more and more from electronic (analogue and digital) to multidiscipline design. These current needs imply implementation of methodologies to make the CAD product reliable in order to improve time to market, study costs, reusability and reliability of the design process.

This paper proposes a high level design approach applied for the characterization and the optimization of Switched-Current Sigma-Delta Modulators. It uses the new hardware description language VHDL-AMS to help the designers to optimize the characteristics of the modulator at a high level with a considerably reduced CPU time before passing to a transistor level characterization.

***Keywords*—**high level design, optimization, switched-Current Sigma-Delta Modulators, VHDL-AMS.

I. Introduction

THE need for new analogue synthesis techniques that would be able to support a future high-level mixed-signal synthesis environment is increasing along with the advancement in technology and the evolution of commercial requirements. The emergence of VHDL-AMS since 1999 [1] has provided a platform which can form the basis for high-level analogue and mixed-signal synthesis systems. Many efforts are focused on the development of new methodologies to integrate the Top-Down hierarchical design flow in a synthesis environment using VHDL-AMS [2]-[3]. We are still far from the achievement of this objective; however, designers can profit from the several opportunities offered by the standard VHDL-AMS when designing mixed analogue and digital systems.

So far, electrical simulators like SPICE or ELDO have been the most widely used simulation tools. Abstraction level is low and accuracy level is high since accurate device models are used. However, CPU time grows with the circuit size and the type and length of simulation. There is no doubt that electrical simulation is the logical choice for simulating basic cells. The situation changes considerably when dealing with more complex subsystems, like data converters.

To avoid too lengthy electrical simulations of analogue circuits, a higher level of abstraction is required. An immediate solution is the use of macro-models of the basic cells. But, although the problem is simplified, CPU times are still too long because equation formulation is still based on a set of differential equations which must be solved by numerical integration using millions of time steps [4].

A most efficient solution consists of using behavioral simulation. This approach requires the circuit to be partitioned into basic blocks and described by using a behavioral description language. A set of explicit expressions relates the output variables with the input and internal state variables of each block. Thanks to this high level description approach, behavioral simulators are able to perform long transient analysis in reasonable CPU times while maintaining a satisfactory accuracy level. Another reason for the use of higher levels of abstraction is related to the possibility of the achievement of an optimum architectural choice before passing to a transistor sizing [5].

Switched-current technique (SI) has been highly used to implement Sigma-Delta modulators and analogue-to-digital converters because it allows a reduction of voltage supply and power consumption [6]-[7]-[8]. However, such systems require a relatively very long CPU time which make difficult a design optimization at the transistor-level. The proposed methodology in this work makes possible an accurate characterization and optimization of SI systems at a high level design. In addition, it facilitates the designer work by proposing generic VHDL-AMS models, easily adaptable when system specifications are modified.

This paper is outlined as follows. In section 1, we describe the proposed design methodology. In section 2, we detail the development of a VHDL-AMS description of an SI cell. Section 3 details the SI cell optimization. In section 4, we describe a high level simulation and characterization of an SI Sigma Delta modulator. Section 5 draws a conclusion.

N. Masmoudi, Laboratory of Electronics and Technology's Information, National School of engineers in Sfax, B.P. W. 3038 Sfax Tunisia (phone: +216 74274088; fax: +216 74275595; e-mail: nouri.masmoudi@enis.rnu.tn).

A. Fakhfakh, High Institute of Electronics and Communication of Sfax (ISECS), B.P. 868, 3018, Sfax, Tunisia. He is member of the Laboratory of Electronics and Technology's Information, National School of engineers in Sfax (e-mail: ahmed.fakhfakh@isecs.rnu.tn).

N. Ksentini, High Institute of Electronics and Communication of Sfax (ISECS), B.P. 868, 3018, Sfax, Tunisia. She is member of the Laboratory of Electronics and Technology's Information, National School of engineers in Sfax (e-mail: nisrine.kossentini@yahoo.fr).

II. Description of the Analog Design Approach

When designing data converters, designers generally start with behavioral simulations to achieve a verification of the converter performances. Then, they go down in the hierarchical design flow to do physical simulations. Data converters generally contain both analogue and digital parts which make difficult to achieve physical simulations with a single simulator. Many design approaches have been proposed in the literature.

For example, the design approach presented by R. Maghrebi [9] was applied to design multi ramp A/D converters. The digital part was described with VHDL, whereas the analogue part represented by a current controlled oscillator was described at the transistor level and simulated with ELDO. In V. K. Navin *et al.* works, authors have developed with C language a simulator to simulate pipeline CANs. Compared to MATLAB performances, the simulations require a less CPU time [10]. M. K. Mayes *et al.* used the Verilog hardware description language to model the pipeline CANs [11] (Verilog is suited to a digital system description) whereas B. Murmann used Verilog-A hardware description language [12] (Verilog-A is suited to an analogue system description). R. Isak *et al.* have designed a 12 bit A/D converter with switched capacitance technique. They used SpectreHDL hardware description language [13].

Since 1999, the new hardware description language standard VHDL-AMS offers the possibility to simulate both analogue and digital parts in a same environment. Our idea was to explore the techniques of virtual prototyping using VHDL-AMS in order to suitably simulate the behavior of Switched-Current systems with different abstraction levels. Also, we tried to develop a flexible system, containing reusable building with several blocks called IP. More than that, a library of virtual components at various abstraction levels was made up and implemented in order to reinforce the developed methodology. Figure 1 summarizes the various steps of the hierarchical design cycle developed in this work.

A VHDL-AMS library was developed containing behavioral models for SI cell, quantizer and DAC converter. These blocks are required to design SI Sigma Delta modulators. To obtain an accurate SI cell high level model, the last was extracted from a transistor schematic simulation as detailed in following.

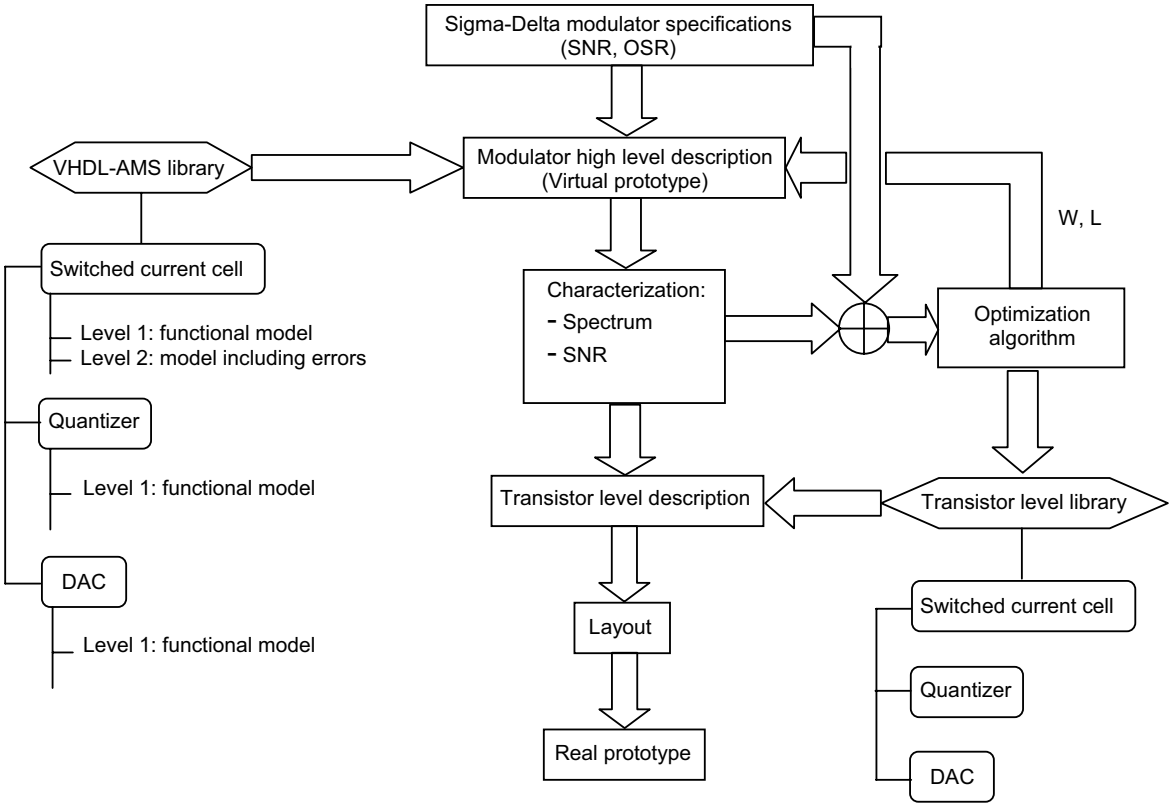

Fig. 1. Diagram of the hierarchical design flow

The designer starts by defining the specifications of the Sigma-Delta modulator, especially its SNR and OSR. Then he exploits the VHDL-AMS library to develop a structural description for the modulator. After a high level simulation, it is possible to do a characterization to draw the output spectrum and determine the SNR. This important characterization is hardly obtained with a transistor-level simulation because of the extremely long required CPU time.

If the obtained results do not suit specifications, an optimization algorithm is applied at the behavioral level to perform new transistor sizes (W and L). If a satisfactory result is finally obtained, each SI cell composing the modulator is replaced by a transistor-level netlist from an updated transistor-level library. The designer then passes to a transistor-level simulation to draw the output spectrum and verify the SNR. At this step, he starts by an already optimized transistor sizes. Consequently, a really shorter design time is required to achieve a transistor level characterization and optimization before developing a layout and manufacturing a real prototype

II. VHDL-AMS DESCRIPTION OF THE SI CELL

The switched-current technique has been highly used to implement Sigma-Delta modulators, particularly cascode second order modulators, composed of two integrators, a quantizer and a one bit D/A converter, as detailed on figure 2. An SI memory cell is ideally modeled by a delay line of a half clock period: $I_{out}(z) = -z^{-\frac{1}{2}} I_{in}(z)$. To achieve the function Z^{-1}, we generally use two cascaded SI cells.

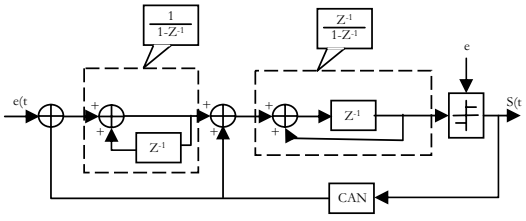

Fig. 2 Second order Sigma-Delta modulator block diagram

A formal computation software such as MATLAB SIMULINK is usually used to validate new design architecture. When it is a question of real integration, hardware description languages are more adapted before passing to a transistor level simulation. Our approach consists of extracting an accurate VHDL-AMS description from a transistor schematic simulation as detailed on figure 3. After a transistor level simulation, optimized transistor sizes (W and L) are performed and injected in the VHDL-AMS description.

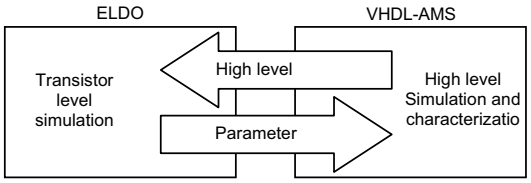

Fig. 3 Modeling approach

Many SI generations have been proposed in the literature. We have studied and optimized the class AB grounded gate memory cell which presents many advantages [14]-[15]. Its transistor schematic is shown on figure 4. It is composed of two memorization transistors (Mp and Mn) controlled by switch transistors (represented by Φ1 and Φ2) and performs the function of a current copier circuit.

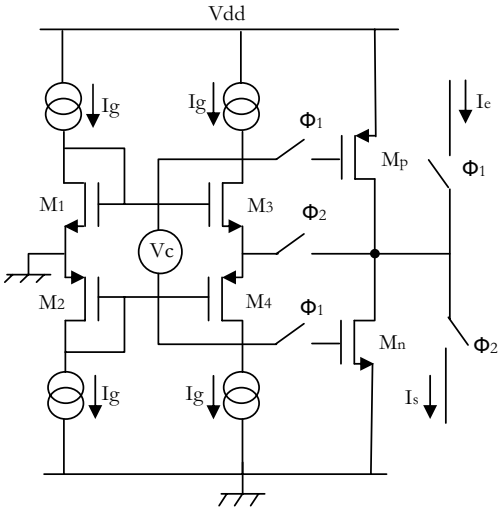

Fig. 4 Class AB switched current cell

To develop a VHDL-AMS description of the cell, the last has been simulated at the transistor level with ELDO simulator. Optimized sizes of the different transistors composing the cell were extracted. Then a VHDL-AMS architecture that describes the SI cell was developed performing a delay of a half clock period. In addition, the SI-memory cell presents some imperfections introduced by MOS transistors; mainly setup, charge injection and output/input conductance's ratio errors [16]-[17].

With the reference of the SI cell dynamic equivalent schematic, we have extracted equations that describe the different errors [18]:

The setup error was modeled by a second order transfer function depending on transistors transconductances:

$$\frac{I_{in}}{I_{acq}} = 1 + \frac{(G_0 + g_{mg})C + g_{0g}C_g}{g_m g_{mg}} p + \frac{CC_g}{g_m g_{mg}} p^2 \qquad (1)$$

where I_{in} and I_{acq} are respectively the input and the output currents, G_0 the equivalent conductance of the memorization transistors, p the Laplace operator and:

$$g_m = g_{mN} + g_{mP} = \sqrt{2K_n I_n \frac{W_n}{L_n}} + \sqrt{2K_p I_p \frac{W_p}{L_p}} \quad (2)$$

$$g_{mg} = g_{mNg} + g_{mPg} = 2\sqrt{2K_n W_g \frac{I_g}{L_g}} \quad (3)$$

$$g_{og} = g_{0Ng} + g_{0Pg} = 2\alpha_g \frac{I_g}{L_g} \quad (4)$$

$$C_g = \left(1 + \frac{K_n}{K_p}\right)\left(2W_g L_g \frac{C_{ox}}{3}\right) \quad (5)$$

$$C = \frac{2}{3} C_{ox}\left(W_P L_P + W_n L_n\right) \quad (6)$$

The charge injection error Iinj was modelled by the following expression:

$$\Delta I_{dinj} = g_m \Delta V_{gs} = g_m \frac{Q - Q'}{C} \quad (7)$$

where

$$Q = \frac{1}{2}(V_{dd} - V_{TN} - V_x)C_{canali} + V_{dd} C \quad (8)$$

$$Q' = C_{canalf}\left(\frac{V_{dd}}{2} - V_{Tn}\right) + 2C_{recf} V_{dd} \quad (9)$$

C_{canali} and C_{reci} are respectively the channel and the covering capacities of the switch transistors.

C_{canalf} and C_{recf} are respectively the channel and the covering capacities of the phantom transistors.

The output-to-input-conductance ratio error was modeled by:

$$I_{out} = \frac{A g_{m0} g_s}{A g_{m0} g_s + G_0\left(A g_{m0} + g_s\right)} I_{mem} \quad (10)$$

where A is the amplifier gain ($A = g_{mg}/g_{0g}$).

All these mathematical equations were introduced in the architecture of a VHDL-AMS description to obtain a non ideal high level SI cell model (detailed in the appendix).

The developed architecture is organized as detailed on figure 5. It has two inputs (an input current I_{in} and a clock signal H), an output current I_{out} and some generics depending on the process parameters.

A clock period detection block is added to the architecture; so when the clock frequency changes, the VHDL-AMS description is automatically suited to the new period.

The VHDL-AMS description was simulated with Simplorer 6.0 Software [19]. Figure 6 shows the obtained transient response: a sine input current is sampled and hold at every half sampling period. A zoom on the transient response shows the effect of the introduced cell errors (figure 7).

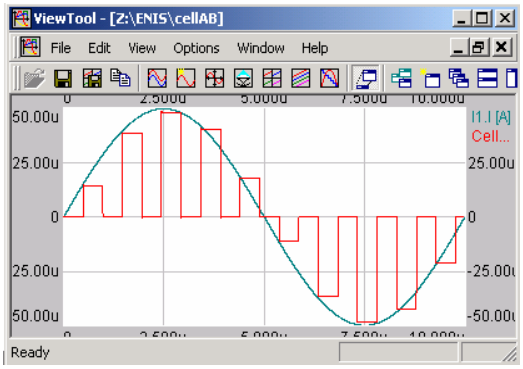

Fig. 6 High level simulation of the SI cell

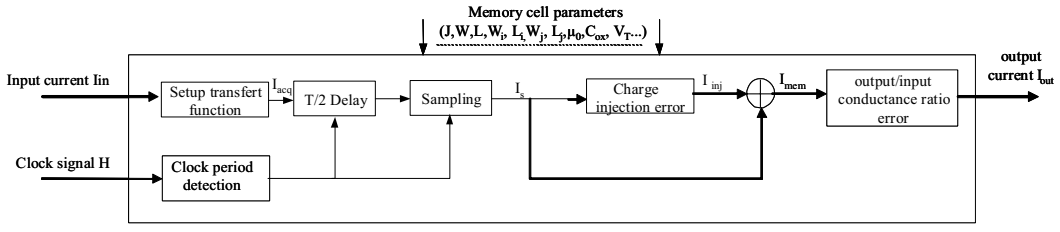

Fig. 5. Block diagram of the VHDL-AMS architecture of the memory cell

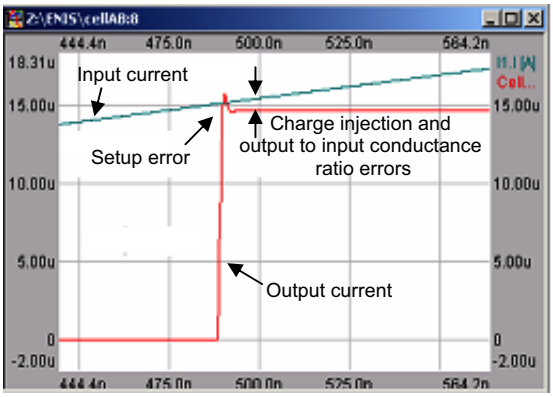

Fig. 7 Zoom on the transient response

To design a Sigma Delta modulator, we need also a quantizer and a DAC converter. The quantizer detects the integrator output sign and generates a positive or a negative quantity respectively. The DAC is a simple 1 bit converter. VHDL-AMS descriptions were developed for each block and added to the library.

III. SI Cell Optimization

Once the VHDL-AMS description of the SI cell is developed, an optimization algorithm performs optimized transistor sizes (W and L). The algorithm we used is the genetic algorithm available in Simplorer environment.

Figure 8 shows the optimization interface: at the left, the list of optimization parameters is depicted (representing sizes of the SI cell transistors and bias current). At the right, we can see the different genetic algorithm characteristics fixed as following: number of generations: 100, individuals: 10, runs: 1000, selections: 5, mutations: 5.

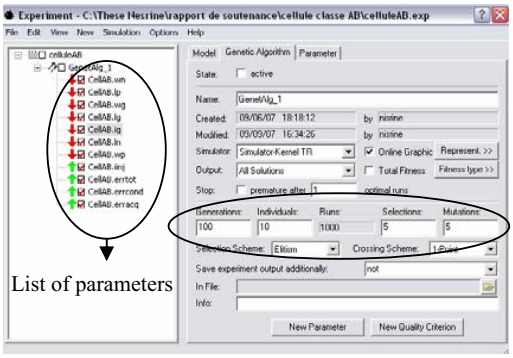

Fig. 8 Optimization interface

We have optimized both the cell error ε and its transient response τ. The objective function was defined by: $\alpha_1\tau + \alpha_2\varepsilon$ where α_1 and α_2 represent weight coefficients.

The obtained results after optimization are shown on table 1. Three cases were studied:

- Case 1: α1=0.7 and α2=0.3. In this case, we give more importance to the optimization of the transient response.
- Case 2: α1=0.5 and α2=0.5. In this case, the same weight was given to the optimization of cell error and transient response.
- Case 3: α1=0.3 and α2=0.7. In this case, we give more importance to the optimization of the cell error.

We can see in table 1 that the minimum transient response was obtained in the first case (69 ps) whereas the minimum cell error was achieved in the third case (0.17%). The case 2 is a compromise between precision and speed. Figure 9 illustrates the SI cell transient response obtained for the three cases. The choice of the suitable one is driven by the initial modulator specifications fixed at the beginning of the hierarchical design flow.

TABLE I
PARAMETERS BEFORE AND AFTER OPTIMIZATION

	Before optimization	After optimization		
		α1=0,7 α2=0,3	α1=0,5 α2=0,5	α1=0,3 α2=0,7
Wn	32.7µm	36. 27µm	35.44µm	36.11µm
Ln	4µm	1µm	4.13µm	4.95µm
Wp	52.2µm	47.14µm	33.9µm	53.35µm
Lp	2.5µm	2.6µm	3.17µm	4.75µm
Wg	14.7µm	14.63µm	18.9µm	17.31µm
Lg	1µm	1.92µm	2.48µm	0.85µm
Ig	13µm	48.07µm	47.65µm	40.5µm
Error	0.33%	2.18%	0.27%	0.17%
τ	-	69p	0.61n	1.17n

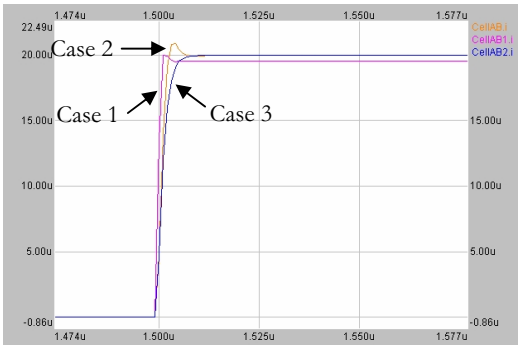

Fig. 9 Transient response of the SI cell

IV. High Level Description of the Modulator

Many recent design applications use the Switched Current technique, particularly the Sigma Delta modulators. As said above, a second order modulator requires two integrators, each one is designed with two SI memory cells. Consequently, the developed library was exploited to develop a structural

VHDL-AMS description for the modulator. Figure 10 depicts a transient simulation response performed with 1.43 kHz frequency sine input current, sampled at the rate of 1024 kHz. It shows a good and correct response of the modulator.

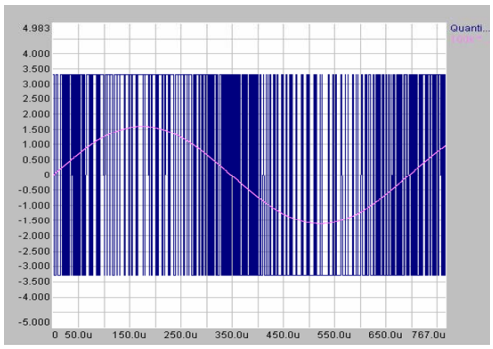

Fig. 10 High level simulation of the modulator

In order to prove the efficiency of our VHDL-AMS description, we proceed to a spectral characterization, which is hardly obtained with transistor-level simulation because of the extremely long CPU time needed to simulate the whole modulator. Figure 11 shows the obtained spectrum. Its shape suites classical spectrums of a 2nd order Sigma-Delta modulator.

Figure 12 depicts a zoom on the obtained spectrum limited to 8 kHz. It shows that the fundamental frequency is located at 1.43 kHz and the noise floor is about –65 dB.

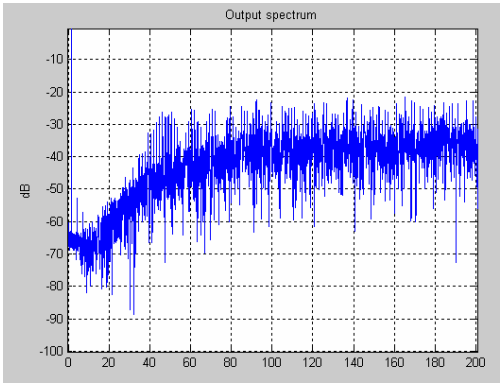

Fig. 11 Simulated power spectrum

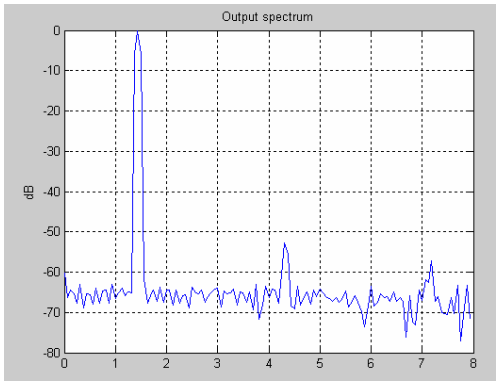

Fig. 12 Spectrum limited to 8 KHz

A further important characterization consists of drawing the Signal-to-Noise Ratio (SNR) characteristic obtained when varying the input amplitude. Figure 13 shows a high level simulation result. This important characterization gives the possibility to predict the maximum SNR (which is about 56 dB in our case) before passing to a transistor-level simulation. Traditionally, the designer is constrained to do this characterization at the final step of the design flow with a real prototype. If the obtained results do not suit the required specifications, he should go back to improve and optimize again his design, which represents a waist of time and makes difficult to reach a satisfactory time-to-market.

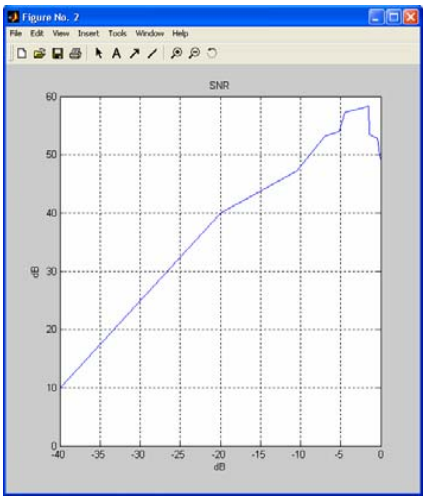

Fig. 13 SNR simulation

Once the characterization of the modulator is performed, the obtained results are compared to specifications. If there is an agreement between them, the designer can pass to a transistor-level simulation. So that, each SI cell is automatically replaced by a spice netlist description taking into account the transistor sizes (W and L) calculated at the high level description. A transistor-level simulation performs

more accurate results and predicts the effect of the physical model of transistors on the transient output of the modulator before developing the layout.

In an other case, if there is no agreement between the simulated results and specifications, new transistor sizes are performed with the optimization algorithm that will be injected in the VHDL-AMS description of the SI cells.

Figure 14 illustrates our simulation plateform. It is composed of both behavioral and transistor level simulators (Simplorer and Orcad respectively). But the proposed hierarchical design flow remains of course useful with other simulation tools.

V. Conclusion

This paper proposes an analog synthesis approach applied for the design of switched-current Sigma-Delta Modulators. It applies the Top-Down hierarchical design flow and uses the new hardware language VHDL-AMS. In the proposed design flow, we developed both a VHDL-AMS and transistor-level libraries. We associate to the SI cell VHDL-AMS description a transistor-level netlist. The designer starts by a high level simulation and characterization to perform the output spectrum and the SNR. If the desired specifications are not reached, a genetic algorithm performs new transistor sizes. When satisfactory results are finally obtained, each SI cell high level model is replaced by a transistor-level netlist to do a transistor-level simulation and verification.

Our proposed design approach using a high level description with VHDL-AMS is very useful to study and characterize complex SI systems with a reduced CPU time. At this level, it is possible to study the effect of the system imperfections because the developed models are so accurate. This work illustrates new simulation possibilities provided by the new standard VHDL-AMS.

The test of high resolution Sigma-Delta Analogue to-Digital Converters (ΣΔ ADCs) is a costly task due to its high resolution and the large number of samples required. That's why, many recent works propose a Built-In Self-Test (BIST) technique for the test of SNDR (Signal-to-Noise plus Distortion Ratio) in ΣΔ ADCs. The technique, mostly digital, uses a binary stream as test stimulus and carries out a sine-wave fitting algorithm to analyze the output response. Both the test signal generation and the output response analysis are performed on-chip, taking advantage of the digital resources already present in a ΣΔ ADC [20]. The design and the simulation of the chip (ADC + BIST) requires an important CPU time. Our proposed design approach presents a solution to solve this difficulty and we are now focused on the modeling of a BIST to develop a virtual prototype of a chip containing both a ΣΔ ADC converter and a self test circuit.

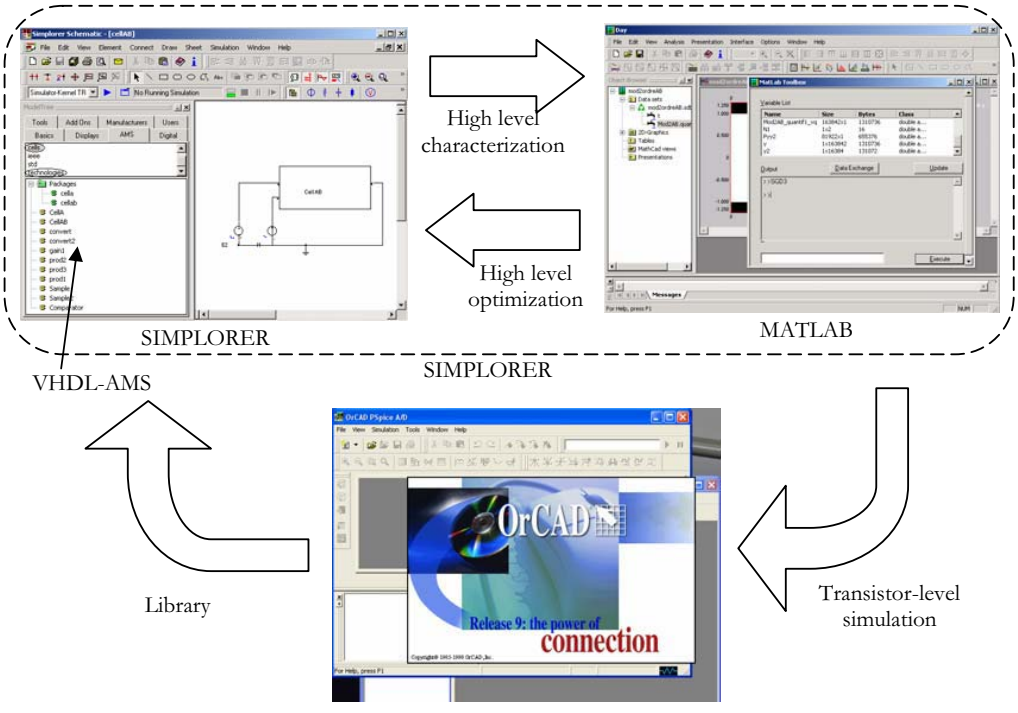

Fig. 14 Simulation plateform

APPENDIX

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ENTITY cellAB IS
PORT (TERMINAL e, h, s : ELECTRICAL);
END cellAB;
ARCHITECTURE modele OF cellAB IS
QUANTITY ve across ie THROUGH electrical_ref TO e;
QUANTITY i THROUGH s TO electrical_ref;
QUANTITY iacq, ier, iinj , errcond, erracq, errtot: REAL ;
QUANTITY Ccanal, crec, ccanf, qcanf, Crecf, Qrecf: REAL;
QUANTITY Vx0, Vx, beta, A, A1,A2, vgs,r,gs : REAL;
SIGNAL ret : REAL:=0.0;
CONSTANT Vc : REAL := (0.5) * (VDD-VTN-VTP+2.0*Vsat);
CONSTANT I0 : REAL := (KN/8.0) * (WN/LN) * (VDD-VTN-VTP-Vc)**2;
CONSTANT Gm0 : REAL := sqrt(abs(2.0*KN*I0*(WN/LN))) + sqrt (abs
(2.0*KP*I0*(WP/LP)));
CONSTANT vgs0 : REAL := sqrt(abs(I0)/(Un*cox*(WN/LN))) + VTN;
CONSTANT gi : REAL := Un*COX*(Ws/Ls) * (VDD-vgs0-VTN);
CONSTANT Gmg : REAL := 2.0*sqrt(2.0*KN*Wg*(Ig/Lg));
CONSTANT Gog : REAL := 2.0*ALPHAg*(Ig/Lg);
CONSTANT G0 : REAL := ALPHAN*(I0/LN) + ALPHAP*(I0/LP);
CONSTANT C : REAL := 2.0*(WN*LN + WP*LP)*(COX/3.0);
CONSTANT Cg : REAL := (1.0+(KN/KP)) * (2.0*Wg*Lg*(COX/3.0));
CONSTANT a10 : REAL := ((gm0*gi) * (gmg+gog)) / ((gm0*gi) *
(gmg+gog) + (g0*gog*gi));
CONSTANT b20 : REAL := 1.0;
CONSTANT b21 : REAL := ((c*(((gi-g0)*(gmg+gog)) + (g0*gi))
+ (cg*gog*(g0+gi)))) / ((gm0*gi) * (gmg+gog) + (g0*gog*gi));
CONSTANT b22 : REAL := (C*Cg*(gi+g0)) / ((gm0*gi) * (gmg+gog) +
(g0*gog*gi));
CONSTANT N : REAL_VECTOR (1 TO 3) := (a10 ,0.0 , 0.0);
CONSTANT D : REAL_VECTOR (1 TO 3) := (b20,b21, b22);
BEGIN
ret <=ie;
retard_periode : PROCESS
BEGIN
WAIT UNTIL ret = 0.5*T0;
END PROCESS retard_periode;
ier == ret;
IF (erreur_etab = true) USE
iacq == ier'ltf(N,D);
ELSE
iacq == ier;
END USE;
erracq == ier-iacq;
crec == cgd0*ws;
Ccanal== Ws*Ls*COX;
Crecf == Cgd0*Wf;
Qrecf == 2.0*Crecf*VDD;
Ccanf == Wf*Lf*COX;
Qcanf == ((VDD/2.0)-VTN)*Ccanf;
Vx0 == VDD/2.0;
A == gmg/gog;
Vx == Vx0 - (Iacq/(2.0*A*Gm0));
IF (erreur_inj = true) USE
iinj == (gm0/C) * ( ((0.5*(VDD - Vx - VTN)*Ccanal)+(Crec*VDD)) -
(qrecf+Qcanf) );
ELSE
iinj == 0.0;
END USE;
beta == (KN*WN)/LN;
A1 == 1.0 + ((G0*Vx0)/I0) +(G0/(A*Gm0));
A2 == 1.0 + ((G0*Vx0)/I0) -(G0/(A*Gm0));
vgs == sqrt(abs(I0 + iacq)/(Un*cox*(WN/LN))) + VTN;
gs == Un*COX*(Ws/Ls) * (VDD-vgs-VTN);
r == (A*gs*gm0)/((A*gs*gm0)+(g0*(gs+(A*gm0))));
IF (erreur_cond = true) USE
i == r*(A2/A1)*((iacq-iinj)) ;
ELSE
i == iacq-iinj;
END USE;
errcond == iacq-iinj - i ;
errtot == (iinj) + (errcond) + (erracq);
END modele;
```

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Dr Ahmed Fakhfakh was born in Sfax, Tunisia, in 1972. He received the Electrical Engineering degree in 1997 from National school of engineers in Sfax (ENIS), Tunisia; the Master degree in electronics in 1998 and the PhD degree in Electronics in 2002 both from IXL Laboratory, Bordeaux, France. He is an associate professor at the High Institute of electronics and Communication of Sfax at the University of Sfax in Tunisia. He became a member (M) of **IEEE** in 2000.

His research interests are in the development of VHDL-AMS virtual prototyping, new CAD methods and analogue synthesis tools.

Dr Fakhfakh is a member of the group 'Circuits and Systems' of the Laboratory of Electronics and Information Technology in Sfax, Tunisia.

Dr Nesrine Ksentini received the Electrical Engineering degree in 2001 from National School of Engineers in Sfax (ENIS), Tunisia; the Master degree in electronics in 2002 and the PhD degree in Electronics and Communications in 2007 both from ENIS, Tunisia and ENST, PARIS. She is an associate professor at the University of Sfax in Tunisia.
Her research interests are in the development of VHDL-AMS virtual prototyping and analogue synthesis tools applied especially to switched current systems.
Dr Ksentini is a member of the laboratory of electronics and information technology in Sfax, Tunisia. In 2006, she joined the High Institute of electronics and Communication of Sfax, Tunisia as an assistant professor.

Dr. Mourad Loulou was born in Sfax, Tunisia in 1968. He received the Engineering Diploma from the National School of Engineers of Sfax in 1993. He received his Ph.D. degree in 1998 in electronics system design from the University of Bordeaux France. He joints the electronic and information technology laboratory of Sfax "LETI" since 1998 and he has been assistant Professor at the National School of Engineers of Sfax from 1999. Since 2004 he obtained his HDR from the University of Sfax and he has been an associate Professor. Currently he supervises the Analogue, Mixed Mode and RF Design Group EleCom of LETI Laboratory.
Dr Loulou current research interests are on Analogue, Mixed and RF CMOS integrated circuits for communications and design automation of analogue CMOS Integrated Circuits.

Pr Jean Jacques Charlot was a professor at the High National School of Telecommunications (ENST) in Paris, France. He is now a professor at the University of Boumerdes in Algeria.
He is a scientific and pedagogic international consultant and an expert in micro electronic in TAMPUS and MEDA projects.
Pr Charlot research interests are in the VHDL-AMS modeling of multidisciplinary systems.

Pr Nouri Masmoudi was born in Sfax, Tunisia, in 1955. He received the electrical engineering degree from the Faculté des Sciences et Techniques de Sfax, Tunisia, in 1982, the DEA degree from the Institut National des Sciences Appliquées de Lyon and Université Claude Bernard de Lyon, France in 1982. From 1986 to 1990, he prepared his thesis at the laboratory of Power Electronics (LEP) at the National school of engineers in Sfax (ENIS). He then received the 'Thèse de 3ème Cycle' at the National school of engineers in Tunis (ENIT), Tunisia in 1990. From 1990 to 2000, he was an assistant professor at the electrical engineering department at the ENIS.
Since 2000, he has been an associate professor and head of the group 'Circuits and Systems' of the Laboratory of Electronics and Information Technology in Sfax. Currently, he is responsible of the Electronic Master Program at ENIS.
Dr Masmoudi's research activities have been devoted to several topics: Design, Telecommunications, High-level design flow, Embedded systems and Information technology.