First Order Filter Based Current-Mode Sinusoidal Oscillators Using Current Differencing Transconductance Amplifiers (CDTAs)

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Abstract—This article presents new current-mode oscillator circuits using CDTAs which is designed from block diagram. The proposed circuits consist of two CDTAs and two grounded capacitors. The condition of oscillation and the frequency of oscillation can be adjusted by electronic method. The circuits have high output impedance and use only grounded capacitors without any external resistor which is very appropriate to future development into an integrated circuit. The results of PSPICE simulation program are corresponding to the theoretical analysis.

Keywords—Current-mode, Quadrature Oscillator, Block Diagram, CDTA

I. INTRODUCTION

THE current design of the active building block (ABB) L devices begins the role as being used in analog technology and analog signal processing. Therefore, ABB has been developed to be used as a pawn in the designed circuit, which is suitable for a class of analog signal processing for voltagemode and current-mode technique. The filter and oscillator circuits are important in electrical and electronic engineering. These circuits have been widely implemented such as, telecommunication system, measuring tool systems, and signal processing for instance. Consequently, a lot of filter and oscillator circuits are needed to be introduced with modern active building blocks. Recently, circuits designed using block diagram/signal flow graph have been recommended in convenience for designing [1], [2]. In the last decade, a lot of papers in electronic circuit design have been presented in current-mode technique. It is stated that the circuit designed from current-mode technique provides advantages, such as, larger dynamic range, inherently wide bandwidth, higher slewrate, greater linearity and low power consumption [3], [4].

From literature survey, it is found that several implementations of oscillators and quadrature oscillators using active building block, have been reported [4]-[20]. Unfortunately, these reported circuits suffer from one more of weaknesses. For example, the proposed circuits use floating capacitor [5]-[7], [9], [15], which is not convenient for further fabrication in integrated circuits [21]. The external resistors are excessively used [4]-[7], [9]-[11], [13]-[15], [17]-[20], as well as, the condition of oscillation and the frequency of

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oscillation cannot be adjusted by electronic method [4]-[7], [9]-[11], [13]-[15], [17]-[20], Moreover, output impedances are not high, that make the circuit cannot directly drive load [12], [14], [16], [20].

The purpose of this paper is to present the current-mode oscillator circuits using CDTAs which is designed from new block diagram. The block diagram consists of current-mode first order high-pass and low-pass filters which are cascade connection. The oscillator circuits consist of two CDTAs and two grounded capacitors. The proposed oscillator circuits have high output impedance appropriate for cascade connection application in current mode technique which is capable to directly drive load. The circuits use only grounded capacitors without addition external resisters. This qualification is convenient for further fabrication in integrated circuits [22]-[23]. Accordingly, the PSPICE simulation program results are in correspondence with the theoretical analysis.

II. BASIC CONCEPT OF CDTA

In 2003, there was a new active building block namely current differencing transconductance amplifier (CDTA) presented for analog signal processing suitable for voltage-mode and current-mode techniques [24]. The characteristics of the ideal CDTA are represented by the following hybrid matrix:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & g \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V \end{bmatrix}$$
 (1)

The symbol and equivalent circuit of the CDTA are illustrated in Figs. 1 (a) and (b), respectively. The CMOS internal construction of CDTA is shown in Fig 2.

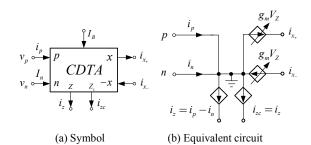


Fig. 1 CDTA

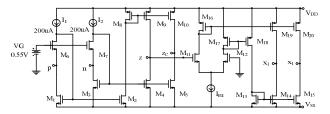


Fig. 2 Internal construction of CDTA [25]

The difference of the input currents (i_p and i_n) flows from port z. In some applications, the z terminal of CDTA can be extended to utilize the current through z terminal which is called z_c (z-copy) [26]. For CMOS CDTA, the transconductance (g_m) can be written as

$$g_m = \sqrt{kI_R} \tag{2}$$

where

$$k = \mu_n C_{ox} \left(\frac{W}{L} \right)_{1112} \tag{3}$$

 $k = \mu_n C_{ox}(W/L)$ is the physical parameter of CMOS transistor. Where μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width and L is the effective channel length.

III. PROPOSED CURRENT-MODE OSCILLATORS

The proposed current-mode sinusoidal oscillator circuits designed from block diagram shown in Fig. 3. It is designed based on cascading of current-mode first order high-pass and low-pass filters.

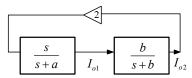


Fig. 3 Block diagram for the oscillator

From block diagram in Fig. 3, the characteristic equation of the oscillator circuit is written as

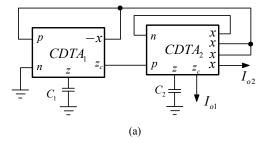
$$s^{2} + s(a-b) + ab = 0 (4)$$

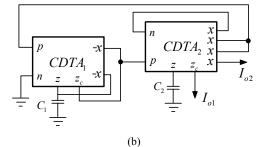
From (4), the condition of oscillations and frequency of oscillation are written as

$$a = b \tag{5}$$

and

$$\omega_{osc} = \sqrt{ab}$$
 (6)





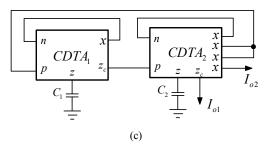


Fig. 4 Proposed current-mode oscillators

From block diagram in Fig. 3, the realization of proposed current-mode sinusoidal oscillators is achieved in Figs. 4 (a) to (c). Additionally, the characteristic equation of the proposed circuits can be written in (7).

$$s^{2} + s \frac{g_{m1}C_{2} - g_{m2}C_{1}}{C_{1}C_{2}} + \frac{g_{m1}g_{m2}}{C_{1}C_{2}} = 0$$
 (7)

From (7), the condition of oscillation and frequency of oscillation are written as

$$g_{m1} = g_{m2}, \quad C_2 = C_1$$
 (8)

and

$$\omega_{osc} = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{9}$$

It is found from (8) and (9) that if $g_{mi} = \sqrt{kI_{Bi}}$, the condition of oscillation and frequencies of oscillation are as follows:

$$I_{B1} = I_{B2}, \quad C_2 = C_1$$
 (10)

and

$$\omega_{osc} = \sqrt{k \frac{\sqrt{I_{B1}I_{B2}}}{C_1 C_2}}$$
 (11)

Sensitivities of the active and passive of oscillators are shown in (12).

$$S_{C_1,C_2}^{\omega_{\text{osc}}} = -\frac{1}{2}, \quad S_{g_{m_1},g_{m_2}}^{\omega_{\text{osc}}} = \frac{1}{2}$$
 (12)

IV. ANALYSIS OF NON-IDEAL CASE

For non-idealities case, the characteristic equation of CDTA in (1) is written as

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix}$$
(13)

The parameters α_p , α_n and β are the voltage/current transfer deviated from one, depending on the value of intrinsic impedances and temperatures. In non-ideal case the characteristic equation, the condition of oscillation and the frequency of oscillation from (7) to (9) are as follows:

Circuit 4(a):

$$\begin{cases}
s^{2} + s \left(\frac{C_{1}\beta_{2}\alpha_{n2}g_{m2} + C_{2}\beta_{1}\alpha_{\rho1}g_{m1} - 2C_{1}\beta_{2}\alpha_{\rho1}\alpha_{\rho2}g_{m2}}{C_{1}C_{2}} \right) \\
+ \frac{\beta_{1}\beta_{2}\alpha_{\rho1}\alpha_{n2}g_{m1}g_{m2}}{C_{1}C_{2}}
\end{cases} = 0 \quad (14)$$

$$C_1 \beta_2 \alpha_{n2} g_{m2} + C_2 \beta_1 \alpha_{n1} g_{m1} = 2C_1 \beta_2 \alpha_{n1} \alpha_{n2} g_{m2}$$
 (15)

and

$$\omega_{osc} = \sqrt{\frac{\beta_1 \beta_2 \alpha_{p1} \alpha_{n2} g_{m1} g_{m2}}{C_1 C_2}}$$
 (16)

Circuit 4(b)

$$\begin{cases}
s^{2} + s \left(\frac{C_{1}\beta_{2}\alpha_{n2}g_{m2} + C_{2}\beta_{1}g_{m1} - 2C_{1}\beta_{2}\alpha_{p1}\alpha_{p2}g_{m2}}{C_{1}C_{2}} \right) \\
+ \frac{\beta_{1}\beta_{2}\alpha_{n2}g_{m1}g_{m2}}{C_{1}C_{2}}
\end{cases} = 0 \quad (17)$$

$$C_1 \beta_2 \alpha_{n2} g_{m2} + C_2 \beta_1 g_{m1} = 2C_1 \beta_2 \alpha_{p1} \alpha_{p2} g_{m2}$$
 (18)

and

$$\omega_{osc} = \sqrt{\frac{\beta_1 \beta_2 \alpha_{n2} g_{m1} g_{m2}}{C_1 C_2}}$$
 (19)

Circuit 4(c):

$$\begin{cases}
s^{2} + s \left(\frac{C_{1}\beta_{2}\alpha_{n2}g_{m2} + C_{2}\beta_{1}\alpha_{n1}g_{m1} - 2C_{1}\beta_{2}\alpha_{p1}\alpha_{p2}g_{m2}}{C_{1}C_{2}} \right) \\
+ \frac{\beta_{1}\beta_{2}\alpha_{n1}\alpha_{n2}g_{m1}g_{m2}}{C_{1}C_{2}}
\end{cases} = 0 (20)$$

$$C_1 \beta_2 \alpha_{n2} g_{m2} + C_2 \beta_1 \alpha_{n1} g_{m1} = 2C_1 \beta_2 \alpha_{n1} \alpha_{n2} g_{m2}$$
 (21)

and

$$\omega_{osc} = \sqrt{\frac{\beta_1 \beta_2 \alpha_{n1} \alpha_{n2} g_{m1} g_{m2}}{C_1 C_2}}$$
 (22)

V. ANALYSIS OF THE PARASITIC RESISTANCES AND CAPACITANCES

The parasitic resistances and capacitances of the CDTA can be shown in Fig. 5. If the parasitic resistances at the z and x terminals are much greater than the parasitic resistances at p and n terminals $(R_z, R_x \gg R_p, R_n)$, in this case, the characteristic equation, the condition of oscillation and the frequency of oscillation of the current-mode sinusoidal oscillators, from (7) to (9) are represented as follows:

Circuit 4(a) and 4(c):

$$\begin{cases}
s^{2} + s \frac{g_{m1}(C_{2} + C_{z2}) - g_{m2}(C_{1} + C_{z1})}{(C_{1} + C_{z1})(C_{2} + C_{z2})} \\
+ \frac{g_{m1}g_{m2}}{(C_{1} + C_{z1})(C_{2} + C_{z2})}
\end{cases} = 0$$
(23)

$$g_{m1}(C_2 + C_{z2}) = g_{m2}(C_1 + C_{z1})$$
 (24)

and

$$\omega_{osc} = \sqrt{\frac{g_{m1}g_{m2}}{(C_1 + C_{z1})(C_2 + C_{z2})}}$$
 (25)

Circuit 4(b):

$$\begin{cases}
s^{2} + s \frac{g_{m1}(C_{2} + C_{z2}) - g_{m2}(C_{1} + C_{z1} + C_{x1})}{(C_{1} + C_{z1} + C_{x1})(C_{2} + C_{z2})} \\
+ \frac{g_{m1}g_{m2}}{(C_{1} + C_{z1} + C_{x1})(C_{2} + C_{z2})}
\end{cases} = 0$$
(26)

$$g_{m1}(C_2 + C_{22}) = g_{m2}(C_1 + C_{21} + C_{21}) \tag{27}$$

and

$$\omega_{osc} = \sqrt{\frac{g_{m1}g_{m2}}{(C_1 + C_{z1} + C_{x1})(C_2 + C_{z2})}}$$
 (28)

Fig. 5 The parasitic resistances and capacitances of the CDTA

VI. SIMULATION RESULTS

To verify the theoretical prediction of the proposed current-mode oscillators in Fig. 4, (for example, proposed oscillator in Fig. 4 (c)) the PSPICE simulation was built with $C_1 = C_2 = 0.3$ nF, $I_{B1} = I_{B2} = 250\mu A$. The CMOS implementation of the internal construction of CDTA used in simulation is shown in Fig. 2. The PMOS and NMOS transistors employed in the proposed circuit were simulated by using the parameters of $0.35\mu m$ TSMC CMOS technology [27]. In addition, the ratio of dimension of the transistors PMOS and NMOS is shown in Table I.

TABLE I DIMENSIONS OF CMOS TRANSISTORS

DIMENSIONS OF CIVIOS TRANSISTORS		
Transistor	W(µm)	L(µm)
M1-M10	20.00	1.00
M11-M12	40.00	1.00
M13-M15	3.00	1.00
M16	5.00	1.00
M17	5.35	1.00
M18-M20	6.40	1.00

The circuit was biased with $\pm 1.6V$ supply voltages. This yields oscillation frequency of 715.358 kHz, where the calculated value of this parameter from (11) yields 749.586 kHz (deviated by 4.785%). In this case, value of the parameter changed because the CMOS implementation used in the circuit deviated from the non-ideal properties and the effect of parasitic elements. Figs. 6 and 7 show the simulated quadrature output waveforms during initial state and steady state, respectively. Fig. 8 shows the simulation result of output spectrum. The total harmonic distortion (THD) of I_{o1} and I_{o2} are about 1.488% and 0.662%, respectively. In addition, the phase difference of the output current I_{o1} and I_{o2} are approximately 89.75 degrees. The generated waveforms relationship within oscillator circuit has been verified by Lissagous Figure, shown in Fig. 9.

VII. CONCLUSION

The current-mode oscillators have been introduced in this paper. The proposed current-mode oscillators consists of two CDTAs and two grounded capacitors, the condition of oscillation and frequency of oscillation can be electronically controlled by adjusting the bias currents of the CDTA. The proposed circuits use only grounded capacitors without addition external resistor which are very appropriate for further development into integrated circuits. Additionally, this paper also presents block diagram designed for signal generating oscillation application for other active devices. The designed block diagram is easy for application because it uses only first order high-pass filter and low-pass filter which is cascade connection. PSPICE simulations are included to verify the theoretical analysis.

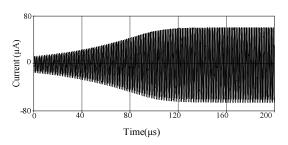


Fig. 6 The simulation result of output waveforms during initial state

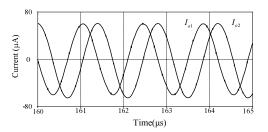


Fig. 7 The quadrature output waveforms in steady state

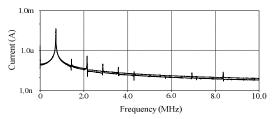


Fig. 8 The output frequency spectrum

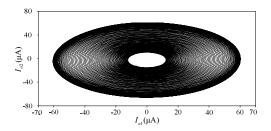


Fig. 9 Lissagous figure

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