

# Fast and Efficient On-Chip Interconnection Modeling for High Speed VLSI Systems

A.R. Aswatha, T. Basavaraju, and S. Sandeep Kumar

**Abstract**—Timing driven physical design, synthesis, and optimization tools need efficient closed-form delay models for estimating the delay associated with each net in an integrated circuit (IC) design. The total number of nets in a modern IC design has increased dramatically and exceeded millions. Therefore efficient modeling of interconnection is needed for high speed IC's. This paper presents closed-form expressions for RC and RLC interconnection trees in current mode signaling, which can be implemented in VLSI design tool. These analytical model expressions can be used for accurate calculation of delay after the design clock tree has been laid out and the design is fully routed. Evaluation of these analytical models is several orders of magnitude faster than simulation using SPICE.

**Keywords**—IC design, RC/RLC Interconnection, VLSI Systems.

## I. INTRODUCTION

AS the result of the scaling down of technology and increase in transistor density, the cross sectional area of wires has been reduced. With these trends, it is becoming crucial to be able to determine which nets within high speed VLSI circuit exhibit prominent inductive effects. To accomplish this, it is necessary to analyze and model the timing characteristics of the interconnects. An interconnection can be described by means of its electrical parameters, and today most extraction and delay analysis tools are limited to resistor and capacitance. The increasing operation speed of integrated circuits may have more important consequences on the transmission line. Therefore RC modeling is not efficient for global interconnection at high frequencies. Therefore, the model chosen to describe and simulate the interconnection should take effects of inductance into account. The most complete description of the line is given by the RLC model.

Various techniques have been proposed for the delay analysis of interconnects. These techniques are based on either simulation techniques or (closed-form) analytical formulas for voltage-mode (VM) signaling. Simulation tools such as SPICE give the most accurate insight into arbitrary interconnect structures but are computationally expensive. However, with the increasing speed requirements in VLSI circuits, current-mode (CM) signal transporting techniques may provide an attractive solution to some of the challenges caused by aggressive interconnect scaling.

The main objective of this paper is to find out when the inductance of the line must be included in the model considering a typical case of VLSI interconnections. The closed-form delay expression presented in this paper provides

fast delay estimation including the inductance effect for long global interconnection. A closed-form RC model for CM interconnects has been derived using first order moment approximation. The RLC model is derived using the concept of absorbing inductance effect into equivalent RC model and then recurring MNA (modified nodal analysis) is used to obtain the equivalent resistance to model load delay.

The paper is organized as follows: section II presents the derivation of the closed form current mode (CM) delay expression for RC modeling; Section III presents the closed form CM delay expression for RLC modeling of interconnection. Section IV discusses the accuracy of RC/RLC delay formula in various operation regions.

## II. CLOSED-FORM RC DELAY FORMULA FOR CM SIGNALING

Long global interconnects can be modeled by distributed RC transmission lines as long as the overall line resistance dominates the response (i.e.  $R \gg j\omega L$ ). The key to current-mode signal transporting is the low impedance termination at the receiver which results in reduced signal swings and increased bandwidth performance. The distributed RC model for CM interconnects [1] is shown in Fig 1a. The driver is modeled as a voltage source with source resistance  $R_s$ . For the sake of generality, the line is terminated with a resistor  $R_L$  and load capacitance  $C_L$ . For voltage-mode signaling the termination resistance  $R_L$  is infinite and the output voltage seen across  $C_L$ . In current-mode signaling, the terminating resistance  $R_L$  is finite.

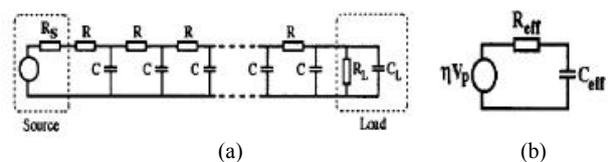


Fig. 1 (a) Generalized distributed RC model (b) Approximate effective lumped element model

### A. Effective Resistance and Capacitance

Since Elmore's formulation is basically a first moment approximation of the signal delay time, Moment-Matching Methods [2][3] can be used to derive a first-order RC network with effective lumped element parameters for voltage and current mode signaling. It is well understood that a lumped, linear, time-invariant circuit such as that of a generalized distributed RC line shown in Fig. 1, can be conveniently expressed in terms of state equations using the modified nodal

Analysis (MNA) representation [4]. The generalized output equation [1] can be expressed in the Laplace domain as:

$$[\bar{G} + s\bar{C}].[X(s)] = b(s) \quad (1)$$

where  $G$  and  $C$  are the nodal conductance and capacitance matrix, respectively;  $X(s)$  is the vector of node voltages; and  $b(s)$  is the input source excitation. The  $N \times N$  nodal conductance matrix  $G$  for the circuit topology shown in Fig. 1(b) can be written as:

$$[G] = \begin{bmatrix} G_{S1} + G_u & -G_u & 0 & \dots & 0 \\ -G_u & 2G_u & -G_u & 0 & \\ 0 & -G_u & 2G_u & -G_u & 0 \\ \vdots & \dots & \dots & \dots & \vdots \\ 0 & 0 & -G_u & 2G_u & -G_u & 0 \\ & 0 & -G_u & 2G_u & -G_u & \\ 0 & \dots & 0 & -G_u & G_L + G_u \end{bmatrix} \quad (2)$$

$G_u$  is the segment conductance of the distributed transmission line and  $G_L$  is the load conductance. In (2),  $G_{S1} = 1/(R_S + R_u)$ ; where  $R_S$  is the source resistance and  $R_u$  is unit length resistance.

As described in [1][2], the node voltage vector  $X(s)$  is expanded using the Taylor series and coefficients of similar powers of  $s$  are equated to obtain the following expressions:

$$\begin{aligned} GM_o &= b \\ GM_q &= -CM_{q-1} \quad q > 0 \end{aligned} \quad (3)$$

where  $M$ , represents the moment vector of the transfer function  $H(s)$  of Fig. 1(a). A general closed-form expression for the  $q^{\text{th}}$  moment and the  $k^{\text{th}}$  node voltage of  $X(s)$  is given by:

$$m_{q+1}^k = \sum_{j=1}^N -G_{inv}(k, j) \cdot C(j) \cdot m_q^j \quad (4)$$

where  $N$  is the number of distributed segments and  $G_{inv}$  is the inverse matrix ( $G^{-1}$ ) which can be expressed as:

$$\begin{aligned} G_{inv}(k, j) &= \frac{[G_u + (N-k)G_L][G_u + (j-1)G_{S1}]}{G_u[G_u G_{S1} + (N-1)G_L G_{S1} + G_L G_u]} \quad j \leq k \\ &= \frac{[G_u + (N-j)G_L][G_u + (k-1)G_{S1}]}{G_u[G_u G_{S1} + (N-1)G_L G_{S1} + G_L G_u]} \quad j > k \end{aligned} \quad (5)$$

Similarly, we can express the  $0^{\text{th}}$  moment for the  $k^{\text{th}}$  nodal voltage as:

$$m_o^k = \frac{G_S [G_u + (N-k)G_L]}{[G_u G_S + (N-1)G_L G_S + G_L G_u]} \quad (6)$$

From (4), (5) and (6) all higher order moments can be derived.

To obtain the effective resistance and capacitance of the first order AWE approximation, we express the reduced single order rational transfer function  $H(s)$  in terms of the polynomial coefficients  $a_0$  and  $b_1$ , calculated from the  $0^{\text{th}}$  and  $1^{\text{st}}$  moments using (4) and (6), given as:

$$a_o = m_o, \quad b_1 = -m_1/m_o \quad (7)$$

Since the pole of  $H(s)$  is  $1/(R_{\text{eff}}C_{\text{eff}})$ , the effective resistance and capacitance is derived from (7), which can be written in closed-form

$$\begin{aligned} R_{\text{eff}} &= \eta \frac{R_{\text{tot}}}{\sqrt{2}} \left( \frac{N+1}{N} \right) \left( 1 + \frac{R_{\text{tot}}}{3R_L} \left( \frac{N-1}{N} \right) \right) \\ &\quad + 2\eta \frac{R_S}{\sqrt{2}} \left( 1 + \frac{R_{\text{tot}}}{2R_L} \left( \frac{N-1}{N} \right) \right) \end{aligned} \quad (8a)$$

$$C_{\text{eff}} = \frac{C_{\text{tot}}}{\sqrt{2}} + C_L \eta \frac{R_S + R_{\text{tot}}}{R_{\text{eff}}} \quad (8b)$$

$$\eta = \frac{R_L}{R_L + R_S + R_{\text{tot}}} \quad (8c)$$

Where  $R_{\text{tot}}$  and  $C_{\text{tot}}$  are the total resistance and capacitance calculated from the unit length components  $R_u$  and  $C_u$  and total interconnect length  $l$ ;  $N$  is the number of distributed segments;  $R_S$  and  $R_L$  are the source and load resistance respectively.

Thus the lumped element resistance and capacitance in (8) are the effective components that model the distributed transmission line. The generalized effective lumped element model is shown in Fig. 1(b). For current mode signals the source voltage ( $V_p$ ) is scaled by  $\eta$ .

### III. CLOSED-FORM RLC DELAY FORMULA FOR CM SIGNALING

The distributed RLC model for CM interconnects [5] is shown in Fig. 2.  $R$ ,  $L$  and  $C$  are designated as unit length resistance, inductance and capacitance, respectively,  $\Delta d$  is the length of each lumped section;  $R_o$  is source resistance;  $C_L$ ,  $R_L$  are load capacitance and resistance. The principle of current mode signaling is that, by loading the line with finite impedance, the dominant pole of the system shifts, resulting which causes a smaller time constant and thus less delay.

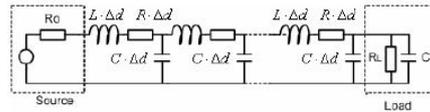


Fig. 2 Current mode RLC analysis model

#### A. Absorbing Inductance into Effective Resistance

In modern technology, as the self-inductance of the line increases, it affects both line delay and load delay. In order to quantify the inductance effect, a Voltage Mode delay model is expressed in terms of characteristic impedance  $Z_o$ , which is derived using both analytical methods and simulation approximation in [6]. Fig. 3 shows the equivalent load delay for the VM interconnects [5], where  $Z_o = \sqrt{L/C}$ ,  $d$  is the total length of the line. As shown in Fig 3, in the case of RC model, the equivalent resistance is " $R_o + R.d$ "; in the case where inductive effect is considered the equivalent resistance is " $R.d + 0.65R_o + 0.36Z_o$ ", where the coefficient "0.65" and "0.36" reflect the shielding effect of inductance.



similar way in the voltage mode derivation [8]. The transfer function is in the form of  $H(s) = \omega_n^2 / (s^2 + 2\zeta\omega_n s + \omega_n^2)$ .

where  $\zeta$  is the damping ratio and  $\omega_n$  is the undamped natural frequency.  $H(s)$  is given by (16) and the damping ratio is given by (17).

$$\frac{1}{dLC_t s^2 + \left[ \frac{dL}{R_L} + R_t C_t \right] s + 1 + \frac{R_t}{R_L}} \quad (16)$$

$$\zeta_{CM} = \left( \frac{Ld}{R_L} + R_t C_t \right) \frac{1}{2\sqrt{dLC_t \left( 1 + \frac{R_t}{R_L} \right)}} \quad (17)$$

when  $\zeta > 1$ , the system operates predominantly in RC region; when  $\zeta < 1$ , the system will exhibit inductive effect; when  $\zeta < 0.7$ , the system enters inductance dominant region [9], where the RLC expression has the maximum accuracy.

Fig. 5 shows the delay versus load capacitance [5]. The damping ratio increases as  $C_L$  increases. When  $\zeta = 0.7$ , the expression has an error of 2% at point A where  $C_L$  is 350fF. At point B,  $\zeta = 1$ , the accuracy of RLC model is equal to the RC model. As  $C_L$  increases further, the RC model becomes more accurate. Given the nature of the line, the designer can choose the appropriate model to estimate the delay.

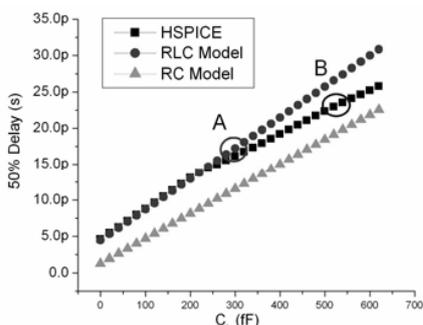


Fig. 5 50% delay versus load capacitance

Fig. 6 shows the comparison of HSPICE with RLC and RC model when line length varies from 1mm to 6mm. The average error for the RLC expression compared to HSPICE simulation is 2.7%, while the RC model has 20% error in this case.

V. CONCLUSION

Simple closed form expressions for RC model and RLC model is presented. These closed-form delay formulas are compared with HSPICE. Finally RC and RLC regions are identified based on the value of damping ratio. These current mode closed-form expressions give more efficient results than the voltage mode signaling expressions. Hence these closed form expression can be implemented in VLSI design tool for efficient modeling of interconnection in high speed VLSI chips. These analytical delay formulas are much faster than simulating using SPICE.

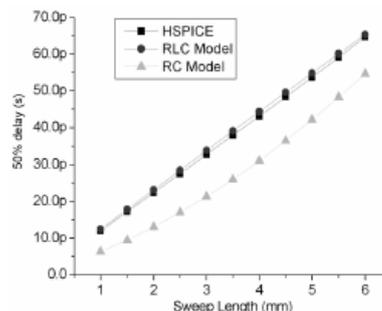


Fig. 6 Comparison of HSPICE simulation with the RLC and RC model. The 50% delay is based on step excitation versus line length

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