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Effect of Field Dielectric Material on Performance of InGaAs Power LDMOSFET

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***Abstract*—**In this paper, a power laterally-diffused metal-oxide-semiconductor field-effect transistor (LDMOSFET) on $In_{0.53}Ga_{0.47}As$ is presented. The device utilizes a thicker field-oxide with low dielectric constant under the field-plate in order to achieve possible reduction in device capacitances and reduced-surface-field effect. Using 2D numerical simulations, performance of the proposed device is analyzed and compared with that of the conventional LDMOSFET. The proposed structure provides 50% increase in the breakdown voltage, 21% increase in transit frequency, and 72% improvement in figure-of-merit over the conventional device for same cell pitch.

***Keywords*—**InGaAs, dielectric, lateral, power MOSFET.

I. Introduction

LOW-VOLTAGE (5-40 V) power integrated circuits (PICs) are playing an important role in the portable power management systems such as telecommunication, computer, transportation, and industrial power applications. Power laterally-diffused metal-oxide-semiconductor field-effect transistors (LDMOSFETs) are used as key components in the development of PICs. Presently, silicon is most widely used material in the fabrication of LDMOSFETs due to its ease of fabrication with CMOS process. As the silicon based devices are reaching their performance limit, it is necessary to consider the alternate semiconductor materials for further improvement in the device performance. InGaAs is one of the promising materials which may replace Si in MOSFETs due to its high electron mobility leading to higher current density and lower ON-resistance [1]-[3]. These advantages along with improvements in the fabrication process and oxide-InGaAs interface have led to development of MOSFETs with InGaAs channel for radio-frequency and digital applications [4]-[6]. For the first time, the simulation results on InGaAs power LDMOSFET was reported by Steighner et al. [7]. They have demonstrated that the performance of an InGaAs power LDMOSFET is better as compared to its silicon counterpart. It is important to note that although, the gate field-plate over the drift region is used to enhance the breakdown voltage of a power LDMOSFET but it degrades the high frequency response of the device due to increased gate to drain capacitance. Further, in the reported structure [7], a uniform thickness with same dielectric material was used for gate and field oxides. We propose that the performance of a power LDMOSFET can be improved by using a thicker field-oxide with high-κ and low-κ dielectric materials for the gate-oxide and field-oxide, respectively. Therefore, motive of this work is to propose a power LDMOSFET on $In_{0.53}Ga_{0.47}As$ which consists of greater field-oxide thickness under the field-plate with lesser dielectric constant as compared to the gate-oxide to achieve reduction in the device capacitances as well as redistribution of electric field in the drift region. Using 2D simulations in the device simulator (ATLAS) [8], the performance of the proposed device has been evaluated and compared with that of the conventional $In_{0.53}Ga_{0.47}As$ power LDMOSFET for the same cell pitch. The proposed device not only exhibits a better trade-off between ON-resistance and breakdown voltage but also improves the transit frequency.

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II. Device Structure

Fig. 1 shows cross-sectional view of the conventional power LDMOSFET (Device1) and the proposed power LDMOSFET structure (Device2) on $In_{0.53}Ga_{0.47}As$. The conventional LDMOSFET structure is similar to the device reported in [7] which has a field-plate over the drift region to improve the breakdown voltage. In this structure, Al_2O_3 with high dielectric constant ($\kappa = 8.0$) material is employed for both the gate-oxide and field-oxide. On the other hand, as shown in Fig. 1 (b), the modified LDMOSFET structure is having a field-plate with thicker field-oxide (t_{ox1}) as compared to that of Device1. Further, SiO_2 as a low dielectric constant ($\kappa = 3.9$) material is used for the field-oxide and high-κ Al_2O_3 is placed as the gate-oxide. The larger field-oxide thickness under the field-plate together with a low-κ dielectric reduces the device capacitances and hence improves the transit frequency. The modified structure also helps in redistributing the electric field in the drift region causing reduced-surface-field (RESURF) effect in the device. A reduction in peak electric field in the drift region improves the breakdown voltage resulting better trade-off between ON-resistance and breakdown voltage. It may be noted that the peak electric field responsible for the breakdown in both the structures occurs at the end of field-plate on InGaAs surface (at point 'A' marked in Fig. 1). The optimized structural parameters used in the simulation for both the devices are given in Table I. Note that all structural parameters are kept same for both the devices except field-oxide thickness (t_{ox1}).

TABLE I
STRUCTURAL PARAMETERS USED IN SIMULATION

Parameter	Symbol	Units	Device1	Device2
Cell pitch	L	μm	4.0	4.0
Gate length	L_G	μm	0.5	0.5
Field-plate length	L_{FP}	μm	1.2	1.2
Drift region length	L_D	μm	2.1	2.1
Gate oxide thickness	t_{ox}	μm	0.03	0.03
Oxide thickness 1	t_{ox1}	μm	-	0.06
Drift epilayer thickness	t_{epi}	μm	0.65	0.65
Drift region doping	N_d	cm^{-3}	$5x10^{16}$	$5x10^{16}$
P-body doping	-	cm^{-3}	$1x10^{17}$	$1x10^{17}$

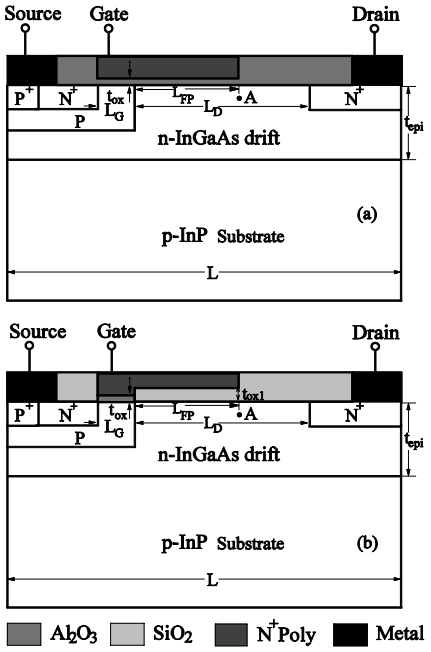

Fig. 1 Cross-sectional view of (a) Device1 (b) Device2

III. SIMULATION RESULTS

Both the device structures were implemented in device simulator (ATLAS) and 2-D numerical simulations were performed by choosing suitable models for Shockley-Read-Hall, concentration-dependent mobility, electric-field-dependent mobility, and impact ionization [8]. Fig. 2 shows drain characteristics of the Device1 and Device2 at different gate bias voltages. As seen, drain current of both the devices is same below 2.5V gate bias. However, at higher gate voltages, drain current of Device1 is more than that of Device2. This is due to the fact that as gate voltage is increased, an accumulation of electrons occurs in the drift region under the field-plate in Device1 which has thinner field-oxide with high-κ dielectric as compared to Device2 having thicker field-oxide with low-κ dielectric. It can be better understood from Fig. 3 which gives electron concentration near the surface along a vertical line below gate field-plate in the drift region for both the structures. It is clearly indicated that at same gate bias, V_{GS}=5V, the conventional device shows higher electron concentration near the surface as compared to the proposed device. This increased accumulation of electrons in Device1 also reduces its ON-resistance. ON-resistance of a MOSFET is taken as the ratio of drain voltage to drain current when device operates in the linear region. Fig. 4 gives drain characteristics in linear region at V_{GS} = 5V for both the device. Specific ON-resistance of Device1 and Device2 are found to be 20.9 and 27.2 mΩ-mm^2, respectively. In other words, specific ON-resistance of Device2 is 30% higher as compared to that of Device1.

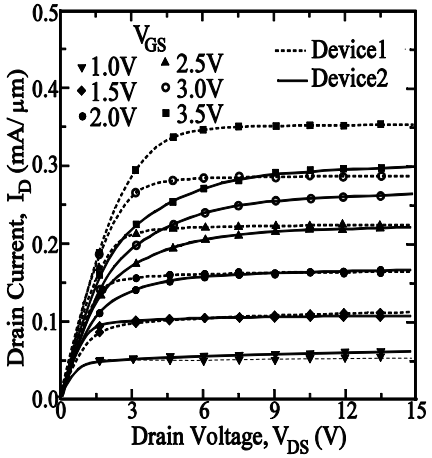

Fig. 2 On-state characteristics of Device1 and Device2

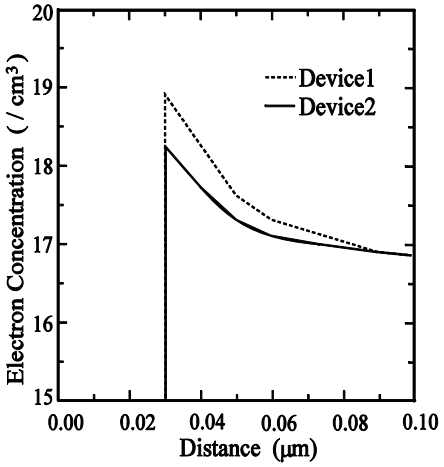

Fig. 3 Electron concentration in the drift region along a vertical line near the surface at V_{GS} = 5V for Device1 and Device2

Fig. 5 shows off-state breakdown characteristics of both the devices. At a drift region doping of $5\times10^{16}cm^{-3}$, it is observed that the breakdown voltage of Device2 and Device1 are 39V and 26V, respectively, which provides 50% improvement in the breakdown voltage. The reason for increase in breakdown voltage of the proposed device is reduction in peak electric field in the drift region due to increased field-oxide thickness. Fig. 6 gives the electric field distribution along the surface in the drift region for both the devices. The peak electric field occurs on InGaAs surface in the drift region at point 'A' i.e. at the end of field-plate in both the structures. It can be seen that at V_{DS} = 20V, peak electric field in the conventional device is

0.65 MV/cm which reduces to 0.40 MV/cm in the proposed structure. However, at breakdown voltages, the peak electric field in both the devices is equal confirming their breakdown at point 'A'. It may be noted that the breakdown voltage of both the devices will be affected by their structural parameters whose optimized values are given in Table I. Although, specific ON-resistance (R_{on-sp}) of the proposed device is higher than that of the conventional device but the proposed structure exhibits large improvement in the breakdown voltage (V_{br}). Overall effect is that the figure-of-merit (FOM = V_{br}^2/R_{on-sp}) of the proposed structure is 72% higher than that of the conventional device i.e. the proposed device provides a better trade-off between ON-resistance and breakdown voltage.

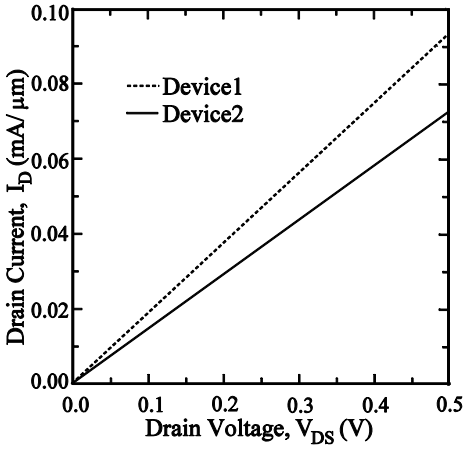

Fig. 4 Drain characteristics in linear region at V_{GS} = 5V

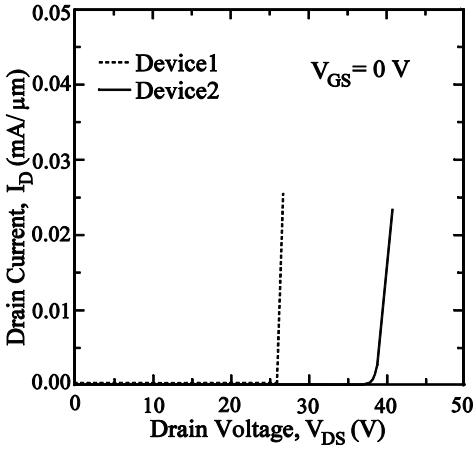

Fig. 5 Breakdown characteristics of Device1 and Device2

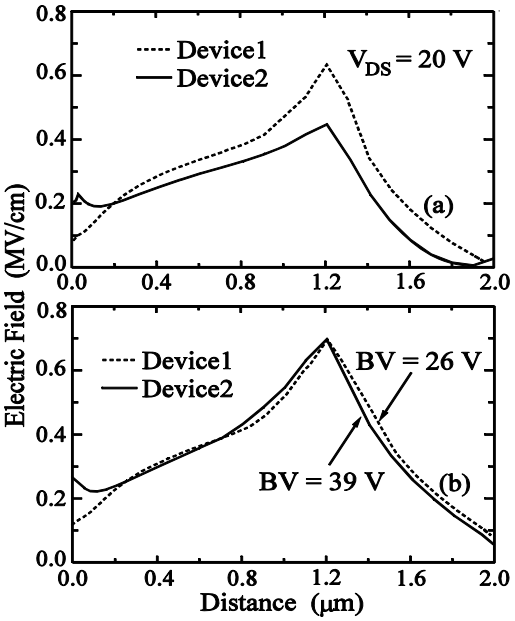

Fig. 6 Electric field variation: (a) at V_{DS} = 20V and (b) at breakdown

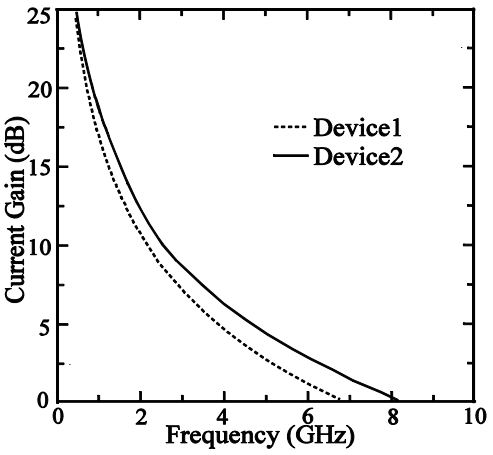

Fig. 7 Frequency response of Device1 and Device2

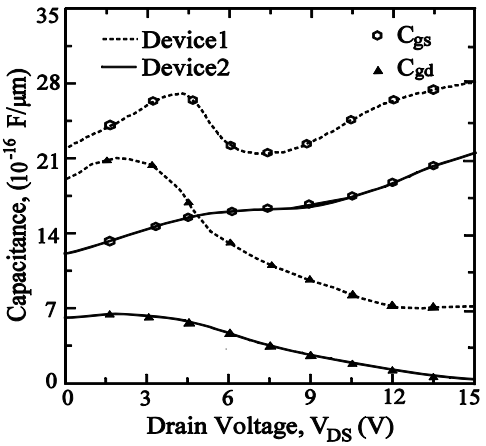

Fig. 8 Capacitance variation for Device1 and Device2

For high frequency power LDMOSFET, it is important to see its current gain variation with frequency to determine transit frequency of the device. Transit frequency (f_T) of a MOSFET is expressed as; $f_T = g_m/(2\pi (C_{gs}+ C_{gd}))$, where g_m is the transconductance, C_{gs} is gate-source capacitance, and C_{gd} is gate-drain capacitance. In order to improve the transit frequency, device capacitances should be minimized. Fig. 7 gives frequency response of both the devices. The transit frequency of Device1 and Device2 are found to be 6.7 and 8.1 GHz, respectively. In other words, transit frequency of Device2 is 21% higher as compared to Device1. This improvement in frequency response of the proposed structure is due to reduced C_{gs} and C_{gd}. These capacitances of both the structures are compared in Fig. 8. It is observed that the proposed device provides much lower capacitances due to thicker field-oxide with low-κ dielectric as compared to the conventional device.

IV. Conclusion

An $In_{0.53}Ga_{0.47}As$ based power LDMOSFET structure is presented. The proposed device uses a thicker field-oxide with low dielectric constant material to improve the performance. Based on 2D numerical simulations, it is demonstrated that the proposed structure provides 50% increase in breakdown voltage, 21% increase in transit frequency and 72% improvement in figure-of-merit when compared with the conventional LDMOSFET. However, drain current and ON-resistance of the proposed device degrade at higher gate bias due to formation of an accumulation layer in the conventional device. The proposed structure is a suitable power MOSFET for power integrated circuits and high frequency power amplifier applications.

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