Dynamic Variation in Nano-Scale CMOS SRAM Cells Due to LF/RTS Noise and Threshold Voltage

M. Fadlallah, G. Ghibaudo, C. G. Theodorou

Abstract—The dynamic variation in memory devices such as the Static Random Access Memory can give errors in read or write operations. In this paper, the effect of low-frequency and random telegraph noise on the dynamic variation of one SRAM cell is detailed. The effect on circuit noise, speed, and length of time of processing is examined, using the Supply Read Retention Voltage and the Read Static Noise Margin. New test run methods are also developed. The obtained results simulation shows the importance of noise caused by dynamic variation, and the impact of Random Telegraph noise on SRAM variability is examined by evaluating the statistical distributions of Random Telegraph noise amplitude in the pull-up, pull-down. The threshold voltage mismatch between neighboring cell transistors due to intrinsic fluctuations typically contributes to larger reductions in static noise margin. Also the contribution of each of the SRAM transistor to total dynamic variation has been identified.

Keywords—Low-frequency noise, Random Telegraph Noise, Dynamic Variation, SRRV.

I. INTRODUCTION

THE nano-sized reduced CMOS enabled the creation of smaller, fast, low-voltage surface circuits [1]-[3]. However, since the oxide zone is reduced, the variability of the parameters from one device to the other is improved due to process variations, which in turn results in the variability of the circuit performance [4]. Moreover, in addition to the spatial variability, the amplitude of the time-dependent dynamic variation of the device parameters such as the threshold voltage is also increased, due to the magnification in low-frequency noise (LFN) [5] and the random telegraph noise (RTN) [6]-[8] with smaller area. This kind of variation can give power limitations, memory problems, and phase jitter/noise problems [9]-[11].

In this paper, we study the SRAM dynamic variation as a function of the intrinsic noise of the transistors, both by measurements and simulations.

II. RESULTS AND DISCUSSION

The six transistors SRAM cells used in this paper come from a 28 nm CMOS technology. The most important is the choice to measure SRAM cells with a minimum surface area ($0.12\ \mu m^2$), to better observe the noise phenomena.

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Simulations were developed using a SPICE model that precisely describes the specific behavior of the devices, while measurements are made by using the Agilent B1530A .

Fig. 1 shows a typical SRAM six-transistor, as used in our measurements and simulations. Table I gives us some abbreviations.

TABLE I
NOMENCLATURE

Symbol	Abbreviation
L,R	left and right
BL	Bit-Line
PG	Pass-Gate
PD	Pull Down
PU	Pull-Up
WL	The two-bit versions (0 and 1) are written using the write line and stored at the CH and CL nodes
RSNM and WSNM	the static read and write noise margin
SVNM	the static voltage noise margin
SRRV	read retention voltage

In this work, we focus on SRRV and RSNM metrics that can provide a representative overview of the dynamic stability of SRAM cells.

A. Supply Read Retention Voltage - SRRV

The SRRV is defined as the maximum allowable reduction of the supply voltage of the cell for which readability is not affected. Fig. 2 shows the time-domain polarization configuration of the VBL (L) (Fig. 2 (a)) and the VCELL (Fig. 2 (b)) to correctly monitor the SRRV. During the measurement, the WL and the BLR are biased to VWL = VBL (R) = 1 V. An initial time is required for the pre-charge of 0, for example to the left bit node (CL), then VBL is constant at 1V, while VCELL is reduced to read IBL bit line current.

In Fig. 2 (c), we show that, at some point, the stored bit is returned and IBL falls sharply, becoming much lower and equal to the I_PG. The VCELL value at this point is called Vflip, and SRRV is extracted such as SRRV = 1-Vflip.

To measure the dynamic variation of SSRV, we have applied the principle of Fig. 2 periodically, so that the voltage slope is repeated until the total time of the measurement always gives 10 s. Two SRAM cells with a noticeable variation in behavior were measured. Fig. 3 (a) shows the IBL-VCELL characteristic curve for cell # 1, with tfall = 5 ms. SRRV variation in the time domain is clearly noticed, but it does not exceed 5 mV, which means that the specific cell has low levels of low frequency noise. In contrast, the SRRV variation of cell # 2 for the same fall (see Fig. 3 (b)) reveals a higher noise than cell # 1, an effect related to the high

variability of CMOS noise at the nanoscale [12]. In addition, some curves do not fit with the rest due to TN noise.
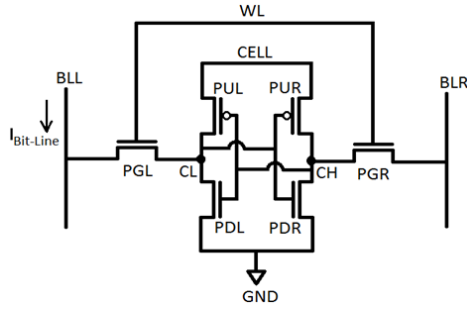

Fig. 1 Typical SRAM cell schematic: R stands for Right, L for left, PU for pull-up, PD for pull-down, PG for pass-gate, BL for bit-line and WL for word-line
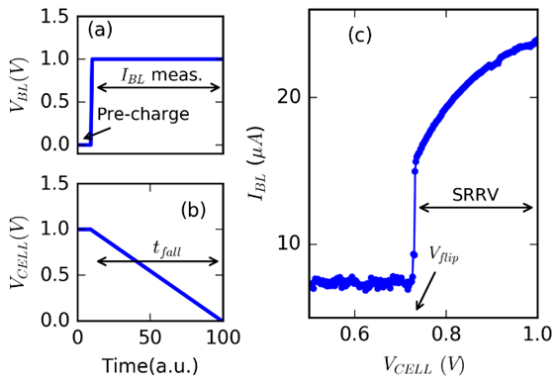

Fig. 2 Setup for measuring the Supply Read Retention Voltage: (a) Bit-line voltage and (b) Cell supply voltage versus time. (c) Measured SRAM cell bit-line current versus cell supply voltage: the supply read retention voltage is extracted as the difference between power supply (1 V) and data flip voltage V_{flip}

To check this hypothesis, we do a much faster measurement on cell 2 with tfall = 5 μs. The results are presented in Fig. 3 (c). It is to be noticed that we have two set of curves with discrete mean values of the IPG, showing that a transistor in the cell has a higher RTN amplitude. The comparison between Figs. 3 (b) and (c) show, on the one hand, the importance of the measurement speed for the detection of the RTN of a circuit and, on the other hand, the dependence of the SRRV on the speed operating a circuit.

In order to better estimate the SRRV dynamic variation by comparison with cell-to-cell variations due to a threshold voltage difference, an IBL-VCELL Monte Carlo simulation was developed for 100 cells by taking into account typical values of σ (ΔVt) for this technology [11]. As shown in Fig. 4, the cell-cell SRRV variability is significantly higher than the single-one dynamic variation measured in Fig. 3 (c). Also, note that dynamic variations can reach about 10-20% of local mismatch variations, which underlies the importance of the dynamic variation phenomena. In order to further monitor the impact of noise level and operating speed on the SRRV dynamic variation, we do a series of IBL-VCELL simulations,

a portion of which is illustrated in Fig. 5. The LFN level of the transistors was controlled by the SVfb flat-band voltage fluctuations which express the level of flicker noise due to entrapment-trapping of the carriers in the oxide traps [5], through (1):
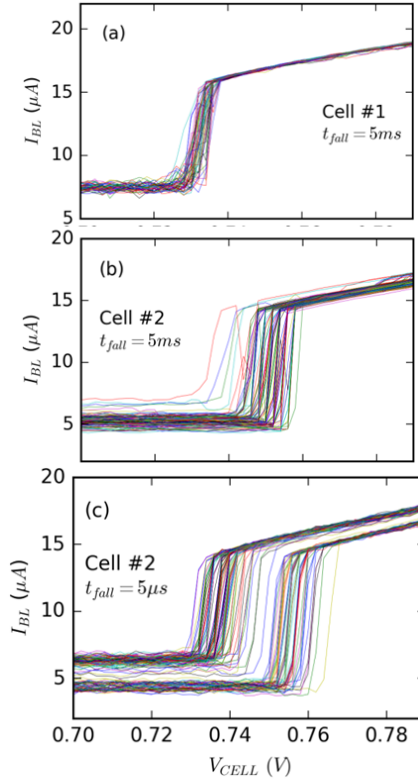

Fig. 3 Measured SRAM cell bit-line current versus cell supply voltage for three different cases: (a) Cell #1: low noise level, (b) Cell #2, slow ramp: higher noise level and strange behavior, (c) Cell #2, fast ramp: higher noise level and clear presence of RTN
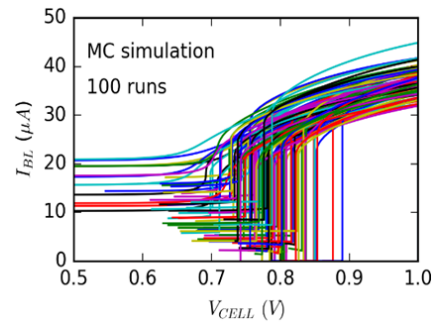

Fig. 4 Monte-Carlo simulation of the bit-line current versus cell supply voltage taking into account the threshold voltage mismatch

$$S_{Vfb} = \frac{q^2 \lambda kT N_t}{WLC_{ox}^2 f^\gamma} \qquad (1)$$

where λ is the tunneling constant in the dielectric, Nt the slow oxide trap densitiy, Cox the gate oxide capacitance per unit area, kT the thermal voltage and f the frequency.
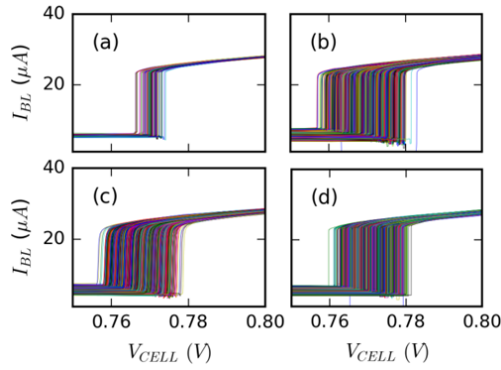
Fig. 5 Periodic transient noise simulation results of the bit-line current versus cell supply voltage for four different configurations: (a) Reference simulation, (b) S_{Vfb}* 100, (c) t_{fall} / 1000, (d) t_{stop} * 100
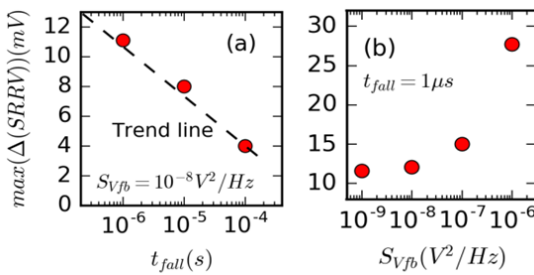

Fig. 6 Maximum variation of SRRV: (a) versus fall time of cell supply voltage ramp and (b) versus flat band voltage power spectral density

A reference simulation with S_{Vfb} = 10-8 V2 / Hz, stopping time tstop = 10 ms and Vcell drop time tfall = 0.1 ms is presented in Fig. 5 (a). Same to Fig. 3 (a), a small variability of SRRV can be shown. In these simulations of Figs. 5 (b), (c) and (d), only one of the three parameters has been modified to explain the influence of each separately. In Fig. 5 (b), the noise level is higher to S_{Vfb} = 10-6 V2, in concordance with the LFN variation experiments of this technology. In Fig. 5 (c), the VCELL descent time was reduced to tfall = 1 μs to increase the operating speed, and in Fig. 5 (d) the simulation dwell time was increased to tstop = 1 s to include the noise contribution from the lower part of the frequency bandwidth. In all cases, with respect to the reference one, a significant increase in SRRV dynamic variation is obtained. Based on the above, we conclude that the SRAM dynamic variation increases with the LFN level of the transistor and the operating speed of the circuit. The max deviation of the SRRV from its typical value is drawn against the tfall in Fig. 6 (a). From the trend of the extracted data, it may be suggested that in high speed operation (above 1 MHz) the SRRV of a single SRAM cell may decrease by more than 15 mV. This simulation was done by taking the average noise level for these transistors, that is to say S_{Vfb} = 10-8 V2 / Hz. In reality, the noise level of a small transistor can also be two orders of magnitude higher or lower, due to the improved variability of LFN [12]. In Fig. 6 (b), we can see the dramatic impact of the increase in the LFN level on the SRRV change. The reason why there is a horizontal obtained in lower values is the presence of the thermal noise.

B. Read Static Noise Margin - RSNM

The RSNM is an equally important stability metric for SRAM cells [4]. It represents the maximum tolerable DC noise voltage on each storage node before causing a loss of reading. As far as measurement is concerned, it requires a more complicated procedure, with respect to the simple one of SRRV measurement, because it requires a high-speed voltage monitoring, requires access to internal nodes and takes place in two stages. RSNM simulation, however, is much easier to perform than SRRV and can also be used to study SRAM dynamic variability behavior.

Using the same methodology for SRRV, we applied Monte Carlo simulations and mismatched periodic transient noise (PTN) to capture local and time domain RSNM variations. Fig. 7 shows a selection of simulation results above. From Fig. 7 (a), it can be seen how the RSNM can be reduced by more than 50% from one cell to another due to the difference in threshold voltage. The noise-induced dynamic variation of a single SRAM cell, on the other hand, as shown in Fig. 7 (b), can lead to a reduction in RSNM of up to 20%. For this last simulation, the noise level of the device has been increased by two orders of magnitude, in order to take into account worse scenario, which is to have a huge LFN variability or the presence of high amplitude RTN. Fig. 8 shows the dependence of the RSNM reduction (expressed as a% of the average value) on the valve. It is obvious that a single operating speed of the SRAM cell can drastically reduce the RSNM by 30%, approaching the reduction caused by local Vt variations.
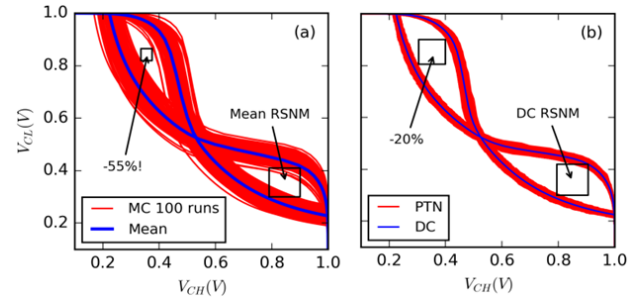

Fig. 7 (a) Impact of Vt mismatch on RSNM, (MC: Monte Carlo), (b) Impact of LFN on RSNM (PTN: Periodic Transient Noise)

III. CONCLUSION

The impact of low frequency noise of nanoscale CMOS on the dynamic operation of SRAM cells has been studied. The dynamic variation of SRRV and RSNM was used to study the effect in both the experimental and simulation aspects. SRAM dynamic variation has been found to increase with noise level and operating speed. It has also been shown that the time domain variability of high speed SRAM cells can reach levels similar to those of cell-to-cell SRAM variations due to a threshold voltage difference. Finally, each contribution of the SRAM transistor to total dynamic variation has been identified for both SSRV and RSNM.

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