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Design and Implementation of TMS320C31 DSP and FPGA for Conventional Direct Torque Control (DTC) of Induction Machines

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***Abstract*–**This paper introduces a new digital logic design, which combines the DSP and FPGA to implement the conventional DTC of induction machine. The DSP will be used for floating point calculation whereas the FPGA main task is to implement the hysteresis-based controller. The emphasis is on FPGA digital logic design. The simulation and experimental results are presented and summarized.

Keywords—**DTC, DSP, FPGA, induction machine**

I. Introduction

Recent successful digital logic design requires a combination of both high resolution and high sample rates. Traditional DSP processors are not generally suitable for the technique due to their fixed resolution and the processing burden [1]. Application-Specific-Integrated Circuit (ASIC) allows optimized design for a specific task. It is possible to include a larger amount of logic circuitry in a custom chip and leads to a better performance. However, the manufacturing takes a considerable amount of time, on the order of months. In contrast, the Programmable Logic Devices (PLD) offers a more realistic alternative. One of the most sophisticated types of PLD is known as Field Programmable Gate Arrays (FPGA). It is a general purpose, multi-level programmable logic device. It can significantly reduce design risk since a design error can be corrected immediately and intensively by reprogramming the FPGA without any manufacturing delays [1], [2]. Nonetheless, the application of FPGA in motion control is not popular. The root cause is FPGA is not suitable for floating point calculation. Arithmetic operations using floating-point operands are significantly more complex. This will increase the computation burden. In [3] – [8], researchers had refined the floating-point number to a fixed-point format. However, new technological problems appeared, requiring digital properties need considering, such as quantization, sampling, word length and data types.

This paper introduces a new digital logic design, which combines the DSP and FPGA to implement the conventional DTC of induction machine. In order to avoid the quantization problems, the DSP will be used for floating point calculation to estimate the torque and stator flux. The main task of the FPGA is to implement the hysteresis-based controller. Besides, the FPGA is also responsible in selecting a proper voltage vector and implementing the blanking time for the inverter. The rest of this paper is organized as follows. Section II briefly gives the design methodology. Section III describes the digital logic design of the conventional DTC. Section IV represents the simulation and experiment results. Finally, conclusions are given in section V.

II. Design Methodology

Very high-speed integrated circuits, Hardware description language (VHDL) is chosen for describing digital circuits in this paper. It is an official IEEE standard which was originally intended to serve two main purposes, i.e. documentation and simulation. It is a technology independent language where the same algorithm can be synthesized into any other FPGA and even has a possible direct path to silicon.

Basically, the digital logic design is started from generate an initial design which hit the specific goal with the assist of necessary Computer Aided Design (CAD) tools [2]. CAD tools not only help to design incredibly complex circuits but also made the design work much simpler in general. Next the simulation of the design is carried out. If the simulation reveals some errors, then the design must be changed and simulated again. When, the simulation indicates a successful design then the designed circuit is ready for physical implementation.

In this paper, 3 softwares are used. VHDL Module Generator (VHDLMG) is used to generate the VHDL source codes in synthesizable form. The codes are then pass to the FPGA Express for synthesis. Finally, the codes are compiled and simulated by MAX+plussII software. The design is then downloaded to the FPGA (EPF10K20) device for hardware testing. The ByteBlaster download cable channels configuration data between the MAX+PLUS II software and the FPGA.

III. Implementation Of The Conventional DTC

DTC is first introduced by Takahashi in the past decade [9]. It is simple as shown in Fig. 1. It consists of a pair of torque and flux hysteresis controllers, voltage vector selection table, torque and flux estimator and a VSI. Fig. 2 shows the block diagram of the experimental set-up. The main components for the implementation of the proposed DTC consist of a digital signal processor board DS1102 from dSPACE (TMS320C31 at 60 MHz) and an Altera UP1 Education Board (EPF10K20). The DSP performs two major tasks, i.e. estimates the stator flux and torque, and determines the stator flux orientation. Due to the lack of I/O pins on the

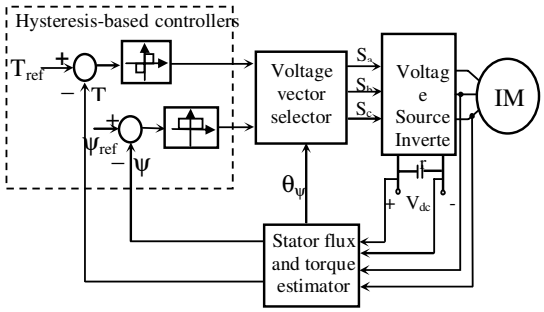


Fig. 1: Hysteresis-based DTC

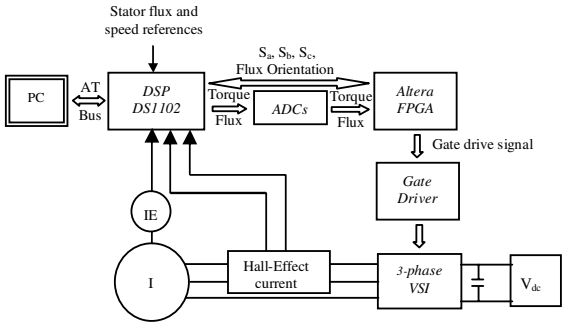


Fig. 2: Block diagram of the experiment set-up

DSP board, two external ADCs are required to pass the stator flux and torque error signals to FPGA.

The functional block diagram of the tasks performed by the Altera FPGA is shown in Fig. 3. A synchronous control of two ADC is designed to ensure that the torque and flux error signals are passed to the FPGA simultaneously. A pair of 8-bits register will capture the data from ADC once the data is valid. The torque error signal will be sent through the torque controller to generate the appropriate torque logic status. Meanwhile, the flux controller will compare the flux error signals and give the flux logic status. DSP will pass the flux orientation to the FPGA directly and store in a 3-bits register. In order to avoid the glitch problem, which may cause instability to the system, a 6-bits register is placed in front of the ROM. It will hold the torque error status; flux error status and stator flux orientation and then pass to the ROM address. The 64-by-3 ROM memories are required to tabulate the Takahashi's voltage vector selection table (Table I). The three bit outputs of the memory element are passed to the blanking time generator before they are fed to the gate drivers. The following section discusses three modules above in more details, they are:

- Synchronous control of two ADC
- Torque and flux controllers
- Blanking time generation

A. *Synchronous control of two ADC*

Fig. 4 draws the functional block diagram of the synchronous control of two ADC. Referring to the stand-alone operation's timing diagram of the AD7821 (Fig. 5), an INTERRUPT

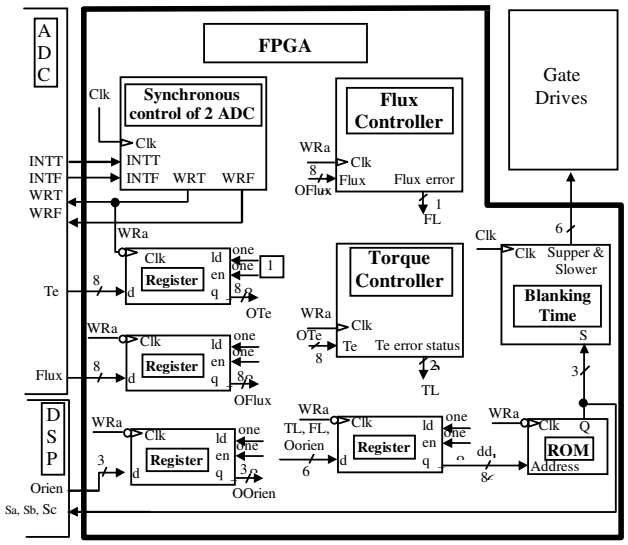


Fig. 3: Functional block diagram of Altera FPGA design

TABLE I
VOLTAGE VECTOR SELECTION TABLE

Stator Flux Error Status	Torque Error Status	Sector					
		I	II	III	IV	V	VI
0	1	110	010	011	001	101	100
	0	111	000	111	000	111	000
	–1	011	001	101	100	110	010
1	1	100	110	010	011	001	101
	0	000	111	000	111	000	111
	–1	001	101	100	110	010	011

signal, $\overline{INT}$ will turn to zero indicates that the conversion is complete. Therefore, a pair of 1-bit register is designed to latch the $\overline{INT}$ signal. When the ADCs' $\overline{INT}$ signal go LOW, and the WRITE signal, $\overline{WR}$ is HIGH then the latch will output a LOW signal. The CTRL module is initialized by a LOW signal from the output of the OR gate. The flow chat of the CTRL module is shown in Fig. 6. FPGA will ready to get the data from ADC when $\overline{WR}$ goes LOW.

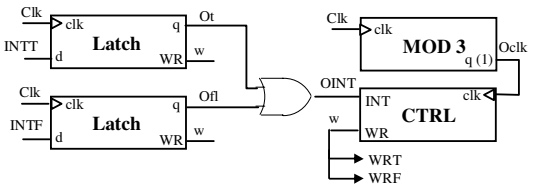


Fig. 4: Functional block diagram of the synchronous control of two ADCs

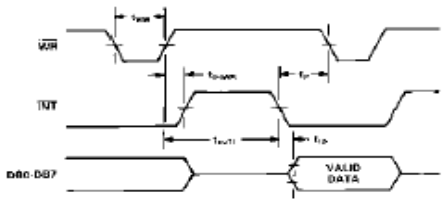


Fig. 5: AD7821 stand-alone operation

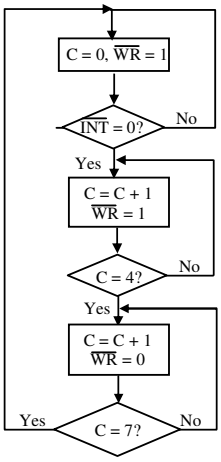


Fig. 6: The flow chart of the CTRL module

B. Torque and flux hysteresis-based controllers

Both the torque and flux controllers are responsible to generate the appropriate torque error status and flux error status. The torque and flux error signals will pass through the 3-level and 2-level hysteresis comparators respectively. Fig. 7 shows the functional block diagram for torque and flux hysteresis-based controllers. The hysteresis comparators are designed using sequential assignment statements, called if-then-else statements, which is placed inside a process statement. In order to ensure proper operation, the comparator is set to operate when an active clock edge occurs.

Since the error signals are fed by DSP via DAC outputs and then converted back to digital form by external ADCs before sending to FPGA, hence some proper scaling have to be made (Fig. 8). Both the hysteresis bands of the 2-level and 3-level hysteresis controllers are set to "11110111" for the upper bound and "00001001" for the lower bound with the purpose to fully utilize the 8-bits ADC.

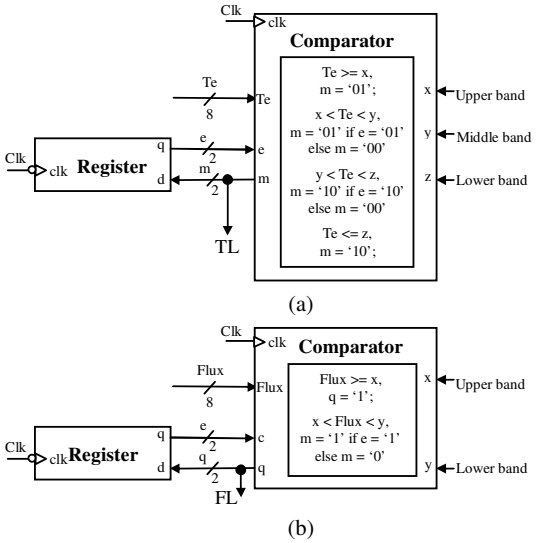


Fig. 7: Functional block diagram for (a) torque and (b) flux hysteresis-based controllers

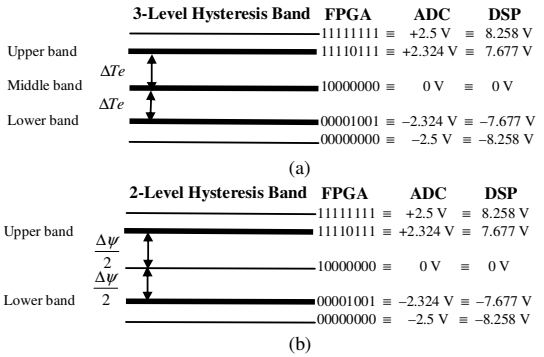


Fig. 8: The scaling of the boundary (a) torque loop – 3-level hysteresis band, (b) flux loop – 2-level hysteresis band

The DSP output is scaled down with 0.30275 to match the input range of ADC. It is found that the DACs inside the DSP will create a signal 10 times larger than the original; hence the calculations for the appropriate gain of *V/Wb* or *V/Nm* for the hysteresis bands are as follows:

If the hysteresis band of the torque loop is set to 10% of the rated torque,

$$\begin{aligned}\text{The upper band} &= 10\% \times 0.6184\ Nm \\ &= 0.06184\ Nm\end{aligned}$$

$$\begin{aligned}\text{Gain} &= \frac{7.677/10\ V}{0.06184\ Nm} \\ &= 12.414\ V/Nm\end{aligned}$$

Same calculation for the flux loop, i.e.
If the hysteresis band of the flux loop is set to 10% of the rated flux,

$$\begin{aligned}\text{The upper band} &= ½ \times 10\% \times 0.495\ Wb \\ &= 0.02475\ Wb\end{aligned}$$

$$\begin{aligned}\text{Gain} &= \frac{7.677/10\ V}{0.02475\ Wb} \\ &= 31.018\ V/Wb\end{aligned}$$

C. Blanking time generation

A blanking time of at least 2 μs is required to avoid short circuit within a leg. A pair of 16-bits counter and 16-bits comparator constructs the blanking time generator for a single leg (Fig. 9).

The signal S indicates one of the 3-bits outputs from ROM. MOD-13 counter is designed to divide the general clock frequency to 516.39 ns. The upper counter will start counting when the S is High while the lower counter is initialized by a Low signal. Fig. 10 illustrates the timing diagram of its operation. Signal 'a' and 'c' draw the output of the counter. Comparing signal 'a' and 'c' with signal 'b' determine the blanking time.

Increasing the value of 'b' will enlarge the blanking time. By setting the 'b' to a value of 4, the blanking time is

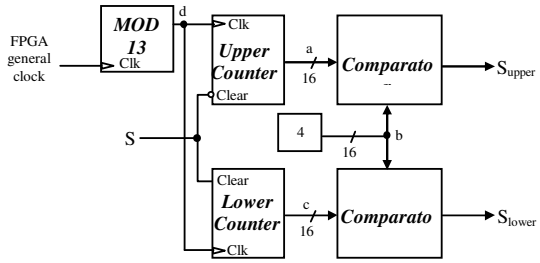


Fig. 9: Block diagram of blanking time generator

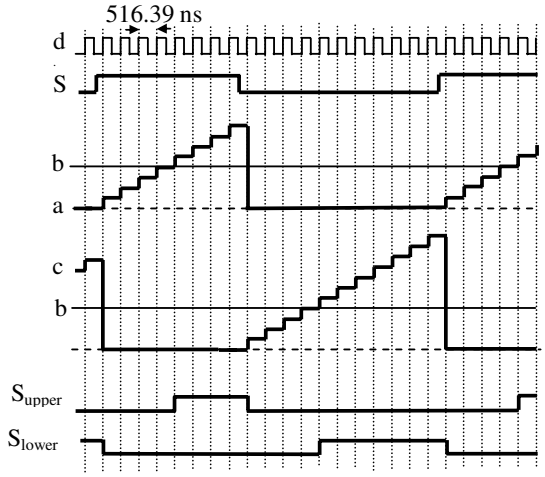


Fig. 10: Timing diagram of the blanking time generation

approximated to 2 µs. Signals S_{upper} and S_{lower} are then fed to the upper and lower devices of a VSI leg. The same blanking time circuit is duplicated for the other 2 phases. Finally, the 6 generated signals are fed to the six gate driver circuits.

IV. Simulation & Experimental Results

This section will show the simulation results of the digital logic design that had been discussed thoroughly in Section III. The simulations are done by using MAX+plusII. Fig. 11 shows the simulation result for the synchronous control of 2 ADCs. It is found that the result is fulfilled the design need, where the CTRL module is initialized when both INTT and INTF signals had gone LOW as discussed previously. The WRT signal will be used as a clock signal, WRa for others module in Fig. 3. When WRa goes LOW, a pair of 8 bits register will get the data from the ADCs and pass to the 2-level and 3-level hysteresis comparators.

Fig. 12 illustrates the simulation result for the torque hysteresis comparator. Signal a, b and c represent the upper, middle and lower bands of the hysteresis comparator with the value of 11110111_2 (247_{10}), 10000000_2 (128_{10}) and 00001000_2 (9_{10}) respectively. The comparator is synchronous with the clock signal, CLK. The input data, Te is compared when an active clock edge occur. The torque error status, Tl holds the value of 10_2 until the input signal, Te greater than 128. When Te goes beyond the upper band (247) then Tl will automatically give the output of 01_2.

In DTC, small torque hysteresis band is ideal to produce a

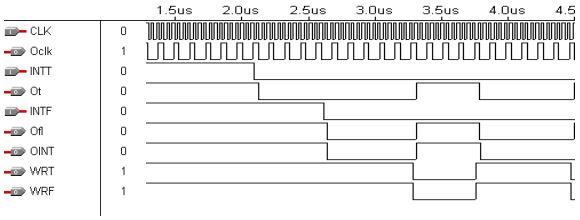


Fig. 11: The simulation result for the synchronous control of 2 ADCs

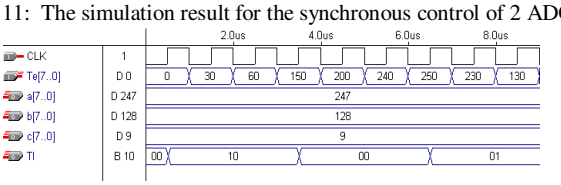


Fig. 12: The simulation result for the 3-level hysteresis comparator

smooth torque. However for microprocessor-based implementation, if the hysteresis band is set too small, the torque may overshoot and touch the upper band. Once it exceeds the upper band the hysteresis comparator will produce a signal that will select a reverse voltage vector instead of zero voltage vector to reduce the torque [10], [11]. Due to this incorrect voltage vector selection, the undershoot may occur and as a result, the torque ripple is increased drastically. When Tl equivalent to 10_2 a reverse voltage vector will be selected meanwhile 00_2 and 01_2 indicate that zero voltage vector and active voltage vector will be chosen.

An experimental test is performed to a ¼ HP squirrel cage induction machine. The widths of the flux and torque hysteresis band are set to 10% of their rated values respectively. The torque reference set to 1.04 Hz ±0.6 Nm. Fig. 13 illustrates the experiment result of the estimated torque with the torque reference (upper trace) and torque error status (lower trace). Although the hysteresis torque band amplitude is set to 10% of the rated torque, but owing to the delay in feedback signal, a reverse voltage vector is selected [12]. As a result the torque ripple increases. Fig. 14 shows the torque response of the conventional DTC, which is inconsistent and contains large torque ripple due to the selection of reverse voltage vector.

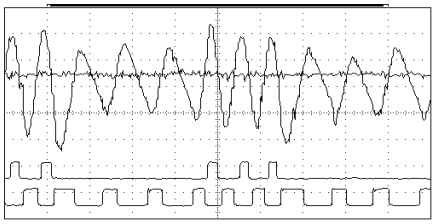


Fig. 13: The experiment result for the 3-level hysteresis comparator

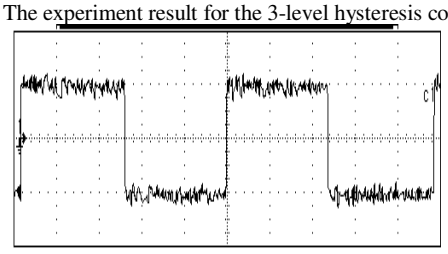


Fig. 14: Torque response for hysteresis-based controller [0.6 Nm/div]

The flux hysteresis comparator works similar to the torque hysteresis comparator. Fig. 15 demonstrates the simulation result. The upper band, a, and lower band, b, are set at 11110111_2 (247_{10}) and 00001000_2 (9_{10}). Once the input data, Flux is greater than 247 the flux error status, Fl, will output 1 and Fl will hold the output signal until the input data below the lower band. Fig. 16 gives the experimental result of the flux hysteresis comparator.

In DTC, the stator flux is forced to follow the reference value within a hysteresis band. In [9], it is proposed that the stator flux plane is divided into six sectors. Each sector will have a different set of voltage vectors to increase (Fl =1) or decrease (Fl = 0) the stator flux. Therefore, the magnitude and orientation of the stator flux must be known in order to directly control the stator flux by selecting appropriate voltage vector. Ideally, small flux hysteresis band reduces current distortion [13]. Since the hysteresis band is set to 10 % of the rated flux, the stator flux locus contains high ripple and consequently produces high ripple current, which contains a lot of harmonic components (Fig. 17).

Fig. 18 and Fig. 19 clearly show that a blanking time of at least 2 μs had been achieved in simulation and experiment respectively. The line-line voltage and the frequency spectrum of the switching pattern, S_b are demonstrated by Fig. 20. The switching frequency of the hysteresis-based controller is inconsistent therefore the harmonic components are widely distributed.

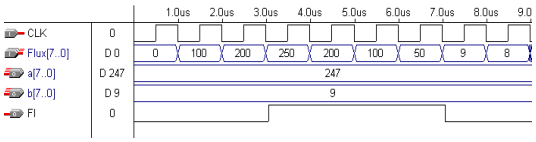


Fig. 15: The simulation result for the 2-level hysteresis comparator

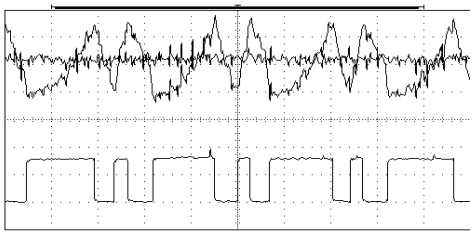
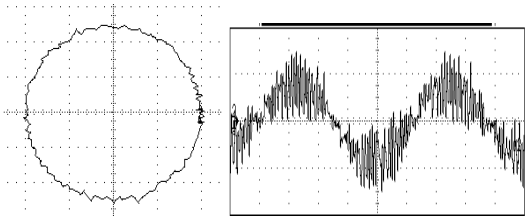


Fig. 16: The experiment result for the 2-level hysteresis comparator



(a) (b)

Fig. 17: The experiment result for (a) stator flux locus [0.2 Wb/div], (b) Steady state phase current (0.5714A/div)

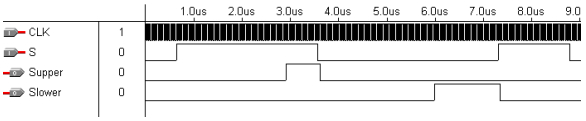


Fig. 18: The simulation result for the blanking time generator

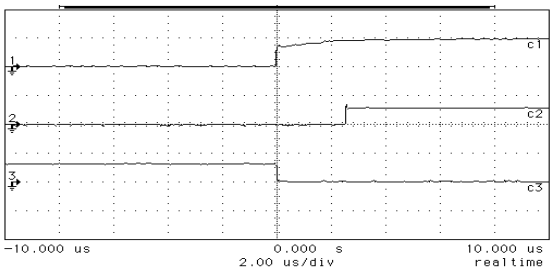
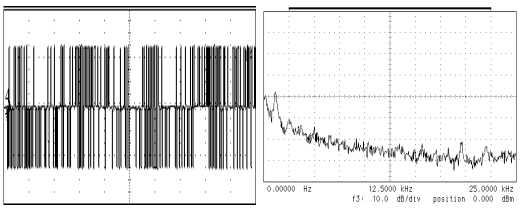


Fig. 19: The experiment result for the blanking time generator, Upper trace: S, middle trace: Supper, lower trace: Slower



(a) (b)

Fig. 20: (a) Line-line voltage (100V/div), (b) Frequency spectrum of the switching pattern, S_b [Horizontal: 2.5 kHz/div, vertical: 10 dB/div.]

V. Conclusion

This paper presents the design and implementation of a DSP and FPGA based conventional DTC. A thoroughly description of FPGA digital logic design had been given. The design is then verified by the simulation and experimental results.

Appendix

Parameters of Induction Machine

Stator resistance	10.9 Ω
Rotor resistance	9.5 Ω
Stator self inductance	0.859 H
Rotor self inductance	0.859 H
Mutual inductance	0.828 H
Rated speed	2880 rpm
Pole pair	2
DC link voltage	120 V
Rated flux	0.495 Wb

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