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Depletion Layer Parameters of Al-MoO_3-P-CdTe-Al MOS Structures

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***Abstract*—**The Al-MoO_3-P-CdTe-Al MOS sandwich structures were fabricated by vacuum deposition method on cleaned glass substrates. Capacitance versus voltage measurements were performed at different frequencies and sweep rates of applied voltages for oxide and semiconductor films of different thicknesses. In the negative voltage region of the C-V curve a high differential capacitance of the semiconductor was observed and at high frequencies (<10 kHz) the transition from accumulation to depletion and further to deep depletion was observed as the voltage was swept from negative to positive. A study have been undertaken to determine the value of acceptor density and some depletion layer parameters such as depletion layer capacitance, depletion width, impurity concentration, flat band voltage, Debye length, flat band capacitance, diffusion or built-in-potential, space charge per unit area etc. These were determined from C-V measurements for different oxide and semiconductor thicknesses.

***Keywords*—**Debye length, Depletion width, flat band capacitance, impurity concentration.

I. Introduction

THE MIS structure is the most useful device in the study of semiconductor surfaces. It is extensively used in many electronic planar devices and integrated circuits. Since the reliability and stability of all semiconductor devices are intimately related to their surface conditions, an understanding of the surface physics with the help of MIS structures is of great importance to device operations [1]. Thin films dielectric materials are finding increasing application in micro electric devices. An initial investigation concerning the temperature and thickness dependence of the electrical properties of evaporated dielectric films was reported by various researchers. MoO_3 belongs to a group of transition element compounds. Transition metal oxides make up a technologically important class of compound. The combination of large band gap, high average atomic number and reasonable mobility- lifetime for both electrons and hole make CdTe and attractive material. CdTe films are known to yield anomalously large photovoltages and the material can be used in the fabrication of solar cell. Studies of MOS capacitors enable the determination of bulk and surface generation and of the interface state density. Investigations had been carried out by several workers [2]-[6] on MIS structures taking different insulators and semiconductors in an encapsulation of different electrodes. In the present work, we are going to report some depletion layer parameters of the Al-MoO_3-P-CdTe-Al structures where oxide thicknesses were in the range 18 to 43 nm and semiconductor film thickness were between 90.0 to 192.5 nm and of device area between 8500 to 11000 nm^2.

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II. Experimental

A. Film Preparation

The Al|MoO_3|P-CdTe|Al sandwich structures were fabricated on cleaned glass substrate by the vacuum evaporation technique. Molybdenum oxide (purity 99.90%) was deposited over aluminum electrode of thickness between 140 to 160 nm. The rate of deposition of MoO_3 was varied from 0.023 to 0.033 nm S^{-1}. The oxide films were stored in dry air for 2-3 days. Then CdTe semiconductor films of thickness between 90 to 192.5 nm were deposited on MoO_3 films at 300 K. The rate of deposition of CdTe films were varied from 0.6 to 1.6 nm S^{-1}. The CdTe film was covered with aluminium film depositing directly from a tungsten helix. All thin films were deposited at a pressure of 2×10^{-5} Torr. The structures were then annealed in air at about 323 K for 2-3 hours and stored for a week in dry air to obtain stabilized characteristics.

B. Area and Thickness Measurement

The oxide film thickness was measured capacitively at 1 kHz taking the high frequency dielectric constant as 5.3 [7]. The aluminum and semiconductor film thickness was measured using Tolansky technique and the effective area by travelling microscope.

C. Capacitance-Voltage Measurements

C-V measurements within the frequency range of 0.3 to 50 kHz were performed in a circuit consisting of a DC source, a potential divider, an electronic voltmeter and a capacitance bridge (Marconi TF 2700). An external audio frequency generator was employed to energize the bridge. The bias voltage was swept from -5 to +5 Volt. All measurements were carried out in a darkened chamber having pressure ~ 10^{-2} Torr.

III. Results and Discussion

A. The C-V Characteristics

The measured steady state capacitance-voltage characteristics of Al-MoO_3-CdTe-Al MOS structures [Fig. 1] indicated that the field effect was occurring in the structure. Evaluation of MOS characteristics was carried out using both low and high frequency C-V measurements. In the negative voltage of the C-V curve a high differential capacitance of the semiconductor was observed which might be due to the accumulation of holes in the semiconductor and as a result, the total capacitance was close to the insulator capacitance. As the

negative voltage was reduced, a depletion region was formed near the semiconductor surface, which acted as a dielectric in series with the insulator. The capacitance passed through a minimum and then increased again as the inversion layer of electrons formed at the surface. From the low frequency C-V curve for p-type CdTe, as the gate bias is made more positive (or less negative), the capacitance goes down slowly in depletion and then rises rapidly in inversion. As a result, the low frequency C-V is not quite symmetric in shape. The increase in capacitance depends on the ability of the electron concentration to follow the applied AC signal. This only happens at low frequencies, where the recombination generation rates of minority carriers (here electrons) could keep up with small signal variation and lead to charge exchange with the inversion layer in step with the measurement signal. Unlike depletion and weak inversion, at strong inversion the incremental charge is no longer at the edges of the depletion region but at the semiconductor surface inversion layer, resulting in a large capacitance.

The observed increase in capacitance in the low frequency C-V curve might be caused by the generation of carriers either by tunneling processes or by avalanche breakdown [2] that might have taken place in the depletion region of narrow gap semiconductor. With the increase in positive voltage, the depletion region widens which acts as a dielectric at the semiconductor surface in series with the insulator, and the total capacitance continues to decrease [9].

The semiconductor surface showed the transition from accumulation to depletion and further to deep depletion as the voltage was swept from the negative to the positive at high frequency for P-type CdTe. Deep depletion occurs when the depletion width is wider than the maximum value at equilibrium. At higher voltages, impact ionization can occur in the semiconductor. This is due to the carrier lifetime and thermal generation rate in the semiconductors [8]. When applied voltage increases, the surface potential and depletion width increases, the surface inversion will occur. Once strong inversion occurs, the depletion-layer width reaches a maximum then the semiconductor is effectively shielded from further penetration of the electric field.

The fall of capacitance observed in the C-V characteristic in the voltage range -1 to +4 volt was found to conform to the relation C^{-2} α V, at high frequency (>1 kHz). A way to verify that the CdTe surface is actually depleting is to plot $1/C^2$ versus V in this region [Fig. 2]. These plots yielded straight line. From the slope and using [9]

$$\frac{d}{dV}\frac{1}{C^2} = -\frac{2}{q\,\epsilon_S\,N_A} \quad (1)$$

the doping or acceptor density, N_A of the semiconductor can be deduced. The permittivity of the semiconductor is ϵ_S and q is the electronic charge. The value of N_A was found to be ~ 10^{24} m^{-3}. The largest hole densities (N_A) reported in the literature for P-CdTe single crystal are around 10^{23} m^{-3} (except for Li doping which is unstable). This large value of N_A could be because of the inclusion of relatively large amount of semi metallic Te [9]. Polycrystalline CdTe is likely to have carrier densities even lower \because of compensation by grain boundary states.

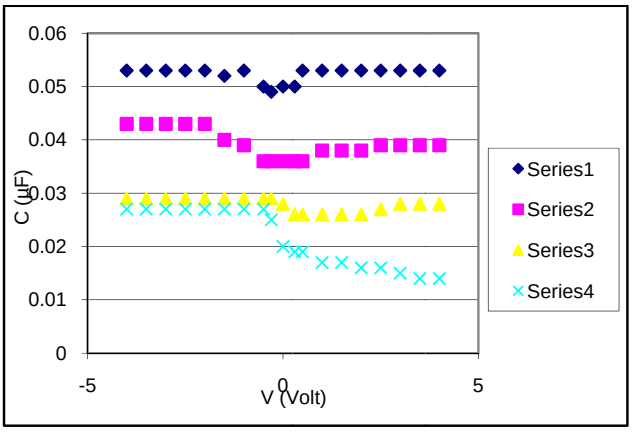

Fig. 1 C-V plots for d_i = 18 nm, 0.3 kHz [Series 1], 1 kHz [Series 2], 10 kHz [Series 3], and 50 kHz [Series 4]

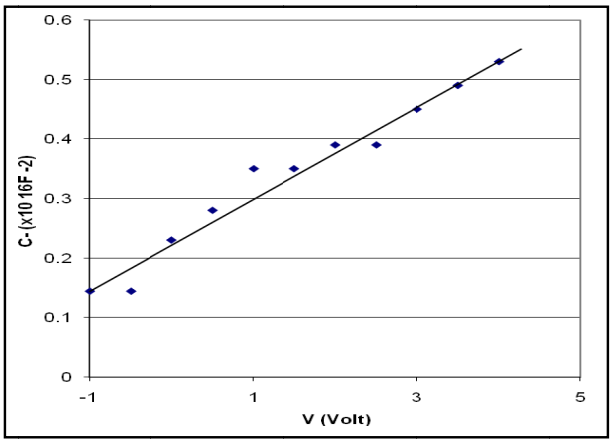

Fig. 2 C^{-2}-V plots for d_i = 18 nm

The flat-band capacitance (C_{FB}) for the MOS structure was calculated using [8]

$$C_{FB} = \epsilon_i A \left[d_i + \frac{\epsilon_i}{\epsilon_s}\left(\frac{kT\epsilon_s}{q^2 N_A}\right)^{\frac{1}{2}} \right]^{-1} \quad (2)$$

and was found to be 0.023 μF. Here, ϵ_i (=$\epsilon_r\epsilon_o$) is the insulator permittivity and ϵ_r = 5.3, the dielectric constant of MoO_3, A = 9500 nm^2, the area of the MOS structure, d_i=18 nm, the oxide thickness, ϵ_s (=$\epsilon_r\epsilon o$) is the semiconductor permittivity and ϵ_r=7.2, the high frequency dielectric constant of CdTe, N_A= 2.90 x 10^{24} m^{-3}, the acceptor density and T = 300 K. From Fig. 1, the flat band voltage was found to be -0.25 V at 50 kHz. The V_{FB} determined the point of transition. It depends not only on the difference between the work function of the gate and that of the semiconductor, but also on the presence in the oxide layer of charges which could be either present in it or subsequently injected into it. The capacitance of the MOS

structure is defined in terms of the capacitance and the interface state capacitance.

B. Depletion Layer parameter

The depletion layer capacitance per unit area is defined as $C \cong dQ_c/dV$, where dQ_c is the incremental change in charge per unit area upon a change of the applied voltage dV. The depletion layer capacitance of a one-sided junction is a function of the doping concentration in the low-doped region.

For one sided abrupt junction, i.e. when the impurity concentration in a semiconductor changes abruptly from acceptor impurities N_A to donor impurities N_D, or if $N_A >> N_D$, the capacitance per unit area is given by [9].

$$C = \frac{dQ_c}{dV} = \frac{d(qN_BW)}{d\left[(\frac{qN_B}{2\,\epsilon_S})W^2\right]} = \frac{\epsilon_S}{W} = \frac{\sqrt{q\,\epsilon_S\,N_B}}{2}\,(V_{bi} \pm V - \frac{2kT}{q})^{-1/2}$$

or

$$C^2 = \frac{q\epsilon_S N_B}{2(V_{bi} \pm V - \frac{2kT}{q})} \quad (3)$$

or

$$\frac{1}{C^2} = \frac{2{L_D}^2}{\epsilon_S}\,(\beta V_{bi} \pm \beta V - 2) \quad (4)$$

or

$$\frac{d(\frac{1}{C^2})}{dV} \cong \frac{2{L_D}^2\beta}{{\epsilon_S}^2} = \frac{2}{q\epsilon_S N_B} \quad (5)$$

where ± signs are for the reverse and forward bias condition respectively and $N_B = N_A$ or N_D depending on whether $N_A >> N_D$ or vice versa. The factor $\beta = q/kT$ and L_D is the Debye length; where Debye length is a characteristic length for semiconductors. The Debye length is defined as

$$L_D = \left(\frac{\epsilon_S kT}{q^2 N_A}\right)^{1/2} = (\epsilon_S/qN_A\beta)^{1/2} \quad (6)$$

which determines the distance over which a small unbalanced charge decays [10]. In semiconductors the space-charge region may extend to a substantial depth about 10^{-6}m and over [11]. This distance is commonly taken equal to the Debye shielding length or Debye length, that describes a path in which the potentials of the field in a substance having free carriers decreases to e^{-1}. For a doping density of $10^{22}m^{-3}$, the Debye length was 40 nm for silicon at room temperature [9].The Debye length is a very important concept in semiconductors. It gives an idea of the distance scale in which charge imbalances are screened or smeared out. If we think of inserting a positively charged sphere in an n-type semiconductor then the mobile electrons will crowd around the sphere. If we move away from the sphere by several Debye lengths, the positively charged sphere and the negative electron cloud will look like a neutral entity. L_D depends inversely on doping because the higher the carrier concentrations, the more easily the screening takes place [12].

It can be shown that the semiconductor capacitance at flat band C_{FB} can be determined from the Debye length capacitance [12].

$$C_{debye} = \frac{\epsilon_s}{L_D} \quad (7)$$

The overall MOS flat band capacitance C_{FB}, is the series of combination of C_{debye} and C_{oxide}. Thus V_{FB} can be determined corresponding to the C_{FB}.

By plotting $1/C^2$ versus V using (1) a straight line should result for a one sided abrupt junction. The slope gives the impurity concentration N_A and the intercept at $1/C^2 = 0$ gives $(V_{bi} - 2\ kT/q)$, from which the diffusion or the built in potential "V_{bi}" and the total depletion width "W" for a one sided abrupt junction determined using the relation [9]

$$W = (\frac{2\epsilon_S V_{bi}}{qN_A})^{1/2} \quad (8)$$

When the applied voltage increases, W increase and the small inversion occurs, the depletion layer width reaches a maximum. The V_{bi} changes only slightly as the doping concentrations changes by orders of magnitude [13].

The space charge Q_{sc} per unit area of the semiconductor also determined using [9]

$$Q_{SC} = qN_AW = \left\{2q\,\epsilon_S\,N_A(V_{bi} - V - \frac{2kT}{q})\right\}^{1/2} \quad (9)$$

Depletion layer parameters namely, C_D, L_D, W, Q_{sc}, V_{bi}, C_{FB}, V_{FB}, and N_A were determined at 300 K and at a frequency 50 kHz have been shown in Table I.

IV. Conclusion

All the parameters and characteristics obtained were found to be reproducible even after several months when stored in dry air. Because of reproducible insulator-semiconductor interface properties and high dielectric constant of the MoO_3 insulator the capacitors may be used as varactor capacitance. The leakage current in the nanoampere range is suitable for device operations. The high breakdown field strength (~ 10^8 V/m) and the absence of hysteresis are the interesting factors which may make these MOS structures suitable for microelectronic device applications.

TABLE I
DEPLETION - LAYER PARAMETERS AT 50 KHZ AND AT 300 K

Sl. No.	Device area (nm^2) A	Oxide thickness (nm) d_i	Semiconductor thickness (nm) d_s	N_A (m^{-3}) x 10^{24}	C_{FB} (μF)	V_{FB} (Volt)	L_D (nm)	V_{bi} (Volt)	W (nm)	C_D (μF/ m^2) x 10^{-4}	Q_{SC} (Coul/m^2 x 10^{-2}
1.	9500	18	164.0	2.90	0.023	-0.25	2.0	-2.948	28.4	0.22	1.32
2.	8500	25	192.5	2.20	0.015	-0.50	2.2	-4.048	38.3	0.17	1.35
3.	11000	43	90.0	0.25	0.010	-0.40	6.4	-2.048	80.7	0.08	0.323

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