

CMOS Solid-State Nanopore DNA System-Level Sequencing Techniques Enhancement

Syed Islam, Yiyun Huang, Sebastian Magierowski, Ebrahim Ghafar-Zadeh

Abstract—This paper presents system level CMOS solid-state nanopore techniques enhancement for speedup next generation molecular recording and high throughput channels. This discussion also considers optimum number of base-pair (bp) measurements through channel as an important role to enhance potential read accuracy. Effective power consumption estimation offered suitable range of multi-channel configuration. Nanopore bp extraction model in statistical method could contribute higher read accuracy with longer read-length ($200 < \text{read-length}$). Nanopore ionic current switching with Time Multiplexing (TM) based multichannel readout system contributed hardware savings.

Keywords—DNA, Nanopore, Amplifier, ADC, Multichannel.

I. INTRODUCTION

BIOLOGICAL inspired CMOS-nanopore sensor has emerged to single electronic detection platform since last few years.

This device provides single-molecule detection and analytical capabilities that are achieved by electrophoretically driving molecules in solution through a nano-scale pore. The Technology CMOS plays an important role for bio-sensors apart from play a supporting role in measurement. It has ability to detect minute changes amongst clutter. It also has ability to reduce noise sources by dynamic feedback loop, which brings advantages to increase sensitivity, range, reliability, and resolution [1].

For DNA sequencing instrumentation, University of California (Santa Cruz) and George Church of Harvard (Cambridge, MA, USA) came out an idea of driving strand of DNA or RNA electrophoretically through a nanopore in a suitable diameter, the nucleobases would similarly modulate the ionic current through nanopore [2]. An array of nanopore based commercially viable sequencing system required electrical measurement using integrated microfluidics and electronic instrumentations.

Common techniques (not limited to) for designing nanopore are biological pores formed by transmembrane proteins and synthetic pores fabricated from various materials. However, one of the major challenges (almost impossible!) to develop natural or manmade structures for detecting ionic current of only one nucleotide at a time during translocation of RNA or DNA strands. Practically, it is quite impossible to design approx. $\sim 5\text{nm}$ nanopore channels.

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The characteristic of transimpedance amplifier is suitable to sense low signal current and convert it into a voltage with maximum SNR for further processing. The classic configuration of transimpedance amplifier having a simple resistor R_f in the feedback path of an operational amplifier (opamp).

This paper describes the importance of resolution of the ion current flow determination through pore to base-pair(bp) notation. To achieve better signal-to-noise ratio (SNR) from noise analysis and velocity of the nucleotides, a low noise and high speed transimpedance amplifier construction parameter brought into consideration. It also discussed about power estimation of the multichannel readout system. The rest of the paper (Section II) we employ simple nanopore signal models and viability of amplifying signals with high SNR. We (Section III) estimated power consumption and system noise analysis. We then (Sections IV & V) explore parallel CMOS system to boost measurements throughput.

II. NANOPORE SIGNALS MODELING

In this section, nanopore model and its ionic current behavior detection is discussed. To amplify current signal, suitable amplifier hardware architecture and its acceptable SNR features are also considered.

A. Nanopore Electrical Model

The properties of solid-state nanopore sensor relies on the activities of individual molecules into an electrical signal while molecules passes through the nanopores. Based on this characteristics, this sensor is modeled to represent the electrical behavior by the combination of capacitances and resistances [3]-[4]. The basic solid-state nanopore sensor model with readout system is described in Fig. 1. The advantages of this model help to analyze operating behavior, different kind of noises, and performances while connected with the complete readout circuit system.

The resolution determination of the nanopore sensor is always highlighted as a challenging issue. The location and number of bases, which influence the ion current signature at any given time, are dependent on the dimensions and architecture of the pore. The minimum suitable ionic current levels by DNA fragments in a pore accounting for the 3-bp resolution [5]. The simulation is conducted over determining bp behavior of the mean ionic current (I_{mean}). The Fig. 2 described the (I_{mean}) deviation by four steps representing nucleotides bp resolution.

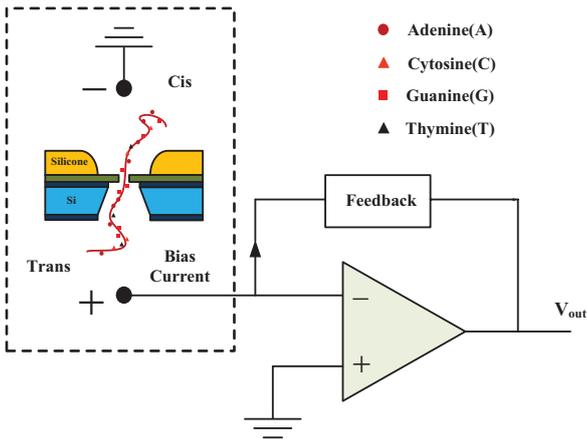


Fig. 1. Basic solid-state nanopore & readout model, consists separated two reservoirs (cis and trans) of conducting liquid solution (typically 0.01-1M KCL). Using voltage difference between two Ag/AgCl electrodes, nucleotides through nanopore is possible to determine using different level of ionic current. low-noise and high-speed amplifier, and ADC are utilized in readout system.

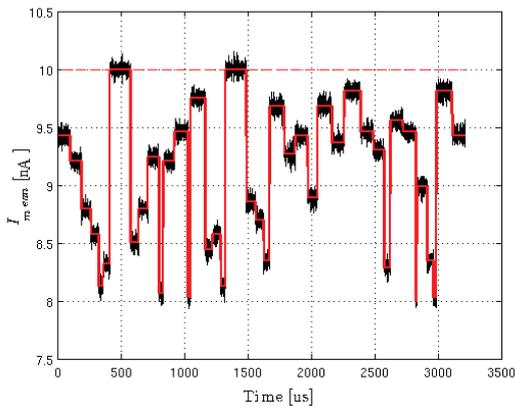


Fig. 2. Ionic current of DNA fragments response in a pore. The current response shows possible DNA triplets ($4^3 = 64$) levels

The signal, I_{meas} , through a nanopore is presented as a step-like deviation from some baseline DC current I_{dc} . The contrived example in Fig. 2 shows some signal deviating from a 10 nA DC current.

As part of this abstraction we need think only in terms of the variations induced in the otherwise constant baseline current. We call these variations I_{signal} and sketch them in Fig. 3 (the scale of the y-axis is arbitrarily set to nA in this example).

As implied in Fig. 3 the signal extends between two extrema (+1 and -1 nA in the example of Fig. 3), which define a peak-to-peak value ΔI , in the example of Fig. 3 $\Delta I = 2$ nA).

Of course the actual information signal, the one that tells us which base (or perhaps which combination of bases) just went through the nanopore depends on any one of L levels that I_{signal} settles on. In the example of Fig. 3 $L = 4^1$ is used, but this could vary as your sensor might only be sensitive enough to discern combinations of bases, e.g. 4^2 , 4^3 , etc.

As a result the actual signal strength, or “size” is the average difference between levels which we can approximate (if we are

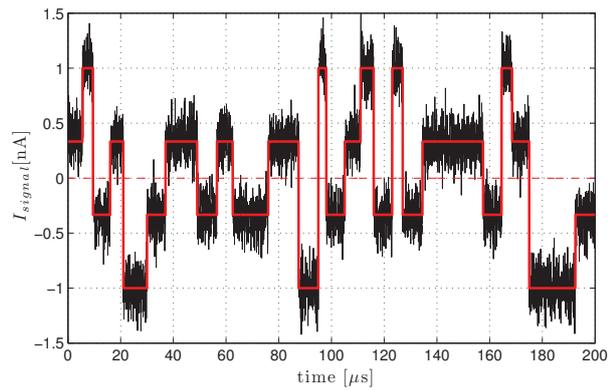


Fig. 3. The variation in the nanopore current as shown is in fact the signal characteristic we are most interested in. These are qualitatively similar to the signals of Fig. 2 which represent the current actually measured.



Fig. 4. The current level values illustrated alongside a mock of a nanopore current signal.

being easy on ourselves) with

$$i_{\delta} = \frac{\Delta I}{L-1} \quad (1)$$

For clarity these variables are illustrated in the sketch shown in Fig. 4

If we wish to adequately recover the measured base information such that we can best decode the bases, A, G, C, T represented by our symbols (i.e. do accurate **base calling**) we must ensure that i_{δ} is sufficiently greater than the noise present in the system. In other words, our signal-to-noise ration, SNR, must be sufficiently large.

B. Input Transimpedance Amplifier

The electronic measurements of ion channels are usually with transimpedance amplifier and this electrical characteristic needs the capability of sensing extremely low signals approximately (1~100) picoamperes for biomolecule nanopore sensor like α -hemolysin [6] and Mycobacterium smegmatis porin A (MspA) [7] and nearly several nano-amperes for the solid-state nanopores [3]. To design high-speed front-end amplifier, the key challenges are to minimize different kind of noises (e.g. capacitive,

flicker, and thermal noises) generated by instruments (nanopore and measuring instruments) and surrounding environments. Commercially available (e.g. Axopatch 200B [[8]]) systems have major drawback of amplifying massive number of channels ($1M < \text{channels}$) at a time. Hence, researchers found importance of designing very low current noise and multi-channel feasible CMOS based input transimpedance amplifier for ion current measurements.

Suitable amplifier from molecular and nanodevices current measurement presented in [9], claimed operating frequency 1MHz [3] with only $4fA/\sqrt{Hz}$ at 100KHz. This amplifier achieved better performance compare to capacitance feedback amplifier [10] and the resistance feedback track-and-hold amplifier [11].

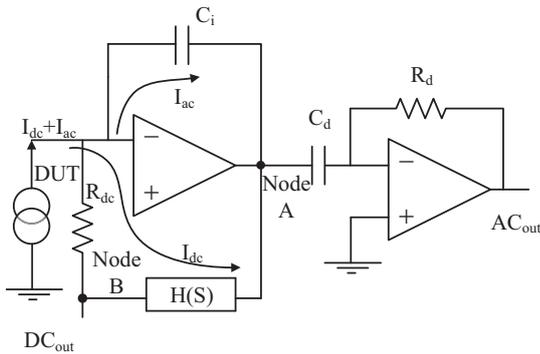


Fig. 5. A novel low-noise Transimpedance Amplifier [9]

The simplified circuit architecture of the transimpedance amplifier [9] is shown in Fig. 5. the circuit consists of two different parts that are the first capacitive feedback amplifier followed with the differentiator amplifier. However, the first stage is different from the normal integrator scheme amplifier because there are two paths, dc path and ac path, comprising the feedback loops. The dc path is used to decouple the stand current from the signal and the rest of the signal current will pass through the ac path, amplified by the integrator-differentiator for all frequencies around high frequency, to the ac output node. Here the gain of the stand current is determined by the values of R_{dc} and the ac signal is determined by:

$$G = C_d/C_i \times R_d \quad (2)$$

The $H(s)$ is the key architecture in this scheme, it has a gain from node A to node B greater than 1 for signal's the frequency below than f_p Hz but the high attenuation for the signal bandwidth. Here the frequency f_p should be as low as possible and it is nearly 16nHz in the paper [12]. Thus when the frequency is below than f_p Hz, the current will go the dc path and the current variation will be reflected at the dc output node but the higher frequency will pass through the ac path and be reflected at the ac out node. Due to the strong attenuation of the $H(s)$, the ac signal won't influence the voltage variation at the dc output node.

III. FRONT-END PROCESSING

In order to achieve a good performance of the nanopore set up and the amplifier, the low power consumption and noise are necessary to be considered at the beginning.

A. Power Consumption

The power consumption of multi-channel nanopore system can be estimated while it is operating specific biasing voltage and bandwidth. It is noted that different nucleotides share different translocation velocity v_t even with the same biasing voltage. The reason also described in [13], highlighted dwell time of nucleotides yields to the poisson distribution and in turn proves the translocation velocity varies with respect to time. To calculate power consumption, ideal amplifier can be modeled as an operational amplifier (op-amp) shown in Fig. 6. The trans-conductance (g_m) of the amplifier can be calculated as –

$$g_m = 2\pi C_{gs} f \quad (3)$$

where C_{gs} is the feedback capacitance and f is the operating frequency

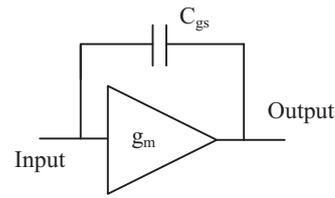


Fig. 6. The Equivalent Simplified Op-amp

The relation between g_m and drain current, I_d ($g_m \propto \sqrt{I_d}$), and each channel Power (P) and I_d ($P \propto I_d$) can be utilized to calculate relation between P and f as

$$P \propto f^2 \quad (4)$$

As a reference [3] of practical power measurement, the similar amplifier consumed 5mW at 1MHz on operating 1.5V biasing source. Assuming the oversample rate is applied as 2 in order to avoid any aliasing, an illustration of the power consumption is shown in the Fig. 7.

Due to the high propotion ratio, the power consumption will increase a lot if the translocation velocity increases slightly and if we consider the influences of the oversample, the performance of the power consumption will become worse.

B. Noise Signals

As with all signal processing chains, the noise from the front-head amplifier will also have great influences on the performance of the amplifier. The preamplifier topology from the Fig. 5 will convert the small input current to the large voltage domain. However, various noise of this impedance amplifier is also amplified at the same time and they are identified as thermal and flicker noise and the capacitance noise will be more important when the sequencing is in the

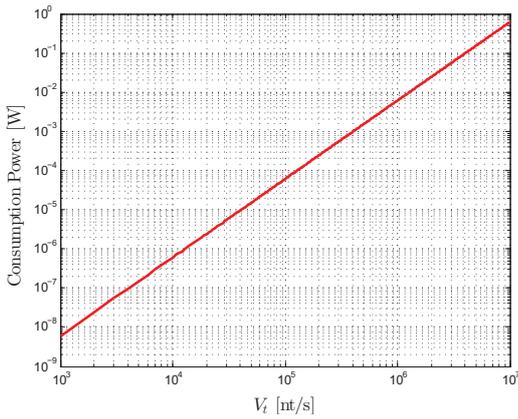


Fig. 7. The Power Consumption in each channel

high speed operation. The expression of input current power spectral density of the noise ([12],[14]) mentioned above which are shown as below.

$$\overline{i_n^2} = \overline{i_f^2} + \overline{i_t^2} + \overline{i_{cap}^2}; \quad (5)$$

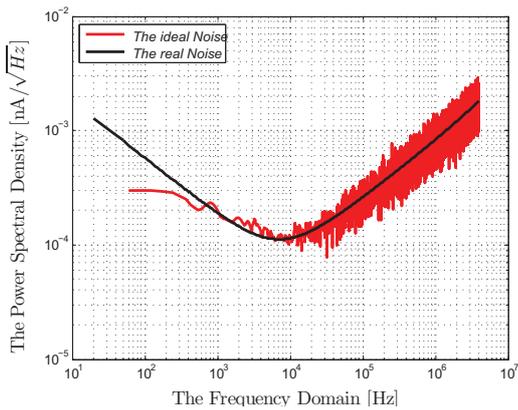


Fig. 8. The PSD of the Input Current Noise

Where $\overline{i_t^2}$ refers to the thermal noise coming from the DUT and the feedback resistance, $\overline{i_f^2}$ refers to the flicker noise from the sensor and $\overline{i_{cap}^2}$ is the overall capacitance noise. However the each part of the noise take on the form

$$\overline{i_f^2} = \frac{A(I_{dc})^2}{f}; \quad (6)$$

Where the I_{dc} refers to the mean of the DC current and f refers to the sampling frequency of the system.

$$\overline{i_t^2} = \left(\frac{e_m}{R_f}\right)^2 + \left(\frac{4KT}{R_f}\right)^2 + \left(\frac{4KT}{R_a + R_p}\right)^2; \quad (7)$$

Where R_p is the resistance of the channel and R_a refers to the resistance between the electrode and the mouth of the nanopores [3]. The e_m refers to the voltage noise source from the front-head op-amp.

$$\overline{i_{cap}^2} = \frac{4\pi f C_{total} e_m^2}{R_f} + (C_{total} e_m 2\pi f)^2; \quad (8)$$

Here, the C_{total} refers to the summation of the input and feedback capacitances. Thus the current noise resulted by each component is shown in the Fig. 9. As we can see from the graph, the dominant noise is the flicker noise when the sequencing is working under 10kHz but the capacitance noise will be the dominant one once the frequency is up to over 10kHz.

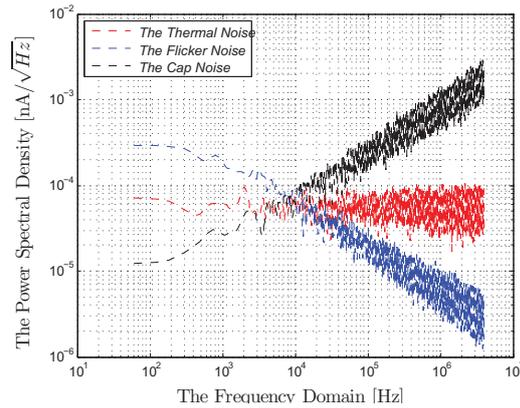


Fig. 9. The PSD of various components from the Input Current Noise

Since the noise part has great connections with the sampling frequency f , the way to show the relationship between the noise and the nucleotides translocation velocity could be more useful for the designers. The basic way to show the performance of the noise is the SNR which refers to the signal-to-noise ratio and we can pick the oversample rate maintaining as 2 to avoid the aliasing as well.

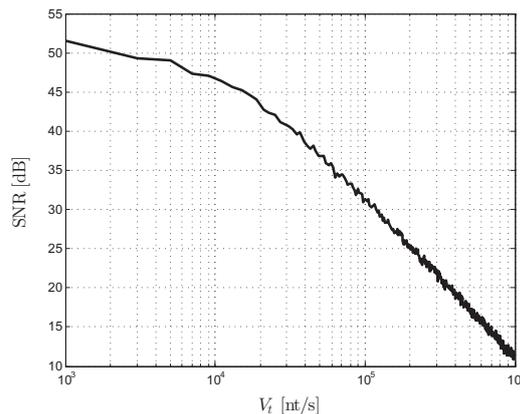


Fig. 10. The changing of the SNR versus the translocation velocity

Obviously, the SNR becomes bad when the velocity increases because the faster of the translocation happening means that we need much higher sampling frequency to capture it and at the same time increase the violet noise.

IV. MULTIPLEX MULTICHANNEL READOUT SYSTEM

The fundamental idea of increasing bandwidth is to run multiple sensors operating in parallel. The most two popular approaches, frequency multiplexing [15] and time multiplexing techniques can employ for CMOS-based sensor readout system. However, time multiplexing system provides low hardware overhead compare to frequency multiplexing. Buffer controlled transistor switching configuration is discussed in [16]. Fig. 11 described overall hardware architecture of the multi-channel system.

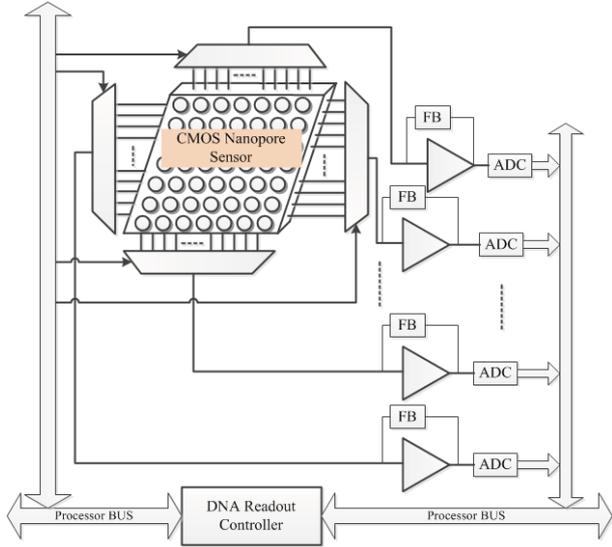


Fig. 11. Nanopore multiple sensor readout system model. DNA readout controller is used for processing bp reading logic and sequencing.

A. Multichannel estimation

The number of channels for parallel processing is proportional to combined nucleotides speed through pore. The nanopore from Oxford Nanopore Tech. (OX), the recommended speed from their MinION Application Program (MAP) is less than 30 nt/s/pore. This is about in line with the speeds discussed in their patent which took about 30-40ms to process a base and perhaps this is the speed at which they currently achieve acceptable base-calling accuracies.

OX claimed that a single cartridge of their GridION system contains a "high-density array of low-noise amplifier circuitry" which "can be scaled to measure from tens to thousands of channels". GridION system might be estimated about approx. 2000 (more calculative estimation ~2048) channels per cartridge. Hence the system speed can be calculated as

$$v_{t,OX} = 30 \times 2048 = 61.4 \times 10^3 [nt/s] \quad (9)$$

B. Switching Impedance Estimation

The multichannel nanopore current measurement hardware system has possibility of placing multiplexed system between nanopore and patch-clamp amplifier. The compromising issues are introducing switching noises for the presence of

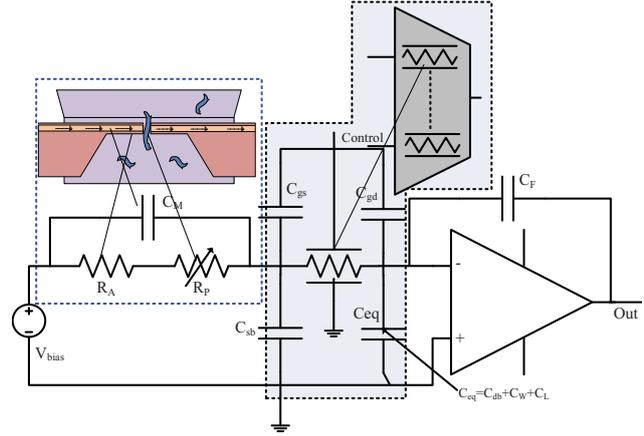


Fig. 12. A multiplexed system (nanopore, multiplexed-switch, and amplifier connection model). C_{gs} , C_{sb} , C_{gd} , and C_{eq} capacitance is introduced during each pore channel is connected to the readout system.

additional capacitance and thermal effects. Fig. 12 shows the nanopore integrated multiplex switching architecture and capacitive noise model for the readout system. In order to nanopore channel sensitive processor control switch design, low impedance while connection is ON and high impedance while NOT connected, estimation is necessary.

The critical issue is the design sophisticated current control and low noise switching mechanism. The nanopore current KVL equation can be formulated along its path while switch is ON–

$$I \times R_A + I \times R_P + I \times r_{ds}(on) = V_{bias} \quad (10)$$

where, I is the nanopore sensor stimulating current, R_A pore fixed impedance, R_P pore sensor variable impedance, and r_{ds} is transistor switching equivalent resistance.

For calculating maximum nanopore sensor current (I_{max}), it can be formulated from KVL–

$$I_{max} \times R_A + I_{max} \times R_{P_{min}} + I_{max} \times r_{ds}(on) = V_{bias} \quad (11)$$

Similarly, for calculating minimum nanopore current, I_{min} –

$$I_{min} \times R_A + I_{min} \times R_{P_{max}} + I_{min} \times r_{ds}(on) = V_{bias} \quad (12)$$

In Ideal case, $V(in) \cong V(out)$ & $V_{DS} \cong 0$ (switch, drain to source voltage) while switch is ON, That is, the transistor is operating in the ohmic region. The drain current is given by –

$$I_{DS} = K(W/L)(V_{GS} - V_T - V_{DS}/2)V_{DS} \quad (13)$$

Hence, the $r_{ds}(on)$ equivalent resistance is calculated by –

$$r_{ds}(on) = \frac{V_{DS}}{I_{DS}} = \frac{1}{K(W/L)(V_{GS} - V_T)} \quad (14)$$

Here, K is the transconductance coefficient, and V_T is the transistor threshold voltage. From equation (14), the $r_{ds}(on)$ resistance can be reduced by increasing (W/L) ratio. However, optimized (W/L) ratio, consideration of the nanopore sensor impedance R_P varies 20% of the R_A [3], and $V_{bias} \cong 400mV$, the nanopore current variation can be estimated as $\Delta I(I_{max} - I_{min}) \approx 0.27nA$.

While switch is OFF ($V_{GS} \cong 0V$), the estimation of subthreshold leakage current ($I_D(off)$) is given by [17]–

$$I_D(off) = (n-1)\mu_n C_{ox} \left(\frac{W}{L}\right) \left(\frac{KT}{q}\right)^2 e^{-\frac{qV_T}{kT}} \quad (15)$$

Typically, $n = \frac{C_{ox} + C_{j0}}{C_{ox}} \approx 1.5$, $C_{ox} = 1.9 \times 10^{-3} pF/\mu m$, at room temperature $V_T = \frac{KT}{q} \cong 26mV$, and $\mu_n \cong 0.01 - 0.06 m^2/V$. From equation (15), $I_D(off)$ can be reduced by decreasing (W/L) ratio. Hence, the transistor switching OFF resistance, $r_{ds(off)}$ can be calculated from [17] –

$$r_{ds(off)} \approx \frac{1}{I_D(off)\lambda} \quad (16)$$

$$\text{where, } \lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{GS} + V_T + \phi_0}} \quad (17)$$

Formulation in equation (14) & (16) shows that $[r_{ds(on)}, r_{ds(off)}] \propto \frac{1}{(W/L)}$. In nanopore multiplexed system, r_{ds} is connected in series with high resistive sensors, the optimum solution is to decrease (W/L) to reduce minimum $I_D(off)$ current. At the same time, it has minimum impact in the circuit with the percentage of increasing $r_{ds(on)}$. This adjustment will also reduce silicon die area as well as overall cost of the CMOS chip. The satisfactory level of 130-nm NMOS switching resistance value is estimated approx $R_{ON} \approx 650\Omega$ and $R_{off} \approx 1G\Omega$ [16].

C. Base-pair(bp) Extraction Model

The resolution of the nanopore is always crucial because of its dimensions and architecture of the pore. Nanopore decoding model is demonstrated 3-bp-resolution electrical measurement to achieve potential accuracy [5]. Hidden Markov model (HMMs) supported bp extraction Graph (BpEG) is constructed (Fig.13) for achievable read-length and accuracy.

Consider nucleotides current signature is observed using 3-bp-resolution method. According to exhaustive HMMs, there are 63 possible transitions from each step. According to de novo base-calling approach, only four possible transitions has equal likelihood. For example, 3-bp nucleotides states CAA has equal likelihood transition to ACA, CCA, GCA, and TCA instead of all 63 possibilities. statistical model allows model to observe chain output with acceptable read-length.

V. SUMMARY

CMOS-based solid state nanopore signal and system characteristics were the major consideration for sequencing techniques enhancement. Time multiplexing switching impedance calculation proven accuracy with R_{ON} and R_{off} value. A parallel readout system was then discussed to boostup nanopore measurement throughput.

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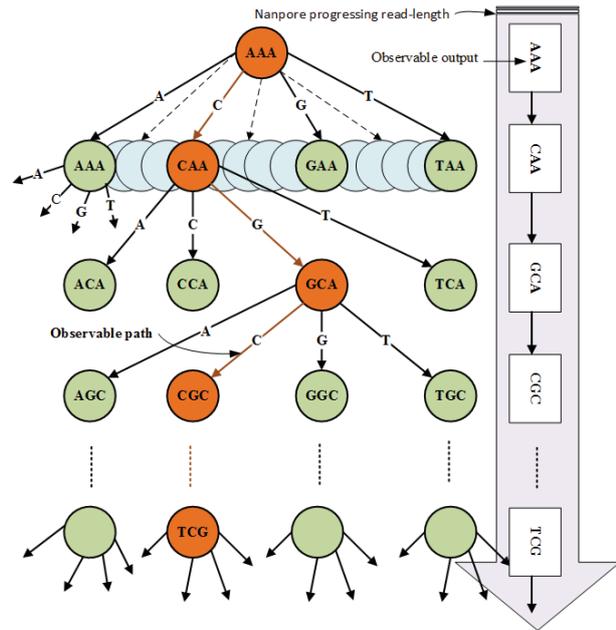


Fig. 13. Nanopore bp extraction Model using 3-bp-resolution concept. Every step advances based on 0.25 transition possibilities. Hence 256 possible transition matrix generated from all equal 64 possible states.

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Yiyun Huang was born in Lishui, China, 1991. He received the undergraduate degree from the Nanjing University of Aeronautics and Astronautics in Electrical Engineering in 2013. From 2014 to present, He is in the master program at the Department of the Electrical Engineering and Computer Science of York University. His primary research interests were using the CMOS technique to design a kind of very low noise and high speed sensor in the DNA sequencing domain. Currently, he works at the development of the CUSUM algorithm to achieve a better detection of each nucleotide and implement it into high speed integrated circuits. He is a coauthor of several papers published in international electronic conferences.



Sebastian Magierowski received the Ph.D. degree in electrical engineering from the University of Toronto in 2004. From 2004 to 2012 he was a faculty member with the University of Calgarys Department of Electrical and Computer Engineering attaining the rank of Associate Professor. In 2013 he joined York Universitys Department of Electrical Engineering and Computer Science as an Associate Professor. His research interests center around integrated circuit design for communication and biomedical systems.