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Closed form Delay Model for on-Chip VLSI RLCG Interconnects for Ramp Input for Different Damping Conditions

Susmita Sahoo, Madhumanti Datta, and Rajib Kar

***Abstract*—**Fast delay estimation methods, as opposed to simulation techniques, are needed for incremental performance driven layout synthesis. On-chip inductive effects are becoming predominant in deep submicron interconnects due to increasing clock speed and circuit complexity. Inductance causes noise in signal waveforms, which can adversely affect the performance of the circuit and signal integrity. Several approaches have been put forward which consider the inductance for on-chip interconnect modelling. But for even much higher frequency, of the order of few GHz, the shunt dielectric lossy component has become comparable to that of other electrical parameters for high speed VLSI design. In order to cope up with this effect, on-chip interconnect has to be modelled as distributed RLCG line. Elmore delay based methods, although efficient, cannot accurately estimate the delay for RLCG interconnect line. In this paper, an accurate analytical delay model has been derived, based on first and second moments of RLCG interconnection lines. The proposed model considers both the effect of inductance and conductance matrices. We have performed the simulation in 0.18μm technology node and an error of as low as less as 5% has been achieved with the proposed model when compared to SPICE. The importance of the conductance matrices in interconnect modelling has also been discussed and it is shown that if G is neglected for interconnect line modelling, then it will result an delay error of as high as 6% when compared to SPICE.

***Keywords*—**Delay Modelling; On-Chip Interconnect; RLCG Interconnect; Ramp Input; Damping; VLSI

I. Introduction

WITH the development of ultra large scale integrated circuit (IC) process, interconnect delay is playing the dominant role as compared to the gate delay. Simple but effective analytical delay models of interconnects are useful for IC designers to avoid the timing issue problem and to optimize the design, such as minimizing delay [1-5]. Hence, it is necessary to build accurate and effective delay estimation models for interconnects.

Susmita Sahoo is with the Department of Electronics & Communication Engg., National Institute of Technology, Durgapur, West Bengal, 713029 (e-mail: susmitas1987@gmail.com).

Madhumanti Datta is with the Department of Electronics & Communication Engg., National Institute of Technology, Durgapur, West Bengal, 713029 (e-mail: madhumanti_datta@rediffmail.com)

Rajib Kar is with the Department of Electronics & Communication Engg., National Institute of Technology, Durgapur, West Bengal, 713029 (e-mail: rajibkarece@gmail.com)

Elmore delay model [1], which is simple in form and easy to be used, has been widely adopted to estimate the interconnect delays in the performance-driven synthesis and layout of very large-scale integrated (VLSI) routing topologies.

It is actually the first order estimation of the interconnect delay with an ideal step input signal, i.e., assuming rise time to be zero. Depending on the frequency used for circuit operation, topology of the interconnect structure, and the rise time of the input signal, the on-chip interconnect may be modelled either as lumped, distributed or as the full wave models. At relatively lower frequency, interconnect may be modelled as distributed RC segments [12-15]. In order to capture the high frequency effect such as, undershoot, overshoot, ringing, the interconnect is modelled as distributed RLC network [16-18] and the accuracy in performance estimation of interconnect eventually got improved. But, unfortunately, these RC or RLC models lack in accuracy as the dielectric loss G can not be ignored in many practical situations especially in the very high frequency domain used in the present VLSI design [19].

With the increase in speed of high performance VLSI circuits, inductance and conductance effect of interconnects are becoming more and more important and can no longer be neglected. Under this circumstance, the Elmore model is inadequate since this model takes only the resistance and capacitance effects into account. It is necessary to use a second order model, which includes the effect of inductance and conductance. There are several approaches proposed to estimate the on-chip interconnect performance characteristic; where the interconnect is modelled as distributed RLCG segment. In [20], the interconnect line is modelled as distributed RLCG elements and the frequency response is calculated and it is shown that RLCG consideration is suitable up to 110 GHz frequency of operation. Hua et. al. [21] have proposed an interconnect RLCG state space models in time domain with computation complexity of O(N), where N is the total system order. An analytical delay model for distributed on-chip RLCG interconnects has been proposed in [6] taking step function as input. Another delay model proposed in [7] calculates delay of distributed RLCG interconnects by taking into consideration the coupling effect and by using difference model approach is put forward. In [8] also, the delay is calculated for on-chip global RLCG interconnect using step input. However, for all these models, a precondition exists that the input signal is assumed to be an ideal step signal. But that

is not the case in practice. There must be a definite rise time slope, i.e., the input must be a ramp signal with a predefined rise time. In a study by Hasegawa et.al. [4], the concept of delay models for interconnects under ramp input is investigated. However, the paper offers only a brief discussion on the over-damped cases irrespective of the under damped and critical damping cases. In [9], unified delay analysis for on-chip RLCG interconnects for ramp input using fourth order transfer function is presented. But this model suffers from accuracy point of view and no information regarding damping is provided. In this paper, analytical delay models for RLCG interconnects under ramp input are presented for different damping situations, i.e., over damped, under damped and critical damped cases. This paper is summarized as follows: Section 2 presents the delay model for on-chip interconnects for step input excitation. Section 3 describes the proposed delay model for ramp input. The different delay metrics have been derived for different pole conditions. Section 4 shows the simulation result. Finally Section 5 concludes the paper.

II. Delay Model for Interconnects under Step Input

In this section, a second order analytical delay model for interconnects under step input has been proposed. In the transform domain, output response can be obtained through $V_{out}(s) = V_{in}(s)H(s)$; where $H(s)$ is the transfer function of the system. By using inverse Laplace transform, the output response in time domain can also be obtained. With the time domain output response $V_{out}(t)$, one can easily obtain the delay under a certain output threshold.

Transfer function of the interconnect line of Figure 1 can be derived as,

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{\left[A + \frac{Z_s}{Z_0}B\right] + \frac{1}{Z_t}\left[Z_0 B + Z_s A\right]} \quad (1)$$

Where, $A = \cosh(\gamma d), B = \sinh(\gamma d)$.

And $\gamma = \sqrt{((r+sl)(g+sc))}$ is the transfer constant, $Z_0 = \sqrt{\frac{(R+sL)}{(G+sC)}}$ is the characteristics impedance, Z_t, Z_s are the load impedance and the source impedance, respectively and are given as, $Z_t = \frac{1}{sC_t}$ and $Z_s = R_s + sL_s$.

$r = R/d, l = L/d, c = C/d, g = G/d$.

Where, r, l, c, g represents resistance, inductance, capacitance and conductance per unit length of the interconnect, respectively and d is the length of the interconnect. By expanding *cosh* and *sinh* as infinite power series and considering the terms up to the coefficient of s^2 in the denominator, the truncated transfer function can be obtained as follows:

$$H(s) = \frac{1}{b_0 + b_1 s + b_2 s^2} \quad (2)$$

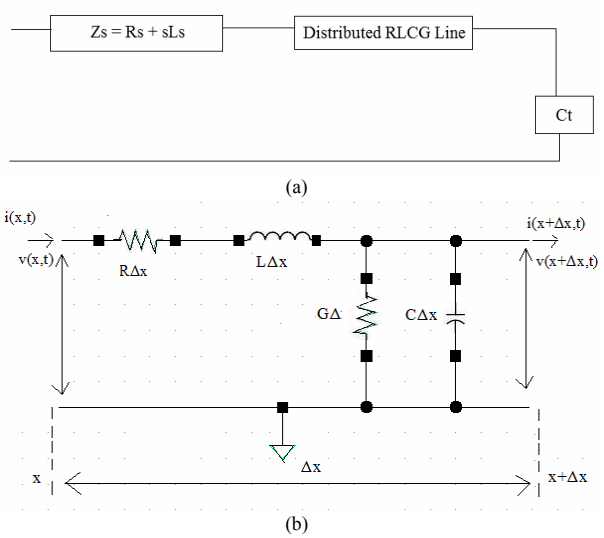

Fig. 1 (a) Two-Port Model of a Distributed RLCG Line with Resistive and Inductive Source Impedance and Capacitive Load Impedance; (b) Section of a Distributed RLCG Interconnect Line

Where the coefficients b_0, b_1, b_2, are, respectively, calculated as,

$$b_0 = 1 + \frac{1}{2}RG + R_s G + \frac{1}{6}R_s RG^2 \quad (3)$$

$$b_1 = R_s C + R_s C_t + \frac{RC}{2} + RC_t + \frac{LG}{2} + L_s G + \frac{1}{6}\left(RR_s GC + R_s LG^2 + RL_s G^2 + R^2 G\right) \quad (4)$$

$$b_2 = \frac{1}{2}LC + CL_s + LC_t + L_s C_t + \frac{RR_s CC_t}{2} + \frac{1}{3}RLGC_t + \frac{1}{2}R_s GLC_t + \frac{1}{2}GL_s RC_t + \frac{1}{6}\left(R_s RC^2 + R_2 CC_t + LL_s G^2 + R_s GLC + L_s CRG + R^2 CC_t\right) \quad (5)$$

When the input is an ideal step signal with the amplitude V_0,

$$V_{out}(s) = V_{in}(s)H(s) = \frac{V_0}{s}\frac{1}{b_0 + b_1 s + b_2 s^2} \quad (6)$$

V_{out} (t) can be obtained by inverse Laplace transform. Assuming $V_{out}(t) = 0.9V_0$, we can get the 90% delay $t_{0.9}$.

III. Interconnect Delay Model for Ramp Input

In practice, the input signal to be transmitted through the interconnect lines can never be ideal. Instead, the input signal must have a finite rise time. Thus, using the delay model, which is obtained with the ideal step signal as the stimulus, will inevitably lead to a calculation error. In this section, a detailed analysis of the delay modelling with ramp input has been discussed for both real and complex pole conditions.

The finite rising ramp input shown in Figure 2 can be expressed in the time domain as [10],

$$V_{f\_in}(t) = V_{f\_in}(t) - V_{if\_in}(t - t_r) \quad (7)$$

$$= \frac{V_0}{t_r}\left[tU(t) - (t-t_r)U(t-t_r)\right] \quad ,t \geq 0 \tag{8}$$

Where $U(t)$ denotes the step function. The finite ramp input in the transform domain is,

$$V_{f\_in}(s) = \frac{V_0}{t_r}\frac{1}{s^2}\left[1 - e^{-st_r}\right] \tag{9}$$

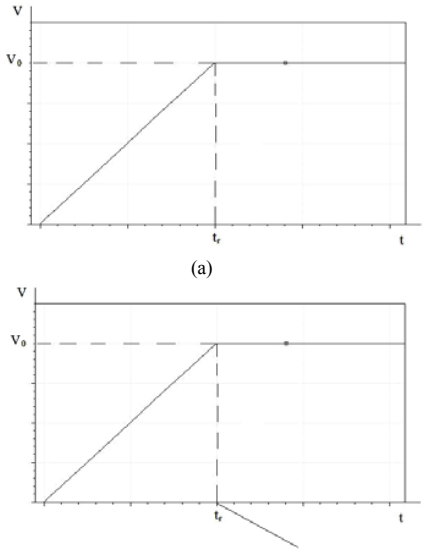

Fig. 2 Ramp Input function (a) Finite Ramp with Rise Time t_r; (b) Finite Ramp Decomposed into Two Shifted Infinite Ramps

In the transform domain, the output response is,

$$\left.\begin{aligned} V_{f\_out}(s) &= \frac{V_0}{t_r}\frac{1}{s^2}\left[1 - e^{-st_r}\right]H(s) \\ &= V_{if\_out}(s)\left[1 - e^{-st_r}\right] \end{aligned}\right\} \tag{10}$$

Applying Elmore's delay definition for step input yields an analytical delay metric t_{AD} for ramp input [10], i.e.

$$t_{AD} = \frac{t_r}{2} + b_1 - a_1 = \frac{t_r}{2} + t_{ED} \tag{11}$$

Where, a_1, b_1 are the co-efficient of s^2 in the numerator and denominator of the transfer function, respectively, and t_{ED} is the Elmore delay for the step input, which is the first moment of the transfer function. Note that t_{ED} should correspond to the different output threshold; Elmore delay corresponds to $t_{0.632}$, i.e., delay with the output threshold of $0.632V_0$ [11] while $t_{0.9}=2.3t_{ED}$, $t_{0.5}=0.693t_{ED}$.

In the following sub-section, the two-pole methodology for interconnect response has been discussed.

A. Real Poles

In the transform domain, response of the infinite ramp is,

$$V_{if-out}(s) = \frac{V_0}{t_r}\frac{1}{s^2}\frac{1}{b_0 + b_1 s + b_2 s^2} \tag{12}$$

$$= \frac{A_0}{s} + \frac{A_1}{s^2} + \frac{A_2}{s-\alpha} + \frac{A_3}{s-\beta} \tag{13}$$

Where,

$$\alpha, \beta = \frac{-b_1 \pm \sqrt{\left(b_1^{\,2} - 4b_0 b_2\right)}}{2b_2} \tag{14}$$

$$A_0 = \frac{-V_0}{t_r}\frac{b_1}{b_0}, A_1 = \frac{V_0}{t_r b_0}, A_2 = \frac{V_0}{t_r}\frac{1}{\alpha^2(\alpha-\beta)}, A_3 = \frac{V_0}{t_r}\frac{1}{\beta^2(\beta-\alpha)} \tag{15}$$

Where α , β are the poles of the transfer function. The corresponding output response in time domain is,

$$V_{if\_out}(t) = \frac{V_0}{t_r}\left(\frac{-b_1}{b_0} + \frac{1}{b_0}t + \frac{1}{\alpha^2(\alpha-\beta)}e^{\alpha t} + \frac{1}{\beta^2(\beta-\alpha)}e^{\beta t}\right)u(t) \tag{16}$$

Considering α , β < 0 and $|\beta| > |\alpha|$ then $\frac{1}{\beta^2(\beta-\alpha)}e^{\beta t}$ decreases more rapidly compared to $\frac{1}{\alpha^2(\alpha-\beta)}e^{\alpha t}$. Hence the two pole response can be approximated as,

$$V_{if\_out}(t) = \frac{V_0}{t_r}\left(\frac{-b_1}{b_0} + \frac{1}{b_0}t + \frac{1}{\alpha^2(\alpha-\beta)}e^{\alpha t}\right)u(t) \tag{17}$$

Then we can get the response of finite ramp as,

$$V_{f\_out}(t) = V_{if\_out}(t) - V_{if\_out}(t-t_r)$$

$$= \frac{V_0}{t_r}\left[\frac{1}{b_0}t_r + \frac{1}{\alpha^2(\alpha-\beta)}\left(e^{\alpha t} - e^{\alpha(t-t_r)}\right) + \frac{1}{\beta^2(\beta-\alpha)}\left(e^{\beta t} - e^{\beta(t-t_r)}\right)\right]u(t) \tag{18}$$

$$\cong \frac{V_0}{t_r}\left[\frac{1}{b_0}t_r + \frac{1}{\alpha^2(\alpha-\beta)}\left(e^{\alpha t} - e^{\alpha(t-t_r)}\right)\right]u(t) \tag{19}$$

Assuming that the delay corresponds to τ when the output reaches v_{th} ,i.e., $V_{f\_out}(\tau) = v_{th}(V_0 = 1)$, then,

$$\tau = \frac{1}{|\alpha|}\ln\left[\frac{(e^{|\alpha|t_r} - 1)}{t_r\alpha^2(\alpha-\beta)\left(\frac{1}{b_0} - v_{th}\right)}\right] \tag{20}$$

This situation can be compared to over damped condition because $b_1^{\,2} > 4b_0b_2$, and the output response shows increasing oscillating pattern

B. Complex Poles

In case of complex poles, we assume that poles of the transfer function are $\alpha, \beta = -p \pm jq$. Response of infinite ramp in the transform domain is thus,

$$V_{if\_out}(s) = \frac{V_0}{t_r}\frac{1}{s^2}\left[\frac{1}{(s+p)^2 + q^2}\right] \tag{21}$$

$$= \frac{A_4}{s} + \frac{A_5}{s^2} + \left[\frac{A_6 s + A_7}{(s+p)^2 + q^2}\right] \tag{22}$$

Where,

$$p = \frac{b_1}{2b_2}, q = \frac{\sqrt{\left(4b_0b_2 - b_1^{\,2}\right)}}{2b_2} \tag{23}$$

$$\left.\begin{aligned} A_4 = \frac{-V_0}{t_r}\frac{b_1}{b_0}, A_5 = \frac{V_0}{t_r}\frac{1}{b_0}, A_6 = \frac{2p}{p^2+q^2}, A_7 = \frac{p^2-q^2}{p^2+q^2} \end{aligned}\right\} \tag{24}$$

$$V_{if\_out}(s) = \frac{V_0}{t_r}\frac{-b_1}{b_0 s} + \frac{1}{b_0 s^2} + \frac{\frac{2p}{p^2+q^2}s + \frac{p^2-q^2}{p^2+q^2}}{\left[(s+p)^2 + q^2\right]} \tag{25}$$

Taking inverse Laplace transform, the time domain

response can be computed as,

$$V_{if\_out}(t)=\frac{V_0}{t_r}\left[\frac{-b_1}{b_0}+\frac{1}{b_0}t+\frac{1}{q}e^{-pt}\sin(qt+\theta)\right]u(t) \quad (26)$$

Where, $\theta=\tan^{-1}\left(\frac{2pq}{p^2-q^2}\right)$

Then we can get the finite response as follows,

$$V_{f\_out}(t)=V_{if\_out}(t)-V_{if\_out}(t-t_r) \quad (27)$$
$$=\frac{V_0}{t_r}\left[\frac{1}{b_0}t_r+\frac{1}{q}e^{-pt}\sin(qt+\theta)-\frac{1}{q}e^{-p(t-t_r)}\sin(q(t-t_r)+\theta)\right]u(t)$$

Assume that the delay corresponds to τ when the output reaches $v_{th}(V_0=1)$, i.e.,

$$V_{f\_out}(\tau)=v_{th}=\frac{1}{t_r}\left[\frac{1}{b_0}t_r+\frac{1}{q}e^{-p\tau}\sin(q\tau+\theta)-\frac{1}{q}e^{-p(\tau-t_r)}\sin(q(\tau-t_r)+\theta)\right]u(t) \quad (28)$$

Equation (28) is a trans-dental equation that can be computed by recursively solving for time. One way to solve the recursion is to approximate the time variable in the *sin* term by equivalent Elmore delay under ramp input, i.e., substitute $t_{AD}'=v_{th}t_r$ for time *t*.

Therefore,

$$\tau=-\frac{1}{p}\ln\left[\frac{\left(\frac{1}{b_0}-v_{th}\right)t_r}{d_2-d_1}\right] \quad (29)$$

Where, $d_1=\frac{1}{q}\sin\left(qt_{AD}'+\theta\right), d_2=\frac{1}{q}e^{pt_r}\sin\left[q\left(t_{AD}'-t_r\right)+\theta\right]$ (30)

If $d_1>d_2$, then substituting $t_{AD}'=v_{th}t_r$ for the time variable in the exponential term and expand the *sin* function as a Taylor series and considering only the first term, we get,

$$\tau=\frac{\left(\left(\frac{1}{b0}-v_{th}\right)+e^{-p\left(t_{AD}'-t_r\right)}\right)t_r}{e^{-pt_{AD}'}\left(e^{pt_r}-1\right)}-\frac{\theta}{q} \quad (31)$$

This situation can be compared to under damped condition because $b_1^{\,2}<4b_0b_2$, and the output response shows decreasing pattern with time.

C. Double Poles

Assume that the poles of the transfer function are α and it is repeated. Then the response of the circuit to infinite ramp input will be,

$$V_{if\_out}(s)=\frac{V_0}{t_r}\frac{1}{s^2}\frac{1}{(s-\alpha)^2} \quad (32)$$

$$=\frac{A_8}{s}+\frac{A_9}{s^2}+\frac{A_{10}}{(s-\alpha)}+\frac{A_{11}}{(s-\alpha)^2} \quad (33)$$

Where,

$$\alpha=\frac{-b_1}{2b_2}, A_8=\frac{2V_0}{t_r}\frac{1}{\alpha^3}, A_9=\frac{V_0}{t_r}\frac{1}{\alpha^2}, A_{10}=\frac{-2V_0}{t_r}\frac{1}{\alpha^3} \text{ and } A_{11}=\frac{V_0}{t_r}\frac{1}{\alpha^2} \quad (34)$$

The time domain response will be of the form given in (35).

$$V_{if\_out}(t)=\frac{V_0}{t_r}\frac{1}{\alpha^2}\left[\frac{2}{\alpha}+t-\frac{2}{\alpha}e^{\alpha t}+te^{\alpha t}\right] \quad (35)$$

The response of finite ramp in transform domain is,

$$V_{f\_out}(t)=V_{if\_out}(t)-V_{if\_out}(t-t_r) \quad (36)$$

$$=\frac{V_0}{t_r}\frac{1}{\alpha^2}\left[t_r+\left(e^{-\alpha t_r}-1\right)\left(\frac{2}{\alpha}e^{\alpha t}-te^{\alpha t}\right)+t_re^{\alpha(t-tr)}\right]u(t) \quad (37)$$

Assume that the delay corresponds to τ when the output reaches v_{th}.

So,

$$V_{f\_out}(\tau)=v_{th}= \quad (38)$$
$$\frac{1}{t_r}\frac{1}{\alpha^2}\left[t_r-\tau e^{\alpha\tau}\left(e^{-\alpha t_r}-1\right)+e^{\alpha\tau}\left(t_re^{-\alpha t_r}+\frac{2}{\alpha}\left(e^{-\alpha t_r}-1\right)\right)\right]u(t)(V_0=1)$$

Here $V_0=1$, is considered as unit step signal has been applied for simplicity.

It is again a trans-dental equation. For simplification, we substitute $t_{AD}'e^{\alpha\tau}$ for $\tau e^{\alpha\tau}$ and τ can be calculated as,

$$\tau=\frac{1}{\alpha}\ln\left[\frac{t_r\left(\alpha^2v_{th}-1\right)}{t_{AD}'+\frac{2}{\alpha}\left(e^{-\alpha t_r}-1\right)+e^{-\alpha t_r}\left(t_r-t_{AD}'\right)}\right] \quad (39)$$

This situation can be compared to critically damped condition because $b_1^{\,2}=4b_0b_2$, and the output response remains constant.

IV. Simulation Results

A. Real Poles

Assume that the length of the interconnect is d=2000 μm; rising time of the input signal is t_r=100 ps; interconnect parameters are, r =0.015 Ω/μm; l=0.246 pH/μm; g =16.65 μS/μm; and c=0.176 pF/μm. The parameter values are taken so to satisfy the condition $b_1^{\,2}>4b_0b_2$ which is represented as over damped condition because $b_1^{\,2}>4b_0b_2$. For 90% delay $t_{0.9}$, the delay estimations using the proposed analytical model [Eq. (20)] is done and the average error is within 5% compared to SPICE simulated delay. In Table 1, 90% delay and Elmore equivalent delay calculation for real poles are estimated and are compared with SPICE result for different values of R_s, L_s, C_t.

B. Complex Poles

We consider that the length of the interconnect is d=2000 μm; rising time of the input signal is t_r =500 ps; interconnect parameters are r =0.015 Ω/μm; l=0.246 pH/μm; g =16.65 μS/μm; and c=0.176 pF/μm. Here the parameter values are taken so to satisfy the condition $b_1^{\,2}<4b_0b_2$ which is represented as under damped condition because $b_1^{\,2}<4b_0b_2$. For 90% delay $t_{0.9}$, the delay estimations using the proposed analytical model [Eq. (31)] is done and the average error is within 5% compared to SPICE simulated delay. In Table 2, 90% delay and Elmore equivalent delay calculation for complex poles are estimated and are compared with SPICE result for different values of R_s, L_s, C_t.

TABLE I
COMPARISON BETWEEN ELMORE AND THE PROPOSED DELAY WITH SPICE RESULT FOR REAL POLES

Source		Load	SPICE delay (90%)(ps)	Delay Model			
$R_s(\Omega)$	L_s(pH)	C_t(pF)		Equivalent Elmore model (90%) (ps)	Error (%)	Proposed model (90%) (ps)	Error (%)
50	2.46	0.176	176.79	162.13	8.29	168.18	4.87
100	2.46	0.176	180.68	167.94	7.05	173.99	3.70
1000	2.46	0.176	387.51	358.76	7.42	362.36	6.49
25	2.46	1.760	183.59	168.87	8.02	175.49	4.41
100	2.46	1.760	187.43	172.42	8.01	177.63	5.23
1000	2.46	1.760	751.54	694.65	7.57	715.54	4.79

TABLE II
COMPARISON BETWEEN ELMORE AND THE PROPOSED DELAY WITH SPICE RESULT FOR COMPLEX POLES

Source		Load	SPICE delay (90%) (ps)	Delay Model			
$R_s(\Omega)$	L_s(pH)	C_t(pF)		Equivalent Elmore model (90%) (ps)	Error (%)	Proposed model (90%) (ps)	Error (%)
10	0.0246	0.0176	770.7	547.74	28.93	730.78	5.18
10	0.0246	0.176	775.7	449.83	42.01	742.27	4.31
20	0.0246	0.176	778.4	476.46	38.79	733.81	5.73
10	2.46	0.0176	771.1	462.27	40.05	730.46	5.27
20	2.46	0.0176	773.3	560.10	27.57	738.73	4.47
10	2.46	0.176	776.0	481.04	38.01	743.33	4.21
20	2.46	0.176	801.1	476.57	40.51	766.73	4.29
10	24.6	0.0176	770.4	455.54	40.87	742.05	3.68
20	24.6	0.0176	773.1	460.07	40.49	736.61	4.72
10	24.6	0.176	775.9	485.63	37.41	735.47	5.21
20	24.6	0.176	779.0	476.36	38.85	744.65	4.41

TABLE III
COMPARISON BETWEEN SPICE AND THE PROPOSED DELAY FOR REAL POLES WHEN $G = 0$

Source		Load	SPICE delay (90%) (ps)	Proposed model (90%) (ps)	Error (%)
$R_s(\Omega)$	L_s(pH)	C_t(pF)			
50	2.46	0.176	27.24	26.28	3.51
100	2.46	0.176	31.11	29.57	4.95
1000	2.46	0.176	57.21	54.29	5.10
25	2.46	1.760	32.46	30.92	4.75
100	2.46	1.760	34.92	33.10	5.21
1000	2.46	1.760	94.23	90.54	3.91

TABLE IV
COMPARISON BETWEEN SPICE AND THE PROPOSED DELAY FOR COMPLEX POLES WHEN $G = 0$

Source		Load	SPICE delay (90%) (ps)	Proposed model (90%) (ps)	Error (%)
$R_s(\Omega)$	L_s(pH)	C_t(pF)			
10	0.0246	0.0176	111.41	106.77	4.16
10	0.0246	0.176	127.57	120.78	5.32
20	0.0246	0.176	131.49	125.29	4.71
10	2.46	0.0176	113.20	108.37	4.27
20	2.46	0.0176	116.01	109.73	5.41
10	2.46	0.176	129.75	125.58	3.21
20	2.46	0.176	156.81	149.64	4.57
10	24.6	0.0176	112.11	107.31	4.28
20	24.6	0.0176	115.32	109.92	4.68
10	24.6	0.176	128.12	123.06	3.95
20	24.6	0.176	153.91	146.66	4.71

C. For G=0

In above discussion delay has been estimated for $G \neq 0$. In this session 90% delay for real and complex poles are calculated for $G = 0$ and are compared with SPICE simulation delay. The average error is as high as 6% when compared to SPICE delay. In Table 3 and 4, delay estimation for $G = 0$ is given for real and complex poles, respectively. From Table 3 and Table 4 it is evident that for accurate modelling of on-chip interconnects, the conductance metrics have to be considered.

The variations of SPICE delay and proposed delay with different values of source resistance R_s and Load capacitance C_t for real poles is presented in Fig-3. Here SPICE delay and Proposed delay for real poles are compared for C_t=0.176 pF and 1.76 pF. It is evident from the graph that with increasing R_s and C_t, delay also shows increasing pattern and proposed model delay closely follows SPICE delay.

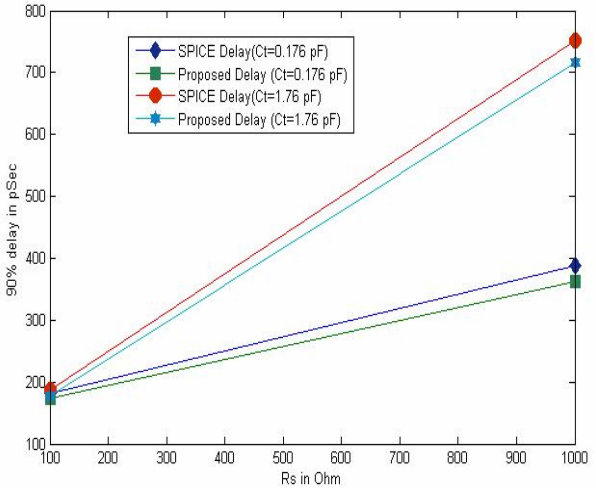

Fig. 3 R_s vs. SPICE and Proposed delay for different values of C_t for Real Poles

The variations of SPICE delay and proposed delay with different values of source resistance R_s and Load capacitance C_t for complex poles are presented in Fig-4. Here SPICE delay and Proposed delay for complex poles are compared for C_t=0.0176 pF and 0.176 pF. It is evident from the graph that with increasing R_s and C_t, delay also shows increasing pattern and proposed model delay closely follows SPICE delay.

The variations of SPICE delay and proposed delay with different values of source resistance R_s and source inductance L_s for complex poles is presented in Fig-5. Here SPICE delay and Proposed delay for complex poles are compared for L_s=0.0246 pH and 24.6 pH. It is evident from the graph that with increasing R_s and L_s, delay also shows increasing pattern and proposed model delay closely follows SPICE delay.

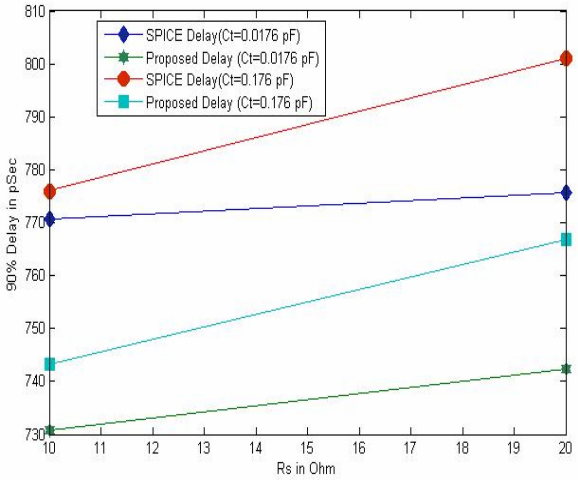

Fig. 4 R_s vs. SPICE and Proposed delay for different values of C_t for Complex Poles

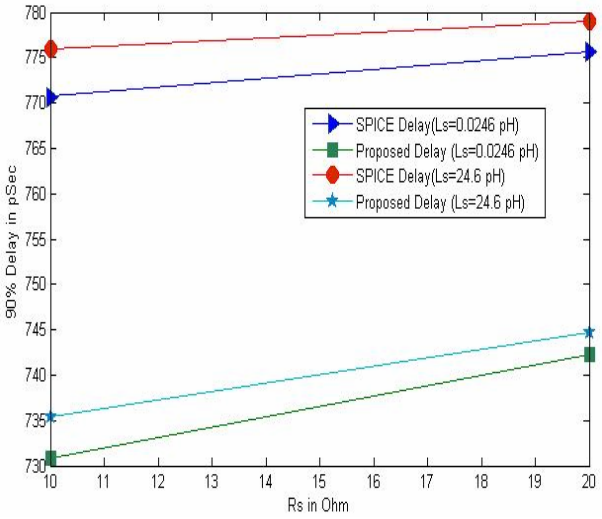

Fig. 5 R_s vs. SPICE and Proposed delay for different values of L_s for Complex Poles

V. Conclusion

In this paper analytical delay models for RLCG interconnects under ramp input are presented which considers the effect of inductance as well as conductance matrices. The resulting delay estimations are significantly more accurate because ramp signal is given as input rather than step signal. Under different situations, i.e. over damped, under damped and critical damped cases, the delay estimation using the proposed delay model are within 5% of error as compared to SPICE simulated delay. The derived delay expression along with the analysis can serve as a convenient tool for delay estimation without much computation during design.

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