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C-V Characterization and Analysis of Temperature and Channel Thickness Effects on Threshold Voltage of Ultra-thin SOI MOSFET by Self-Consistent Model

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Abstract—The threshold voltage and capacitance voltage characteristics of ultra-thin Silicon-on-Insulator MOSFET are greatly influenced by the thickness and doping concentration of the silicon film. In this work, the capacitance voltage characteristics and threshold voltage of the device have been analyzed with quantum mechanical effects using the Self-Consistent model. Reduction of channel thickness and adding doping impurities cause an increase in the threshold voltage. Moreover, the temperature effects cause a significant amount of threshold voltage shift. The temperature dependence of threshold voltage has also been observed with Self-Consistent approach which are well supported from experimental performance of practical devices.

Keywords—C-V characteristics, Self-Consistent Analysis, Silicon-on-Insulator, Ultra-thin film.

I. Introduction

IN nanotechnology and microelectronics where low power consumption and high speed are desired, devices with nano and submicron dimensions are essential. Silicon-on-insulator (SOI) technology is an attractive choice for these applications. In recent years, SOI MOS devices have received great attention due to their advantages over conventional bulk MOSFETs [1]–[4] such as: lower parasitic capacitance, improved subthreshold characterisics and reduced short-channel effects. So to gain insight into the physics of the device and evaluate their performance, an accurate model of the device parameters is essential. The threshold voltage (V_{th}) and Capacitance-Voltage (C-V) characteristics are important features for characterization of the performance of SOI MOSFETs. However, these characteristics are dependent on a wide range of parameters such as: thickness of the channel, front and buried oxide thickness, channel and substrate doping, temperature etc. As device dimensions are scaling down, quantum mechanical effects have become significant specially for SOI with ultra-thin channel [1], [4]. A SOI MOSFET having nearly or below 40nm gate length and 20nm of top silicon layer thickness can be referred to as ultra-thin film device [5]. The classical analysis of (V_{th}) of SOI can not be applied in such a thin region of silicon film thickness (t_{si}) for $t_{si} < 10$ nm [6]. So quantum mechanical study is of great importance for analyzing behavior of nano scale SOI MOSFETs.

Besides, in ultrathin channel devices, the threshold voltage is influenced by operating temperature of the environment. The temperature dependence of V_{th} of accumulation-mode SOI devices has been reported in literature [7], [8] where a semi-classical and quantum mechanical analysis have been performed in [2].

The main contribution of this work is to analyze V_{th} of SOI MOSFETs in an efficient way. Towards this goal, the analysis utilizes the Self-Consistent solver as a newer variant to study the effect of operating temperature on the threshold voltage. Along the way, the effect of doping and channel thickness on V_{th} and C-V characteristics have been studied, which also have independent significance. Self-consistent analysis has been widely used in literature for the analysis of nanoscale bulk MOSFETs [9]–[11]. However, its application for SOI MOSFETs can also provide efficient results as observed from this work. The simulated results with Self-Consistent solver have been compared to experimental device performances and with the results of [2]. The model of [2] produced large deviation with experimental results when t_{si} was increased from 6 nm to 10 nm. But the proposed approach predicted a good agreement with the experimental results compared to the simulated results of [2] irrespective of film thickness. Moreover, C-V characterization is also well established mean for characterizing the strong inversion condition i.e. the V_{th} of SOI devices [12]–[14]. Hence, C-V characteristics have been analyzed with Self-Consistent model to validate the effectiveness of the approach.

II. Analysis Technique: SOI Characterization

A. SOI Structure and Analysis Assumptions

In this paper, the SOI MOSFET on $<100>$ Si surface shown in Fig. 1(a) has been considered. Three interface regions can be identified in the structure such as: gate oxide-silicon film interface, Silicon-film-buried oxide interface (BOX) and the interface of buried oxide and silicon substrate. The buried oxide is thicker compared to other layers. The channel silicon film is ultra-thin with thickness $t_{si} \leq 10$ nm For both the film and substrate, p-type doping is considered. For the thin dimension, the silicon film approaches complete depletion and hence. it works as Fully depleted device [14].

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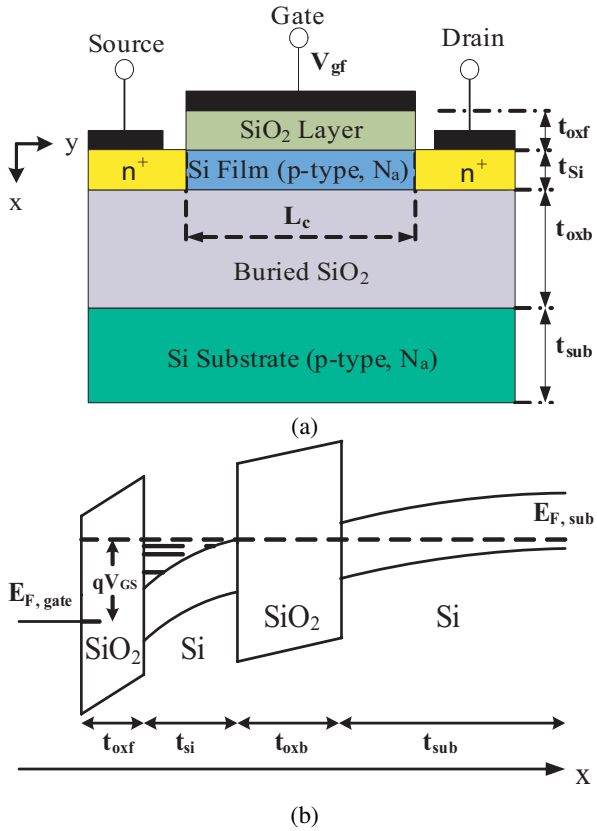


Fig. 1: (a) Schematic structure of ultra-thin SOI MOSFET (b) Energy band diagram at inversion

B. Self-Consistent Analysis: Schrödinger-Poisson Solver

The threshold voltage has been obtained solving the 1-D Poisson and Schrödinger's equation. For the MOSFET, the vertical electric field in channel in the inversion is determined from Poisson's equation as,

$$\frac{d^2V(x)}{dx^2} = -\frac{dE(x)}{dx} = -\frac{\rho_{inv} + \rho_{dep}}{\epsilon_o \epsilon_m} \tag{1}$$

where ρ_{inv} and ρ_{dep} are the inversion and depletion charge density respectively, $V(x)$ is defined as the electric potential, $E(x)$ is the electric field, ϵ_0 is free space permittivity and ϵ_m is the material dielectric constant where $\epsilon_m = \epsilon_{ox}$ for the front and buried oxide and $\epsilon_m = \epsilon_{si}$ for Si channel and substrate.

In most of the cases of SOI devices, the buried oxide is much thicker, hence there is negligible penetration of carriers in the back channel. The eigenstates are found throughout the rectangular well between the two oxide regions [4]. Hence the distribution of inversion charge occurs mostly between this region (Fig. 1(b)). The Schrödinger-Poisson self consistent solver has been implemented to find out the eigen states and inversion carrier concentration.

The Self-Consistent analysis starts with a given gate voltage and ρ_{inv} is initially assumed 0 for solving (1). To obtain ρ_{dep}, a depletion width is assumed in the first iteration and ρ_{dep} is estimated using doping concentration N_a as follows:

$$\rho_{dep}(x) = \begin{cases} -q\,N_a, & \text{when } 0 < x < x_d \\ 0, & \text{when } x > x_d \end{cases} \tag{2}$$

where x_d is depletion layer thickness. Using this depletion and inversion charge density ρ_{dep} and ρ_{inv} respectively, a potential profile is obtained from Poisson solver using equation (1). This potential profile is used to generate an energy band profile for the Schrödinger's solver. Then the inversion carrier concentration is calculated using the eigen energy values obtained as a solution of the one dimensional Schrödinger's solution. The inversion carrier concentration is estimated according to the following expression [15]:

$$n_{inv} = \sum_{ij} n_{ij} |\psi_{ij}(x)^2| \tag{3}$$

where

$$n_{ij} = \frac{n_{vi} m_{di} kT}{\pi \hbar^2} \ln\left[1 + \exp\left(\frac{E_F - E_{ij}}{kT}\right)\right] \tag{4}$$

where n_{inv} is the total inversion carrier concentration, n_{ij} is carrier concentration in the jth subband of the ith valley, E_{ij} is the corresponding eigen energy, E_F is the Fermi energy, n_{vi} is valley degeneracy and m_{di} is density-of-states effective mass in ith valley. The eigen energy E_{ij} is obtained solving the one dimensional Schrödinger's equation,

$$\left[-\frac{\hbar^2}{2m^*}\frac{d^2}{dx^2} + qV(x)\right]\psi_{ij}(x) = E_{ij}\psi_{ij}(x) \tag{5}$$

where $\psi_{ij}(x)$ is the corresponding wavefunction of E_{ij}, $V(x)$ is the potential obtained from (1) and m^* is the effective mass. For <100> oriented silicon surfaces, quantization effective masses are $0.916m_o$ for longitudinal valley and $0.19m_o$ for transverse valley (m_o is rest mass of electron), $n_{vi} = 2$ and $n_{vi} = 4$ for longitudinal and transverse valleys respectively. The density-of-states effective mass m_{di} is $0.190m_o$ for longitudinal valley and $0.417m_o$ for transverse valley. For holes, the effect of heavy hole and light holes are more significant than the split-off holes and are taken into account for evaluating hole quantization. The quantization effective masses of light and heavy holes are $0.20m_o$ and $0.29m_o$ respectively. The density-of-states effective mass m_{di} is $0.169m_o$ for light holes and $0.433m_o$ for heavy holes. For both heavy holes and light holes $n_{vi} = 1$. Effective mass in oxide is considered to be $0.4m_o$.

C. Numerical Analysis

The depletion width x_d is updated while solving the Poisson's equation (1) that is used to estimate the new depletion charge density ρ_{dep}. As a new inversion charge density ρ_{inv} is obtained from Schrödinger's solution, these two updated charge density are substituted in (1) to solve Poisson's and Schrödinger's equations (1 and 5) iteratively until two successive solution produce result within the given convergence limit.

For solution of Schrödinger's equation in the n-th iteration, the updated potential profile is given by,

$$V_n = V_{n-1} + f(V_p - V_{n-1}) \quad (6)$$

where V denotes potential and n is the index of iteration. V_p is the solution from the Poisson's equation using the updated charge densities and f is the relaxation factor to control the speed of convergence. Extensive simulation has been carried out and the best performance for the proposed method has been obtained with $f = 0.05$.

Here, V_{th} has been defined as the gate voltage at which carrier concentration per unit area, N_{inv} reaches a value $N_{th} = 2 \times 10^{14} m^{-2}$, adequate to achieve the device turn on condition (Fig. 2). N_{inv} is obtained by integrating n_{inv} over the total device thickness, t_{total} *i.e.*

$$N_{inv} = \int_{t_{total}} n_{inv} dx \quad (7)$$

where, $t_{total} = t_{oxf} + t_{si} + t_{oxb} + t_{sub}$ (Fig. 1b).

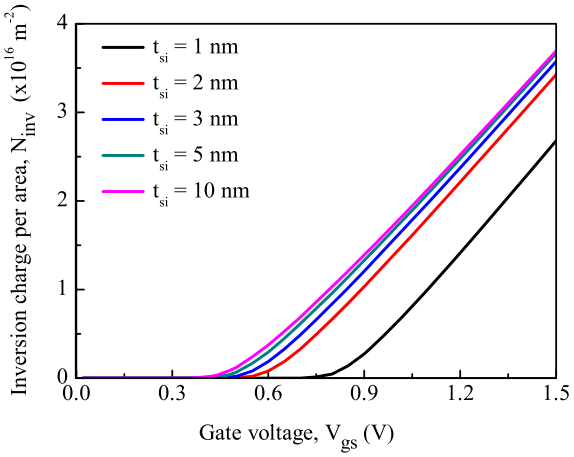
III. Analysis of Threshold Voltage

In fully depleted (FD) SOI, the body is thinner than channel depletion width and body voltage effect on V_{th} can be neglected [16]. So the dependence of V_{th} on some other factors such as-silicon film thickness, channel doping and operating temperature have been analyzed in this paper to observe their quantum mechanical effects on V_{th}.

A. Effect of Doping and Energy Quantization

In ultrathin body devices, channel doping concentration has significant effect on controlling the threshold voltage. In the absence of channel dopants, impurity scattering effect is minimized and depletion charge can not exist in the channel [17]. So band bending is negligible and the potential well is almost of rectangular shape. Hence, the undoped ultrathin-film device will behave mostly like intrinsic and the 1-D Poisson's equation yields a linear potential distribution across the channel. Since $\rho_{dep} = 0$ for undoped channels (from (1)), there is less charge density and hence, there occurs a smaller electric field compared to heavily-doped channel devices in the inversion region. The small electric field results in a lowering of the ground state energy and reduced carrier confinement [17]. This effectively causes a lower V_{th} for undoped SOI devices than the heavily doped ones. Fig. 2 shows the effect of doping on V_{th} for SOI structure considering all other parameters same. The device has the following dimension: front oxide thickness $t_{oxf} = 5$ nm, buried oxide thickness $t_{box} = 40$ nm and acceptor doping level $N_a = 10^{17}$ cm^{-3} for doped structure. For similar device structure, the doped SOI shows higher threshold voltage V_{th} compared to the undoped one.

Table I shows the effect of doping concentration on V_{th} with four values of N_a. It reveals that V_{th} increases as N_a is increased.



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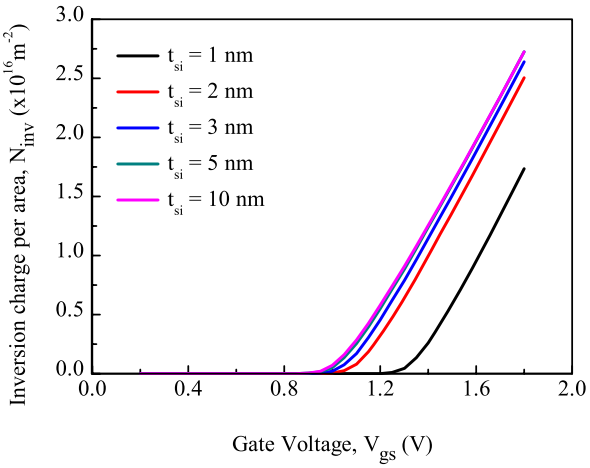


(b)

Fig. 2: Effect of channel doping on threshold voltage (a) for undoped film (b) for doped film with doping concentration $N_a = 10^{17}$cm^{-3}

TABLE I: Values of V_{th} for different doping concentrations

Si thickness t_{si} (nm)	Doping Concentration N_a (cm^{-3})			
	10^{16}	5×10^{16}	10^{17}	5×10^{17}
10	0.9323	0.9802	1.007	1.1058
1	1.1986	1.2448	1.2621	1.3198

B. Effect of Channel Thickness

V_{th} depends greatly on Si film thickness for SOI MOSFETs. The V_{th} increases as t_{si} is reduced. With decreasing t_{si}, the distance between ground state eigen energy and conduction band Ec becomes larger. So the carriers have to go in higher energy sub-band. The Fermi level (E_F) also moves towards ground state eigen energy. These results in a higher V_{th} [6]. This has been realized for both doped and undoped SOI

structure as shown in Fig. 2. As t_{si} has been increased from 1 nm to 10 nm, V_{th} has significantly reduced which reveals this quauntum mechanical phenomena on the V_{th}.

IV. Temperature Dependence on the Threshold Voltage

V_{th} is sensitive to operating temperature. The Fermi energy level in the SOI layer remains below the ground state energy about kT/q at the threshold condition [2] and hence affects V_{th}. The dependence of V_{th} with respect to temperature can be expressed from the following equation [1]:

$$\frac{dV_{th}}{dT} = \frac{d\phi_F}{dT}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\epsilon_{si}N_a}{kT\ln\left(N_a/n_i\right)}}\right] \tag{8}$$

where ϵ_{si} is dielectric constant of Si, N_a is acceptor doping concentration, C_{ox} is oxide capacitance, k is Boltzman's constant, n_i is intrinsic carrier concentration and ϕ_F is potential difference between the Fermi level (E_F) and intrinsic level (E_{Fi}) expressed as [18]:

$$E_{Fi} - E_F = kT\ln\frac{N_a}{n_i} \tag{9}$$

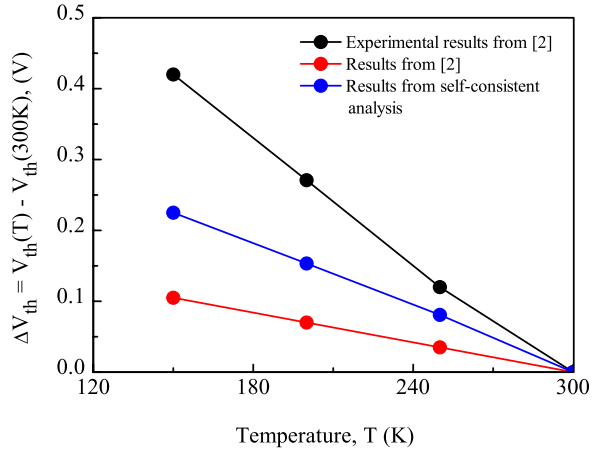
From (8), the inverse relationship with temperature and threshold voltage dominates to increase threshold voltage with decreasing temperature. The temperature dependence of V_{th} has been evaluated for a wide range of temperatures. In the Self-Consistent analysis, temperature effects have been incorporated in the calculation of Fermi level, silicon bandgap and intrinsic carrier concentration. The temperature effect on the Fermi level has been analyzed using (9) where E_{Fi} has been considered at the center of the bandgap of silicon. However, silicon bandgap decreases with temperature according to the following equation [18]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T} \tag{10}$$

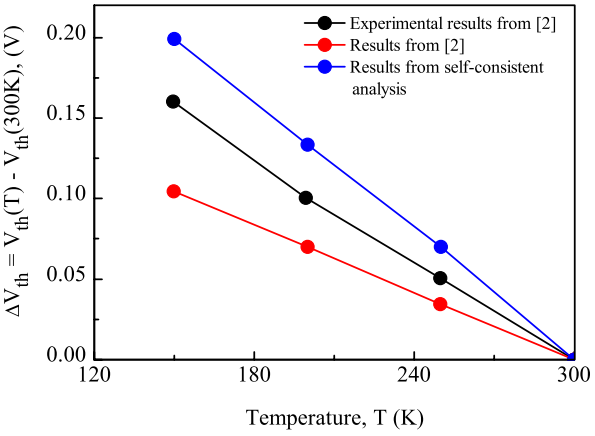
where $E_g(T)$ and $E_g(0)$ refer to the bandgap of silicon at the operating temperature T and 0 K respectively . The parameters α and β have been obtained for silicon as 4.9×10^{-4} ev/K and 655 K respectively [18].

The simulation has been performed in the range from 150 K to 300 K where Boltzman's approximation is clearly valid [19]. The intrinsic carrier concentration at different temperatures has been evaluated utilizing the Fermi-Dirac Integral [19]. Fig. 3 shows the V_{th} shift with temperature. The threshold shift has been plotted for $V_{th}(T) - V_{th}(300K)$. The temperature dependence from the simulation results has been compared with experimental results from [2] and also with the simulation results from [2]. For experimental devices, the dimension was as follows- front oxide thickness $t_{oxf} = 3$ nm or 5 nm, silicon film thickness $t_{si} = 6$ nm or 10 nm, buried oxide thickness $t_{box} = 110$ nm and doping concentration $N_a = 10^{16}\text{cm}^{-3}$.

Fig. 3 shows that the simulated curves of V_{th} shift with temperature using Self-Consistent model follow more closely the experimental data compared to the simulated results from [2]. The model of [2] although predicted near to experimental results [2] for $t_{si} = 6$ nm, showed large deviation when t_{si} is increased to 10nm. Hence, it performs poorly as the film thickness is raised. The proposed Self-Consistent analysis, on the other hand, has performed with good agreement with experimental result for both film thicknesses. Actually, the Self-Consistent approach performs quantum mechanical analysis with 1A^o grid size and convergence error has been maintained as 0.001 which have increased its accuracy. However, the presence of interface states might have increased the V_{th} shift for experimental device beyond the simulation results. Also the temperature effect on poly-Si gate electrode work function ϕ_{ms} has not been considered. These might have been the cause of discrepancies with the experimental result [2].



(a)



(b)

Fig. 3: Threshold voltage shift with temperature from experimental and simulated results for (a) Silicon film thickness 10nm and (b) Silicon film thickness 6nm

V. Analysis of C-V Characteristics

SOI C-V analysis is more complicated due to presence of two oxide-semiconductor interfaces compared to conventional

bulk MOSFETs. The total capacitance is the combination of the oxide and film capacitances, expressed as [12], [14]:

$$C_{oxf} = \frac{\epsilon_{oxf}}{t_{oxf}} \tag{11}$$

$$C_{oxb} = \frac{\epsilon_{oxb}}{t_{oxb}} \tag{12}$$

$$C_{gs} = \frac{dQ_{film}}{dV_{gs}} \tag{13}$$

$$C_{sb} = \frac{dQ_{sub}}{dV_{sb}} \tag{14}$$

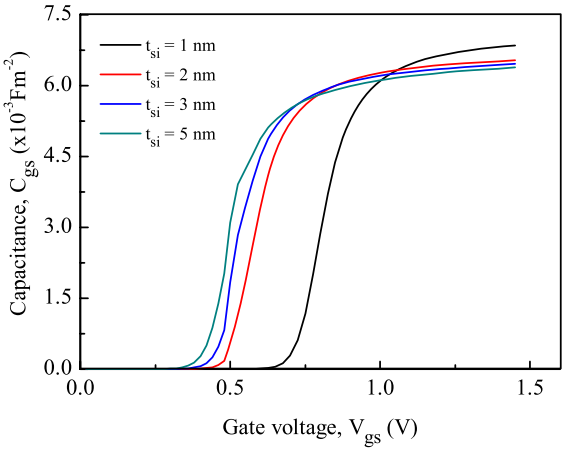
where ϵ_{oxf} and ϵ_{oxb} are permitivity of front and buried oxide and t_{oxf} and t_{oxb} are the respective oxide thickness. C_{gs} is per unit area capacitance in the film for gate voltage and C_{sb} is capacitance between film and substrate. V_{gs} and V_{sb} are the gate voltage and and film to substrate voltage and Q_{film} and Q_{sub} are the corresponding charges of film and substrate. Throughout the analysis carried out here, the voltage at the end of substrate has been taken as reference (0V). Moreover, the SOI device considered here has thick buried oxide layer, so there is few probability of confinement of inversion carriers in the substrate. So the effect of C_{sb} is negligible. The gate and buried oxide capacitances C_{oxf} and C_{oxb} are constant. So the only significant voltage dependent capacitance is C_{gs}.
The capacitance C_{gs} Vs V_{gs} characteristic has been shown in the Fig. 4 for both doped and undoped structure. So this capacitance can be evaluated in the following way [14]:

$$C_{gs} = \int_{film} \frac{\partial \rho(x)}{\partial V_{gs}} dx \tag{15}$$

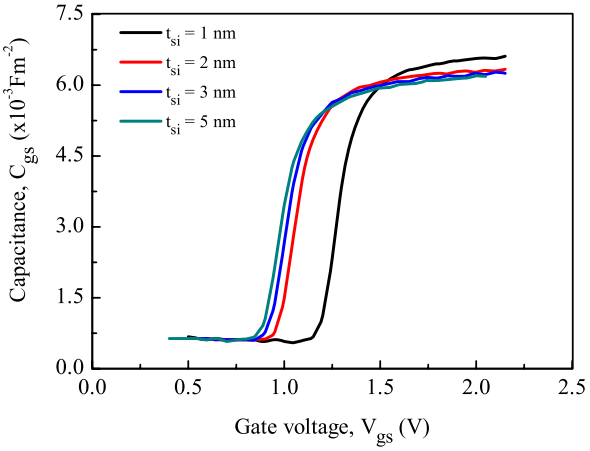
where $\rho(x)$ is the space charge distribution in the film. For intrinsic film, the space charge distribution $\rho(x)$ is the contribution of ρ_{inv} alone where for doped film, $\rho(x)$ is obtained from, ρ_{dep} and ρ_{inv} respectively. Strong inversion condition occurs when the C-V curves start to rise. Note that increasing the film thickness causes reduction of the strong inversion voltage for both doped and undoped film. Thus the C-V characteristics further substantiate the V_{th} dependence on silicon film thickness showing increasing thickness provides achieving faster inversion condition.

VI. Conclusion

The C-V characteristics and threshold voltage dependence on various factors have been observed in this work using the Self-Consistency model for ideal cases. The simulated results showed threshold voltage decreased with temperature although the shifted threshold values had some deviation from experimental results for non-idealities. However, nonideal effects can be easily incorporated in the model such as: fixed charges, trapped charges in oxides and non-zero semiconductor-metal or poly-Silicon barrier heights. Fixed charges and the metal-semiconductor barrier height do not depend on gate voltage and hence, they only lead to a shift of threshold curve which can be included in the flat band voltage V_{FB}. As verified by the experimental results, this work will enhance the field of research of numerical analysis of device characterization by Self-Consistent Model.



(a)



(b)

Fig. 4: Capacitance C_{gs} Vs V_{gs} characteristic for different Si film thickness (a) for undoped film (b) for doped film with doping concentration $N_a = 10^{17}\text{cm}^{-3}$

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