

Balanced and Unbalanced Voltage Sag Mitigation Using DSTATCOM with Linear and Nonlinear Loads

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Abstract—DSTATCOM is one of the equipments for voltage sag mitigation in power systems. In this paper a new control method for balanced and unbalanced voltage sag mitigation using DSTATCOM is proposed. The control system has two loops in order to regulate compensator current and load voltage. Delayed signal cancellation has been used for sequence separation. The compensator should protect sensitive loads against different types of voltage sag. Performance of the proposed method is investigated under different types of voltage sags for linear and nonlinear loads. Simulation results show appropriate operation of the proposed control system.

Keywords—Custom power, power quality, voltage sag mitigation, current vector control.

I. INTRODUCTION

POWER quality is one of the most important topics that electrical engineers have been noticed in recent years. Voltage sag is one of the problems related to power quality. This phenomenon happens continuously in transmission and distribution systems. During a voltage sag event, amplitude of the effective load voltage decrease from 0.9 of the nominal load voltage to 0.1 in very short time (less than one minute). Short circuit, transformer energizing, capacitor bank charging etc are causes of voltage sag. Voltage sag has been classified in 7 groups of A-G [1]. According to this classification most of voltage sags are companion with a phase angle jump (types C, D, F and G). Phase angle jump for power electronics systems such as ac-ac and ac-dc converters, motor drives etc is harmful [2]. Therefore, phase angle jump compensation is one of the voltage sag mitigation goals.

Most industries and companies prefer electrical energy with high quality. If delivered energy to these loads has poor quality, products and equipment of these loads such as microcontrollers, computers, motor drives etc are damaged. Hurt of this phenomenon in companies that dealing with information technology systems is serious. According to a study in U.S., total damage by voltage sag amounts to 400 Billion Dollars [3]. For these reasons power quality mitigation in power systems is necessary. Nowadays, Custom Power equipments are used for this purpose. DSTATCOM is one of these equipments which can be installed in parallel with

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sensitive loads. This device mitigates the load voltage by injecting necessary current to the system. Fig. 1 shows the structure of the DSTATCOM and how it connects to the system for mitigation purposes.

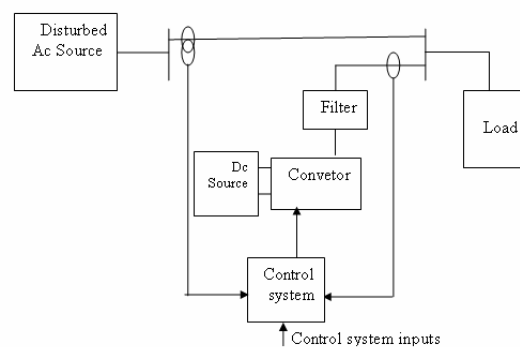


Fig. 1 DSTATCOM constituents and its connection to system

Some methods that have been allocated for voltage sag mitigation using DSTATCOM only take balanced voltage sag into account [4-5]. However, most of the voltage sags are unbalanced. Unbalanced three phase voltages in synchronous reference frame (SRF) generate two components (d and q components) that oscillate with twice frequency of the fundamental frequency. This specialty is not suitable for control purposes.

In references [6] and [7] for improvement of these imperfections, sequence components of voltage and current have been separated in synchronous reference frame. After transformation of three phase voltages or currents to positive synchronous reference frame, a dc component and oscillating component with twice frequency of fundamental frequency are generated. For elimination of oscillating component, an appropriate filter is applied, thus, positive sequence of synchronous reference frame is generated [6].

Delayed signal cancellation (DSC) is considered as a simple method for sequence separation [8]. Sequence components generated by this method are dc quantities; which are desired for control purposes.

The proposed control method in this paper is formed by two control loops. One loop is considered for compensator current regulation and the other one for point of common coupling (PCC) voltage regulation. Vector current control (VCC) [9] has been used for compensator current regulation. The

reference control currents for current control loop generated by the voltage control loop. Measured three phase voltages at PCC are transformed into positive and negative sequence components in synchronous reference frame and compared with the reference quantities. Error signals are then passed through PI controllers to produce reference currents. These reference quantities are fed to the current control loop so that reference voltages are generated. According to the reference voltage, PWM unit generates switching pulses. In this paper the performance of the proposed control system with the presence of linear and nonlinear loads has been studied.

II. CONTROL METHOD

Fig. 2 depicts the control system of compensator where three phase voltages at PCC are transformed into sequence components and compared with their reference values. Error signals are fed into the PI controllers in order to produce reference currents for current control loop. Sequence components of reference voltage are:

$$u_{dp}^* = \max(V_{L-L}); u_{dn}^* = 0; u_{qp}^* = 0; u_{qn}^* = 0$$

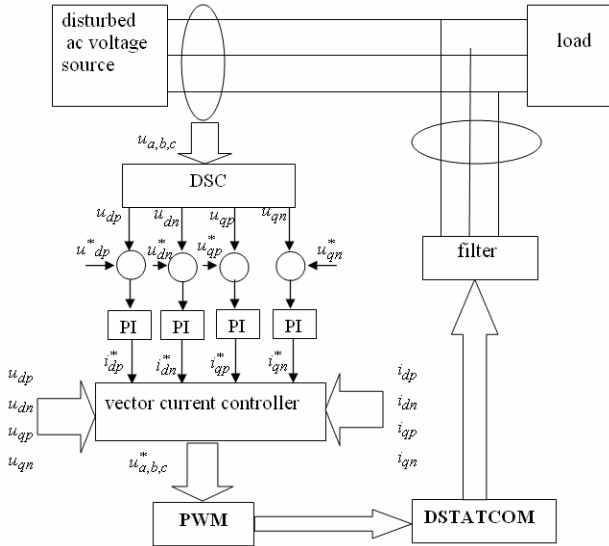


Fig. 2 Control system for voltage sag mitigation using DSTATCOM

A. Sequence Component Separation

In order to separate sequence components, delayed signal cancellation (DSC) method has been used [8]. Equations (1) and (2) shows that how sequence components are obtained by use of this method.

$$u_p^{dq}(k) = (u^{dq}(k) + u^{dq}(k - \frac{f_s}{4f_g})) \quad (1)$$

$$u_n^{dq}(k) = (u^{dq}(k) + u^{dq}(k - \frac{f_s}{4f_g})) \quad (2)$$

Fig. 3 shows block diagram which represents equations (1) and (2). According to this figure, firstly three phase components (abc) are transformed into α, β components. Then, by use of a phase lock loop (PLL), α, β components are transformed into positive and negative synchronous reference frame (u_p^{dq}, u_n^{dq}). The obtained signals are delayed by $T/4$ and added to the initial signal then multiplied by $1/2$ to generate sequence components.

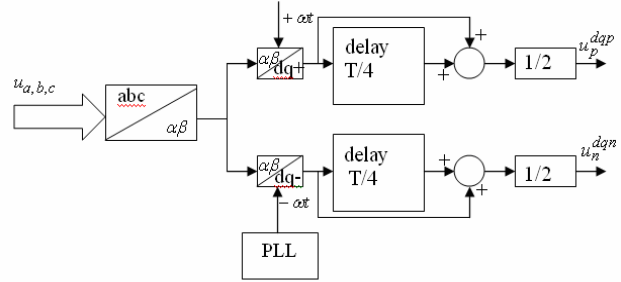


Fig. 3 Delayed signal cancellation block diagram

B. Vector Current Controller

The aim of vector current controller is to follow the reference control current by compensator current. For this purpose converter switching should be regulated. Inputs of vector current controller consist of: sequence components of PCC voltage ($u_{dp}, u_{dn}, u_{qp}, u_{qn}$), sequence components of reference current generated by voltage controller loop ($i_{dp}^*, i_{dn}^*, i_{qp}^*, i_{qn}^*$) and sequence components of injected current by the compensator to the system ($i_{dp}, i_{dn}, i_{qp}, i_{qn}$).

Sequence components of reference voltage applied to the PWM module are obtained from equations (3)-(6) [9].

$$u_{dp}^* = u_{dp} + R_f i_{dp} - (\omega L_f)(i_{qp} + i_{qp}^*) + PI(i_{dp}^* - i_{dp}) \quad (3)$$

$$u_{dn}^* = u_{dn} + R_f i_{dn} + (\omega L_f)(i_{qn} + i_{qn}^*) + PI(i_{dn}^* - i_{dn}) \quad (4)$$

$$u_{qp}^* = u_{qp} + R_f i_{qp} - (\omega L_f)(i_{dp} + i_{dp}^*) + PI(i_{qp}^* - i_{qp}) \quad (5)$$

$$u_{qn}^* = u_{qn} + R_f i_{qn} + (\omega L_f)(i_{dn} + i_{dn}^*) + PI(i_{qn}^* - i_{qn}) \quad (6)$$

In the above equations, R_f is filter resistance and L_f is filter inductance where the filter is placed in series with the compensator. Reference voltages are transformed into three phase coordinates and exerted to PWM unit so that switching pulses are generated.

Harmonic contents of the compensated voltage is about 5.2% (THD=5.2%) so that load voltage harmonic is acceptable.

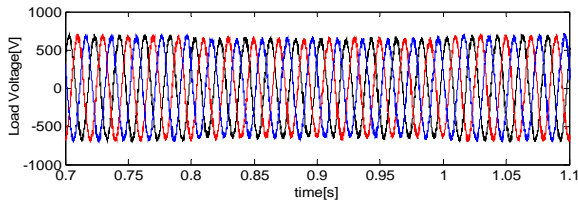


Fig. 6(a)

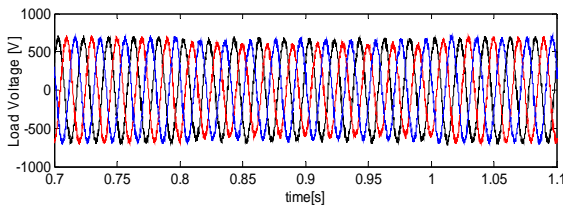


Fig. 6 (b)

Fig. 6 Load voltage after compensation (a) balanced voltage sag (b) unbalanced voltage sag unbalanced

Fig. 7 shows the injected current to power system for voltage sag compensation. According to this figure in balanced voltage sag the injected current is balanced and in unbalanced voltage sag the injected current is unbalanced as expected. In this case the voltage decrease in one phase is higher than others. The injected current amplitude for one phase is higher than other two phases (Fig. 6 (b)).

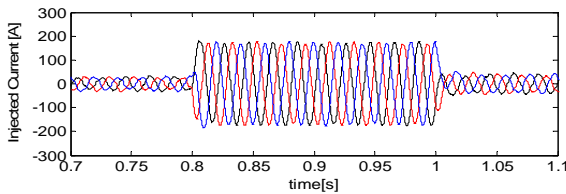


Fig. 7(a)

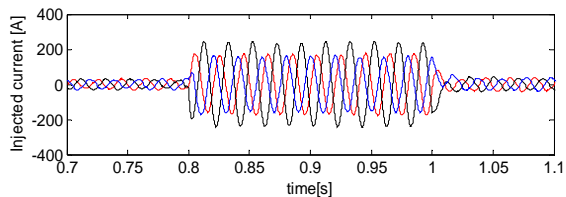


Fig. 7(b)

Fig. 7 Injected current by compensator (a) balanced voltage sag (b) unbalanced voltage sag

Mentionable that for decreasing the load voltage harmonics, multilevel converters and other switching methods can be used. Fig. 8 shows sequence components of injected current to system. It is obvious that these components are dc. According to Fig. 8 (a), the injected current in balanced voltage sag is balanced so that only d component of positive sequence current (i_{dp}) exists and other components are zero.

Fig. 8 (b) shows sequence components of injected current in unbalanced voltage sag conditions. The injected currents

are also unbalanced so that in addition to d component of positive sequence other components also exist.

It is obvious that amplitude of the injected current by compensator depends on the depth of voltage sag. The deeper the voltage sag is, the higher the amplitude of injected current is. Other types of voltage sags have also been simulated and compensated by this method. The parameters of the simulated voltage sags have been introduced in Table II. The injected active and reactive power for compensation of these types of voltage sags are also calculated as shown in Table III.

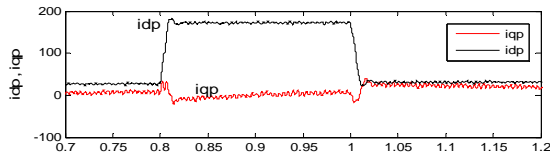


Fig. 8 (a)

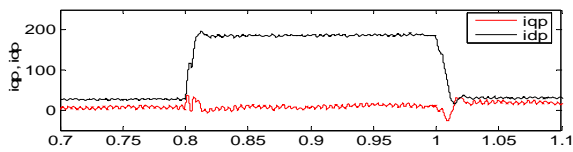


Fig. 8 (b)

Fig. 8 Sequence component of compensator current (a) balanced voltage sag (b) unbalanced voltage sag

TABLE II
PROPERTIES OF DIFFERENT TYPES OF SIMULATED VOLTAGE SAG

Type A	Type B	Type C	Type F	Type G
$200\angle 0^\circ$	$200\angle 0^\circ$	$400\angle 0^\circ$	$200\angle 0^\circ$	$334\angle 0^\circ$
$200\angle -120^\circ$	$400\angle -120^\circ$	$265\angle -140^\circ$	$361\angle -106^\circ$	$241\angle -134^\circ$
$200\angle 120^\circ$	$400\angle 120^\circ$	$265\angle 140^\circ$	$361\angle 106^\circ$	$241\angle 134^\circ$

TABLE III

INJECTED ACTIVE AND REACTIVE POWER BY COMPENSATOR

Voltage sag type	Injected Active Power (kW)	Injected Reactive Power (kVar)	(THD)%
Type A	20	120	5.83
Type B	20	40	5.26
Type C	40	95	5.10
Type F	45	60	5.11
Type G	40	70	5.3

According to the data in Table III, the types of voltage sag that companion with phase angle jump (types C, F and G) need more active power for phase angle jump compensation

than other types of voltage sag. Also for amplitude compensation reactive power is needed so that the deeper voltage sag, more reactive power for compensation is required.

B. Compensation of Nonlinear Load Voltage

For assessment of the effect of nonlinear load on performance of the proposed control system, a rectifier with dc motor load has been considered. The DC motor is a separately excited motor and its parameters are shown in Table IV.

Simulated balanced and unbalanced voltage sags are generated at PCC. Load voltages are similar to Fig. 5. Fig. 9 shows armature current during balanced and unbalanced voltage sags and Fig. 10 shows motor speed variations during the voltage sag event.

TABLE IV
DC MOTOR PARAMETERS

load torque	Field resistance	Armature resistance	Field voltage	Rated speed	Rated voltage
200 n-m	58.8 ohm	0.1968 ohm	300 Volts	1750 rpm	700 Volts

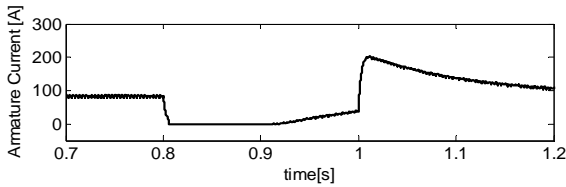


Fig. 9 (a)

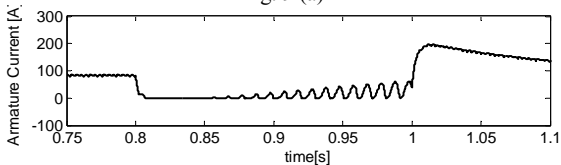


Fig. 9 (b)

Fig. 9 Armature current of DC motor (a) balanced voltage sag (b) unbalanced voltage sag

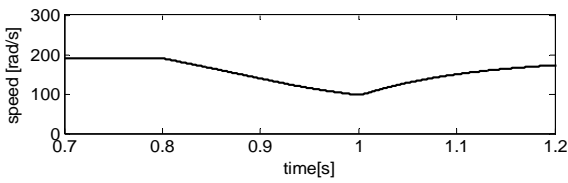


Fig. 10 (a)

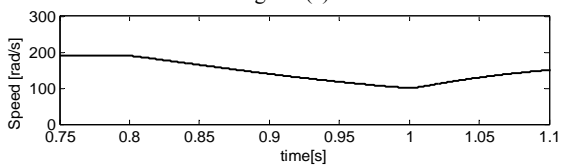


Fig. 10 (b)

Fig. 10 DC motor speed variation during (a) balanced voltage sag (b) unbalanced voltage sag

According to Fig. 9 when the voltage sag happens motor supply voltage decreases (ie $V_t < E_a$), so armature current

tends to flow into power system, but rectifier blocks armature current. During voltage sag motor speed decreases and so E_a decreases. At the instant where $E_a = V_t$ current flow into motor and armature current starts to increase. When voltage sag is cleared, motor supply voltage increases and the armature current increases. Fig. 11 shows load voltage waveform after compensation. Fig. 12 shows armature current waveform and Fig. 13 shows motor speed variations.

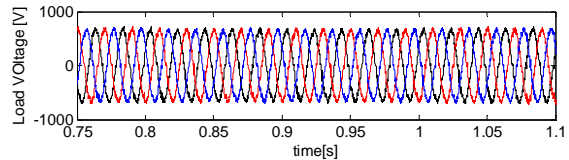


Fig. 11 (a)

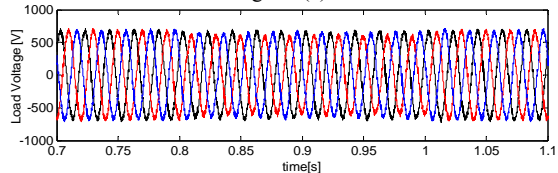


Fig. 11 (b)

Fig. 11 Nonlinear load voltage after compensation (a) balanced voltage sag, (b) unbalanced voltage sag

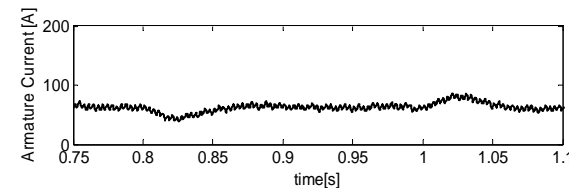


Fig. 12 (a)

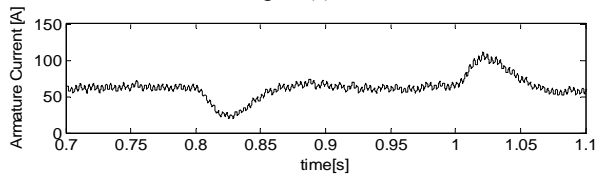


Fig. 12 (b)

Fig. 12 Armature current of dc motor after compensation of (a) balanced voltage sag and (b) unbalanced voltage sag

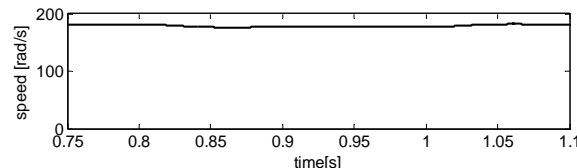


Fig. 13 (a)

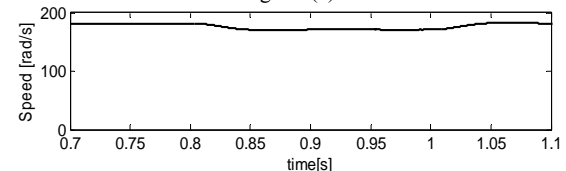


Fig. 13 (b)

Fig. 13 DC motor speed variation after compensation of (a) balanced voltage sag and (b) unbalanced voltage sag

According to Fig. 11, with nonlinear load, the proposed control system compensates balanced and unbalanced voltage sags so that the load type does not affect the control system operation. The reason is that the control system is independent of load current as in accordance to equations (3)-(6). According to Figs. 12 and 13 the load operation after compensation of voltage sag is similar to normal condition.

IV. CONCLUSION

In this paper a new control method for voltage sag mitigation using DSTATCOM is proposed. Three phase voltages and currents are transformed to sequence components and hence the control variables are dc quantities. This specialty results in simplicity of the control system. The proposed control system includes two controllers: one for compensator current regulation and other for load voltage regulation. Voltage controller consists of four PI controllers to control the compensator current and load voltage. By proper adjustment of PI gains, harmonic contents of the compensated voltage can be controlled. According to the simulation results, the proposed method can mitigate the balanced and unbalanced voltage sags and phase angle jump. Performance of the proposed control system has been studied with different types of voltage sags. According to the simulation results the capability of the compensation system in presence of linear and nonlinear loads is investigated and the ability of the proposed system is highlighted.

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