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Backplane Serial Signaling and Protocol for Telecom Systems

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***Abstract*—**In this paper, we implement a modern serial backplane platform for telecommunication inter-rack systems. For combination high reliability and low cost protocol property, we applied high level data link control (HDLC) protocol with low voltage differential signaling (LVDS) bus for card to card communicated over backplane. HDLC protocol is a high performance with several operation modes and is famous in telecommunication systems. LVDS bus is a high reliability with high immunity against electromagnetic interference (EMI) and noise.

Keywords—Backplane, BLVDS, HDLC, EMI, I2C, LCT, OSC, SFP, SNMP.

I. Introduction

FOR modular design and implementation of telecommunication systems, serial backplane is one of new methods that large reduced the volume of physical signal tracks and connector pins [1]. In this case, the subrack is a common domain that managed by control card as a master and other cards such as: Transponders and Optical Supervisory Channel (OSC) as slaves. Safe hot plug and unplug cards, plug and play is another goal of this method.

Because handle and manage of the HDLC protocol is low cost and fully public in telecommunication device and systems [2,3], this protocol selected for creating the physical layer of this network therefore application layer processing of system take a low percent of CPU loading when applied HDLC controller devices.

For high immunity against EMI and noise in the serial back plain, LVDS bus technology selected and implemented [4,5].

II. Transmission System Requirements and Our Solutions

Control and monitoring of the lasers, detector and event logging are three main requirements of the optical Network Element (NE). The new type and Multi Source Agreement (MSA) of optical transceiver module is the Small form Factor Pluggable (SFP). The SFP module is a compact transceiver with internal monitoring and control over Inter-Integrated Circuit (I2C) interface and hot pluggable ability [6]. We use two SFP modules on the each transponder cards in both Tx and Rx optical link directions. One advanced microcontroller with on chip I2C bus driver used for access to SFP module. This microcontroller can control, monitor and calibrate value of measurement parameters such as: laser transmitter power, receiver power, bias current and etc. This microcontroller also buffers all important SFP module data to dedicated location over on-chip RAM memory and performs primary processing as data conditions that required for system Control, Monitoring and Logger (CML) card.

One channel HDLC controller device that applied on control card for master and each cards for slave, covers the physical layer for point to multi-point communication over the in subrack NE.

The CML card has powered by Ethernet port that carries Simple Network Management Protocol (SNMP) packets and monitoring and event logging purpose. All of these functions can be performed into Local Craft Terminal (LCT) via simple serial terminal RS232 and Fast Ethernet (FE) port.

Remote access to these requirements realized by OSC. OSC card carries the manager information traffic over optical fiber that optically multiplexed with other main client traffic into dedicated channel. In our solution, any NE defines an Internet Protocol (IP) address. If IP address filed of Ethernet packet differ with CML IP address, after comparison with gateway address, a routing mechanism send IP packets through OSC channel to far NE. With this method we can implement Point-to-Point network topology with multi add/drop NE. Fig. 1 illustrate block diagram of topology.

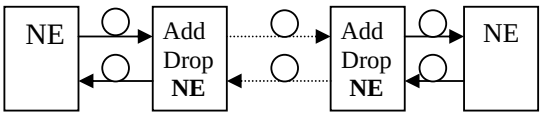

Fig. 1 Block diagram of Point-to-Point network topology with multi add/drop NE.

III. Serial backplane versus Parallel backplane

Serial interconnect for use in serial backplanes have many significant benefits over conventional parallel interconnected backplanes. The first and most important is the performance and reliable/robust operation of the serial connection.

By converting the “local” parallel data to serial, it greatly reduces the number of traces, thus allowing the reduction of the backplane size and complexity. The backplane PCB is the

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largest and most expensive board in many systems. In fact, the actual size of the system backplane, in many cases is the limiting factor for system size. The two main reasons for implementing a serial backplane are (1) the high data throughput with reliable performance and (2) backplane PCB size reduction. The latter is realized through smaller form factor of the system rack, fewer layers of PCB material, resulting in lower cost.

IV. Backplane design considerations and Bus LVDS

Current serial signaling technologies utilize a differential Input/Output (I/O) buffer. The differential buffers provide much smaller signal swings compared to historical single ended buffers. This reduced signal swing, results in a lower power I/O buffer, but more importantly, it significantly lowers noise. The noise reduction benefit is seen in much lower EMI, ground bounce and transmission line effects including crosstalk and reflections.

On the other hand differential data transmission method used in LVDS is less susceptible to common mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to transmit data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers, which looks at only the difference between the two signals. Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Switching spikes in the driver are very small, so that current does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5 mA × 350 mV = 1.2 mW) is very small in magnitude.

V. HDLC as a High Reliable Protocol

HDLC is a bit orient switched/non-switched layer 2 data link control protocol. HDLC developed by International Organization for Standardization (ISO). It has been so widely used in telecommunication because it supports both: half duplex and full duplex communication lines, point to point and multi-point networks, single-master/multi-master configuration and switched/non-switched channels. The procedures outlined in HDLC are designed to permit synchronous, code-transparent data transmission. Other benefits of HDLC are that the control information is always in the same position, and specific bit patterns used for control differ dramatically from those in representing data, which reduces the chance of errors.

A combined station is a combination of a master and slave station. Connection between CML card and OSC card is a combined station. Both combined stations are able to send and receive commands and responses without any permission from any other stations. Each combined station is in fully controlled by itself.

VI. Implementation of Serial Backplane with LVDS Bus and HDLC Protocol

Flow chart of CML and OSC cards for data transaction is illustrated in fig. 2. This describes the physical layer of Ethernet packet data transaction.

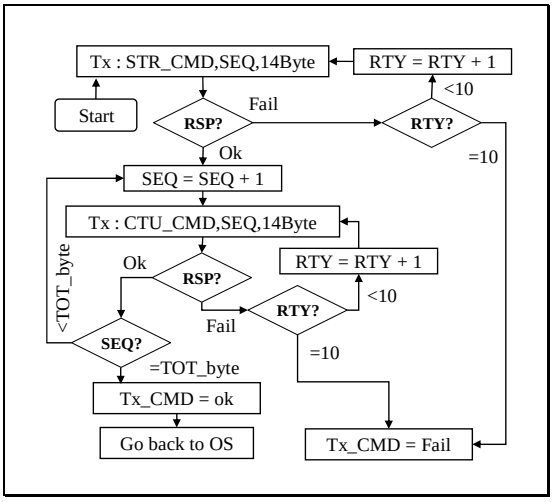

Fig. 2 Flow chart of physical layer data transaction

A. CML Card

All of Telecom systems requirement for control, monitoring and logging process developed in CML card. Interface oriented block diagram of CML card illustrated in fig. 3.

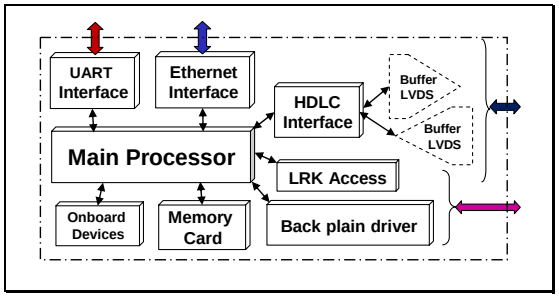

Fig. 3 Block diagram of CML card

Access of CML card to other cards Flow chart through serial backplane illustrated in fig. 4.

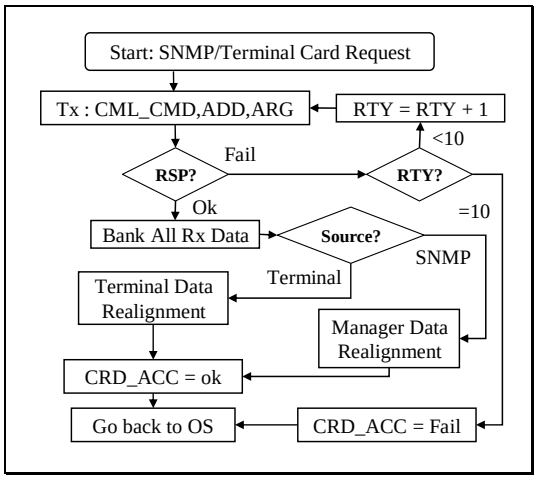

Fig. 4 Flow chart of CML card for access to other cards

B. Transponder Card

Transponder card have 8 bit, 8 MHz general purpose RISC microcontroller for control and monitoring of SFP, send and receive data packet to CML card with HDLC channel 1 via backplane. Fig. 5 shows hardware block diagram of the transponder card.

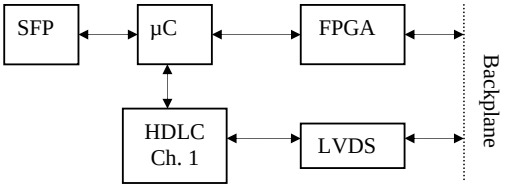

Fig. 5 Block diagram of transponder card

After received packet from backplane the transponder compare address fields of packet then analyze the command and generate related response.

C. OSC card

OSC card has advanced RISC microcontroller for control and monitoring of SFP, send and receive data packet to CML card with two channels HDLC via backplane initialize and handling Order Wire (OW) over coder-decoder (CODEC) bock. Fig. 6 shows hardware block diagram of the transponder card.

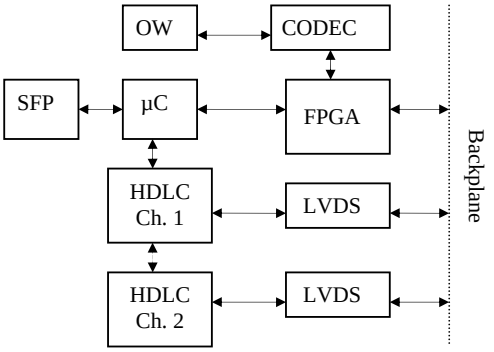

Fig. 6 Block diagram of OSC card

VII. Conclusions

In this project we implement reliable and high performance single master of point-to-multipoint and multi master of point-to-point serial backplane. This configuration expanded with OSC to IP based multi NE ring topology over fiber optic.

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