

Average Current Estimation Technique for Reliability Analysis of Multiple Semiconductor Interconnects

Ki-Young Kim, Jae-Ho Lim, Deok-Min Kim, and Seok-Yoon Kim

Abstract—Average current analysis checking the impact of current flow is very important to guarantee the reliability of semiconductor systems. As semiconductor process technologies improve, the coupling capacitance often become bigger than self capacitances. In this paper, we propose an analytic technique for analyzing average current on interconnects in multi-conductor structures. The proposed technique has shown to yield the acceptable errors compared to HSPICE results while providing computational efficiency.

Keywords—current moment, interconnect modeling, reliability analysis, worst-case switching

I. INTRODUCTION

As process technology for semiconductor goes beyond the ultra-deep submicrometer (below 45nm) regime, interconnect reliability on a chip has become a serious design concern. As process technologies improve, the distance between interconnects has gradually become closer. Due to this, the coupling capacitance between adjacent interconnects is getting larger than their self capacitances. In general, the coupling capacitance is considered to be 1~6 times the self capacitance in the recent processes [1]~[6].

Electromigration in interconnects has been a persistent problem since the very early days of chips design. Power distribution networks have always been considered highly susceptible to electromigration failures due to their high average current densities. Thus, average current analysis at an early stage of design has to be done to guarantee the reliability of the design.

In this paper, an analytic technique for analyzing the current variations on interconnect due to the influence of the current in two adjacent interconnects is proposed. Although the current in an interconnect could be physically influenced by all adjacent interconnects, this paper focuses on the current estimation on one interconnect (Victim) with two most influencing interconnects (Aggressors 1 and 2).

The worst-case switching scenario may be when the Victim is

switched from 0V to V_{DD} and Aggressor 1 and 2 are switched from V_{DD} to 0V (or when the Victim's voltage is falling and the Aggressors' voltage is rising), as shown in Fig. 1, since the current flow in the Victim reaches its maximum at this instant.

Generally, the performance under the worst-case scenario should be analyzed as a guarantee of reliability and the current values estimated in this paper can ultimately be utilized for reliability analysis. Therefore, the analysis in this paper will be carried out by focusing on the worst-case average current value in the Victim.

This paper is organized as follows. We briefly review the concept of the circuit moments and current moments in Section II, and describe the technique for analyzing average current in a single interconnect in Section III. In Section IV, we present our analytical method for computing the average current in multi conductors and summarize the experimental results in Section V. Finally, conclusions are given in section VI.

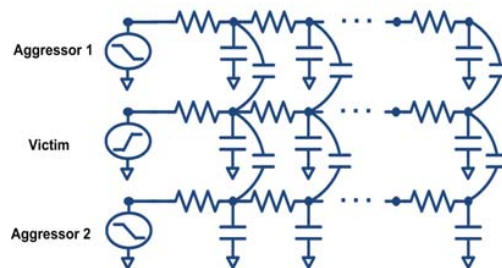


Fig. 1 Worst-Case Switching Scenario

II. BACKGROUND

A. Concepts of Circuit Moments

To understand higher order moments, consider a transfer function in the Laplace domain as (1).

$$H(s) = \frac{b_0 + b_1s + b_2s^2 + \dots + b_ms^m}{1 + a_1s + a_2s^2 + \dots + a_ns^n} \quad (1)$$

Let $h_i(t)$ be the voltage transfer function at any node i in an RC or RLC circuit and $H_i(s)$ be the Laplace transform of $h_i(t)$. The voltage at node i can be expressed as (2).

Ki-Young Kim was with School of Computing, Soongsil University, Sando-dong 511, Dongjak-Gu, Seoul, Korea and is now with Samsung LED Co., Ltd (phone: +82-2-813-0682; fax: +82-2-813-0682; e-mail: kky@ic.ssu.ac.kr). The other authors are with School of Computing, Soongsil University, Sando-dong 511, Dongjak-Gu, Seoul, Korea (e-mails: ljh1424@ic.ssu.ac.kr, kimdm@ic.ssu.ac.kr, and ksy@ssu.ac.kr, respectively.).

$$V_i(s) = H_i(s) \times V_{in}(s) \quad (2)$$

where $V_{in}(s)$ is the Laplace transform of the input voltage waveform. Expanding (1) about $s=0$, we can express the transfer function as an infinite series in powers of s

$$H_i(s) = m_0^i + m_1^i s + m_2^i s^2 + m_3^i s^3 + \dots = \sum_{q=0}^{\infty} m_q^i s^q$$

$$\text{where } m_q^i = \frac{1}{q!} \left| \frac{d^q H_i(s)}{ds^q} \right|_{s=0} \quad (3)$$

The time and frequency domain relationship follows from the Laplace transform of $h_i(t)$

$$H_i(s) = \int_0^{\infty} h_i(t) e^{-st} dt \quad (4)$$

Expanding e^{-st} about $s=0$ in (5) yields:

$$H_i(s) = \int h_i(t) \left[1 - st + \frac{1}{2}(s^2 t^2) - \frac{1}{6}s^3 t^3 + \dots \right] dt$$

$$= \sum ((-1)^k / k!) s^k \int_0^{\infty} t^k h_i(t) dt \quad (5)$$

It follows from (5) that the q -th coefficient of the impulse response $h_i(t)$ is

$$m_q^i = ((-1)^q / q!) \int_0^{\infty} t^q h_i(t) dt \quad (6)$$

We refer to the series coefficients in (3) and (6) as moments.

B. Current Moment Calculation at Resistive Elements

For the concept and calculation method of Circuit moments, refer to [7]-[9]. In this section, we show how to compute the moments of current waveforms through any resistive element in an RC tree in terms of the circuit moments [10]. Let us consider a generic case where we want to compute the current flowing through a resistive element R_{ij} for a rising transition $V_{in}(t)$ at the source node as shown in Fig. 2.

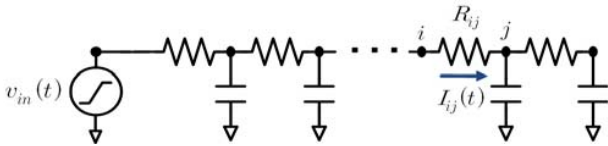


Fig. 2 Current Flowing through a Resistive Element R_{ij}

Here, we focus on the analysis of RC circuits for given time-varying voltage inputs. If $V_i(s)$ and $V_j(s)$ represent the Laplace transforms of voltage waveform at nodes i and j , respectively, then the current I_{ij} through the resistance R_{ij} in the frequency domain can be expressed as

$$I_{ij}(s) = V_i(s) / V_j(s) \quad (7)$$

Let us remind (2), and if $H_i(s)$ and $H_j(s)$ represent the voltage transfer functions at node i and j respectively, then the current expression from (7) can be rewritten as

$$I_{ij}(s) = H_i(s) \times V_{in}(s) - H_j(s) \times V_{in}(s) / R_{ij}$$

$$= V_{in}(s) / R_{ij} \cdot (H_i(s) - H_j(s)) \quad (8)$$

The impulse responses $H_i(s)$ and $H_j(s)$ for nodes i and j can be expressed in terms of corresponding circuit as shown in (3). Expression (8) can now be written in terms of the differences in the circuit moments.

$$I_{ij}(s) = (V_{in}(s) / R_{ij}) (\Delta m_1^{ij} s + \Delta m_2^{ij} s^2 + \Delta m_3^{ij} s^3 + \dots) \quad (9)$$

where Each $\Delta m_q^{ij} (= m_q^i - m_q^j)$ represents the difference between the q -th circuit moments of the nodes i and j .

The finite rising ramp input show in Fig. 2 can be expressed in the time domain as

$$v_{in}(t) = (V_{dd} / T_r) [tU(t) - (t - T_r)U(t - T_r)] \quad (t \geq 0) \quad (10)$$

where T_r is the rise time, V_{dd} is the supply voltage and $U(t)$ denotes the step function. The finite ramp in the transform domain is

$$V_{in}(s) = (V_{dd} / T_r) \cdot (1/s^2)(1 - e^{-sT_r}) \quad (11)$$

Next, (11) can be expanded in a Maclaurin series as follows:

$$V_{in}(s) = (V_{dd} / s) \cdot (1 - sT_r/2 + s^2T_r^2/6 - s^3T_r^3/24 + \dots) \quad (12)$$

Expression (9) can now be rewritten by substituting $V_{in}(s)$ and collecting the coefficients of the s -terms in the resulting expression.

$$I_{ij}(s) = 1/R_{ij} \left[\begin{aligned} &\Delta m_1^{ij} + \Delta m_2^{ij} s - (sT_r/2)\Delta m_1^{ij} \\ &+ \Delta m_3^{ij} s^2 - (s^2T_r/2)\Delta m_2^{ij} \\ &+ (s^2T_r/6) \cdot \Delta m_1^{ij} \end{aligned} \right]$$

$$= 1/R_{ij} \left[\begin{aligned} &\Delta m_1^{ij} + (\Delta m_2^{ij} - (T_r/2)\Delta m_1^{ij})s \\ &+ \left(\Delta m_3^{ij} - (T_r/2)\Delta m_2^{ij} \right) s^2 + \dots \\ &+ (T_r/6)\Delta m_1^{ij} \end{aligned} \right] \quad (13)$$

We define the coefficients of the s -terms in the above expression (13) as current moments with m_q^{ij} being the q -th moment of the current waveform through the resistive element between nodes i and j

$$I_{ij}(s) = m_0^{ij} + m_1^{ij} s + m_2^{ij} s^2 + \dots \quad (14)$$

Finally, the first three current moments through an element R_{ij} in the RC circuit can be computed by matching (13) and (14)

$$\begin{aligned}
m_0^{ij} &= \Delta m_1^{ij} / R_{ij} \\
m_1^{ij} &= (1/R_{ij}) (\Delta m_2^{ij} - (T_r/2) \Delta m_1^{ij}) \\
m_2^{ij} &= (1/R_{ij}) (\Delta m_3^{ij} - (T_r/2) \Delta m_2^{ij} + (T_r^2/6) \Delta m_1^{ij})
\end{aligned} \quad (15)$$

III. AVERAGE CURRENT ESTIMATION IN SINGLE INTERCONNECTS

From the definition of the Laplace transform, we know that

$$\begin{aligned}
I_{ij}(s) &= \int_0^\infty I_{ij}(t) e^{-st} dt \\
&= \sum_{n=0}^\infty ((-1)^n / n!) s^n \int_0^\infty t^n \cdot I_{ij}(t) dt
\end{aligned} \quad (16)$$

Comparing (14) and (16), we can obtain the following information about the current waveform in terms of the first three current moments.

$$\begin{aligned}
\int_0^\infty I_{ij}(t) dt &= m_0^{ij} \\
\int_0^\infty t \cdot I_{ij}(t) dt &= -m_1^{ij} \\
(1/2) \cdot \int_0^\infty t^2 \cdot I_{ij}(t) dt &= m_2^{ij}
\end{aligned} \quad (17)$$

The first expression in (17) represents the total area underneath the $I_{ij}(t)$ curve indicating that the zero order current moment represents the total charge through a resistive element during a switching event. The average current through resistance R_{ij} can therefore be easily expressed as

$$I_{ij}^{avg} = (1/T_c) \int_0^{T_c} I_{ij}(t) dt \approx (1/T_c) \int_0^\infty I_{ij}(t) dt = m_0^{ij} / T_c \quad (18)$$

where T_c is the input duration time.

IV. WORST-CASE AVERAGE CURRENT ESTIMATION

A. Superposition Principle for Current Estimation

If the superposition principle is applied to current estimation, it is possible that the current waveform in each resistive element in the Victim can be expressed as the summation of the waveform of $I_{victim}(t)$, $I_{aggressor1}(t)$, $I_{aggressor2}(t)$ shown in Fig. 3. The Current in each resistive element is defined after it is subjected to the following three steps; the final average current value is calculated by summing up the current values at each step.

♦ Step 1

After it is assumed that Aggressor 1 and 2 are quiet (without switching), and only the Victim is switched from 0V to VDD (or from VDD to 0V), the average current when only the Victim is switched as shown in Fig. 3, can be estimated by calculating the current moment for each resistive element in the

Victim and applying that moment to the current estimation technique on a single interconnect.

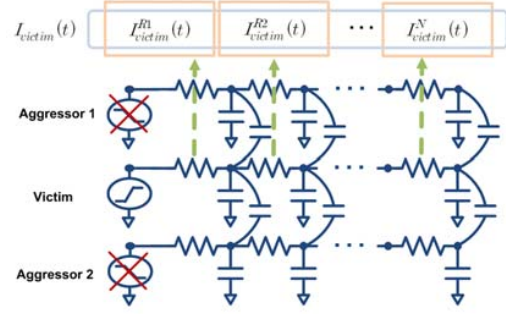


Fig. 3 Scenario When Only the Victim is Switching

♦ Step 2

After it is assumed that Victim and Aggressor 2 are quiet (without switching), and only the Aggressor 1 is switched from VDD to 0V (or from 0V to VDD), the average current when only the Aggressor 1 is switched as shown in Fig. 4, can be estimated by calculating the current moment for each resistive element in the Victim and applying that moment to the current estimation technique on a single interconnect.

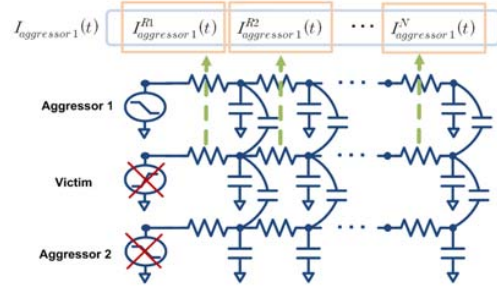


Fig. 4 Scenario When Only the Aggressor 1 is Switching

♦ Step 3

After it is assumed that Victim and Aggressor 1 are quiet (without switching), and only the Aggressor 2 is switched from VDD to 0V (or from 0V to VDD), the average current when only the Aggressor 2 is switched as shown in Fig. 5, can be estimated by calculating the current moment for each resistive element in the Victim and applying that moment to the current estimation technique on a single interconnect.

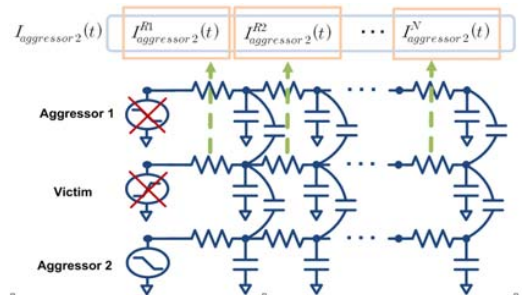


Fig. 5 Scenario When Only the Aggressor 2 is Switching

In Step 1, the total capacitance of the Victim is C_v , the total capacitance of Aggressor 1 is C_{a1} , and the total capacitance of Aggressor 2 is C_{a2} . The coupling capacitance between the Victim and Aggressor 1 is C_{c1} , the coupling capacitance between the Victim and Aggressor 2 is C_{c2} , and the final total capacitance $C_{total}(v)$ (when Victim only switching) from the standpoint of the voltage source of the Victim is expressed as the following expression (19) by using the topology in Fig. 6. The capacitance calculation procedures of the other steps are similar.

$$C_{total}(v) = C_v + \left(\frac{C_{a1}C_{c1}}{C_{a1} + C_{c1}} \right) + \left(\frac{C_{a2}C_{c2}}{C_{a2} + C_{c2}} \right) \quad (19)$$

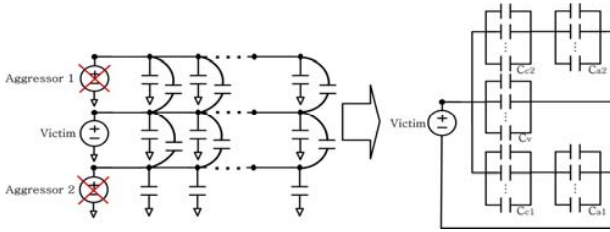


Fig. 6 Circuit Topology to Calculate $C_{total}(v)$ in Multiple Interconnects

B. Average Current Estimation in Multiple Conductors

By applying the superposition principle, the total area of the current waveforms excited at a particular resistor A of the Victim when the Victim and two Aggressors are switched in opposite directions can be approximated by the algebraic sum of the areas of the current waveforms excited at resistor A by the voltage sources of the Victim, Aggressor 1, and Aggressor 2. Therefore, the equation for determining the worst-case average current when the Victim and two Aggressors are switched in opposite directions can be simply represented as shown below.

$$I_{avg} = I_{avg_victim} + I_{avg_aggressor1} + I_{avg_aggressor2} \quad (20)$$

V. EXPERIMENTS AND RESULTS

We have experimented with slightly different characteristics for each interconnect to check the results of our experiment under diverse conditions. For a wide range of interconnect characteristic, samples of per-unit-length resistance and capacitance were chosen based on ITRS 2007 data [11].

For each case, the coupling capacitance was modeled as 2, 4, and 6 times the ground capacitance (ground capacitance is defined as the average of the C_{total} values for the Victim and Aggressor 1 or the Victim and Aggressor 2). In addition, for each case, three different values were used for T_r . More details

on the environment of the experiment are given in Table I and Table II.

TABLE I
EXPERIMENTAL ENVIRONMENT OF MULTIPLE INTERCONNECTS FOR COMPARING CURRENT ESTIMATION ACCURACY (1)

	Role	R_{total}	C_{total}	N	T_r (ns)	$T_c - 1$ (ps)	$T_c - 2$ (ps)	$T_c - 3$ (ps)
Case 1	A1	3.500E+01	1.6000E-15	10	20	25	300	800
	V	1.720E+02	1.5913E-14	10	20	50	400	900
	A2	3.770E+02	9.7778E-15	10	20	100	500	1000
Case 2	A1	5.820E+02	3.6444E-15	10	20	20	300	800
	V	3.500E+02	9.9600E-14	10	20	50	400	900
	A2	1.425E+03	6.8233E-14	10	20	100	500	1000
Case 3	A1	2.500E+03	3.6889E-14	10	20	20	300	800
	V	3.217E+03	1.1000E-13	10	20	50	400	900
	A2	2.433E+03	1.6300E-13	10	20	100	500	1000

TABLE II
EXPERIMENTAL ENVIRONMENT OF MULTIPLE INTERCONNECTS FOR COMPARING CURRENT ESTIMATION ACCURACY (2)

	Role	R_{total}	C_{total}	$C_c(F)$ 2×	$C_c(F)$ 4×	$C_c(F)$ 6×
Case 1	A1	3.500E+01	1.6000E-15	1.7513E-14	3.5026E-14	5.2539E-14
	V	1.720E+02	1.5913E-14	2.5691E-14	5.1382E-14	7.7072E-14
	A2	3.770E+02	9.7778E-15	1.0324E-13	2.0649E-13	3.0973E-13
Case 2	A1	5.820E+02	3.6444E-15	1.6783E-13	3.3567E-13	5.0350E-13
	V	3.500E+02	9.9600E-14	1.4689E-13	2.937E-13	4.4067E-13
	A2	1.425E+03	6.8233E-14	2.7300E-13	5.4600E-13	8.1900E-13
Case 3	A1	2.500E+03	3.6889E-14	2.7300E-13	5.4600E-13	8.1900E-13
	V	3.217E+03	1.1000E-13	2.7300E-13	5.4600E-13	8.1900E-13
	A2	2.433E+03	1.6300E-13	2.7300E-13	5.4600E-13	8.1900E-13

In order to verify the accuracy, each case has been experimented using the proposed technique. We have set HSPICE result as reference standard values and measured the error ratio. Fig. 7 has shown that the average relative error of the average currents for all resistive elements in all cases was found to be approximately 0.674%. This shows the very high degree of accuracy of the proposed technique throughout the entire class of interconnects.

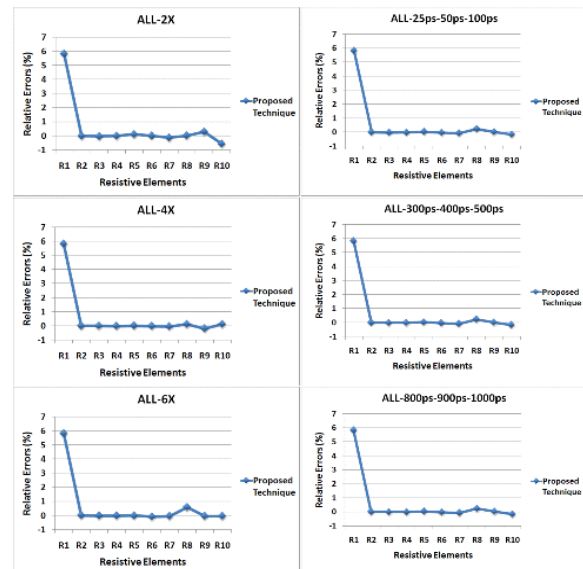


Fig. 7 (a) Relative Errors in Average Current Estimation for Multiple Interconnects: Case I

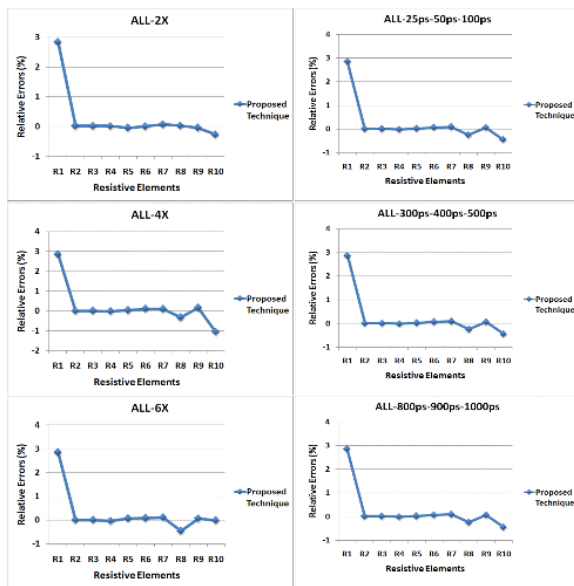


Fig. 7 (b) Relative Errors in Average Current Estimation for Multiple Interconnects: Case II

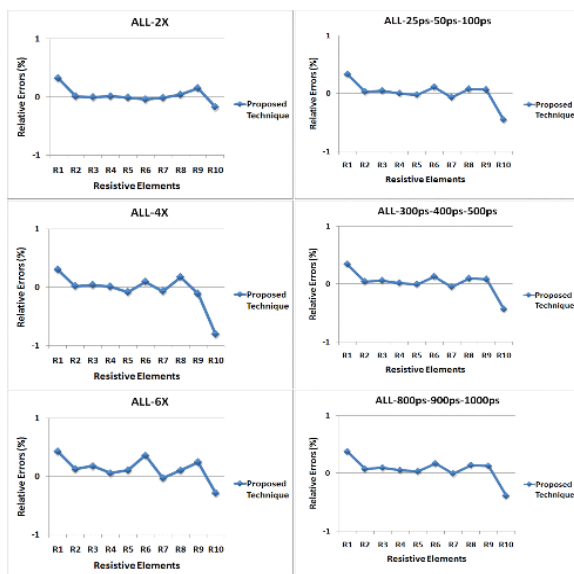


Fig. 7 (c) Relative Errors in Average Current Estimation for Multiple Interconnects: Case III

VI. CONCLUSION

In this paper, we have proposed the technique for worst case average current estimation of multiple interconnects using a closed-form equation. The accuracy of the proposed technique has been validated in terms of a wide range of interconnect characteristics and a realistic interconnect geometry by experiments. The average relative error of the average currents

for all resistive elements in all cases for a wide range of interconnect characteristics has been found to be approximately 0.674%. Also, the average relative error of the average current for all resistive elements in all cases for realistic interconnect geometry has been found to be approximately 0.076%.

ACKNOWLEDGMENT

This work was supported by National Research Foundation of Korea Grant funded by the Korean Government (2009-0074031).

REFERENCES

- [1] P. P. Sotiriadis and A. Chandrakasan, "Reducing bus delay in submicron technology using coding," in *Proc. Asia South Pacific Design Automation Conference*, 2001, pp. 109-114.
- [2] Chunjie Duan, Anup Tirumala and S. P. Khatri, "Analysis and avoidance of cross-talk in on-chip buses," *Hot Interconnects 9*, 2001, pp. 133-138.
- [3] S. R. Sridhara, A. Ahmed and N. R. Shanbhag, "Area and energy-efficient crosstalk avoidance codes for on-chip buses," in *Proc. IEEE International Conference on Computer Design: VLSI in Computers and Processors*, pp. 12-17, 2004.
- [4] B. Victor and K. Keutzer, "Bus encoding to prevent crosstalk delay," in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2001, pp. 57-63.
- [5] Y. S. Shin and T. Sakurai, "Coupling-driven bus design for low-power application-specific systems," in *Proc. ACM/IEEE Design Automation Conference*, 2001, pp. 750-753.
- [6] R. Kumar, "Interconnect and Noise Design for the Pentium 4 Processor," *Intel Technology Journal Q1*, 2001.
- [7] M. Celik, L. Pileggi and A. Odabasioglu, *IC Interconnect Analysis*, Kluwer Academic Publishers, 2002.
- [8] L. T. Pillage and R. A. Rohrer, "Asymptotic Waveform Evaluation for Timing Analysis," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, 1990, pp. 352-366.
- [9] L. T. Pillage, R. A. Rohrer and C. Visweswariah, *Electronic Circuit and System Simulation Methods*, McGraw-Hill, Inc., 1994.
- [10] K. Agarwal and F. Liu, "Efficient Computation of Current Flow in Signal Wires for Reliability Analysis," in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2007, pp. 741-746.
- [11] www.public.itrs.net.

Ki-Young Kim received the B.S., M.S. and Ph.D. degrees in computing science from Soongsil University, Seoul, Korea in 2002 and 2004 and 2009, respectively. He is with Samsung LED in present. His research interests include circuit analysis and design automation and digital systems engineering.

Jae-Ho Lim received the B.S. degree in depart of computing from Soongsil University, Seoul, Korea in 2009.

His research interests include circuit analysis and simulation for high performance computer systems, signal integrity, design automation and digital systems engineering.

Deok-Min Kim received the B.S. degree in depart of computing from Suwon University, Suwon, Korea, in 2008.

His research interests include circuit analysis and simulation for high performance computer systems, design automation and digital systems engineering.

Seok-Yoon Kim (M'93) received the B.S. degree in electrical engineering from Seoul National University, Korea, in 1980 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Texas, Austin, TX, in 1990 and 1993. From 1982 to 1987 he was with the Electronics and Telecommunications Research Institute, Daejeon, Korea. From 1993 to 1995 he was with the Semiconductor Systems Design Technology group of Motorola Inc. where he developed and enhanced the modeling and simulation capabilities of the corporation's circuit simulator, MCSPIICE, for packages and interconnects of high-speed IC's. Since March 1995, he has been with the School of Computing, Soongsil University, Seoul, Korea. His research interests include circuit analysis and simulation for high performance computer systems, design automation and digital systems engineering.