International Journal of Electrical, Electronic and Communication Sciences
ISSN: 2517-9438
Vol:10, No:2, 2016

An Accurate, Wide Dynamic Range Current Mirror Structure

Hassan Faraji Baghtash

***Abstract*—**In this paper, a low voltage high performance current mirror is presented. Its most important specifications, which are improved in this work, are analyzed and formulated proving that it has such outstanding merits as: Very low input resistance of 26mΩ, very wide current dynamic range of 8 decades from 10pA to 1mA (160dB) together with an extremely low current copy error of less than 0.6ppm, and very low input and output voltages. Furthermore, the proposed current mirror bandwidth is 944MHz utilizing very low power consumption (267μW) and transistors count. HSPICE simulation results are performed using TSMC 0.18μm CMOS technology utilizing 1.8V single power supply, confirming the theoretically proved outstanding performance of the proposed current mirror. Monte Carlo simulation of its most important parameter is also examined showing its sufficiently resistance against technology process variations.

***Keywords*—**Current mirror/source, high accuracy, low voltage, wide dynamic range.

I. Introduction

TECHNOLOGY down scaling introduces great advantages in the performance of both digital and analog integrated circuits. It is well-known that shrinking transistor feature size increases intrinsic speed of devices and lowers both the supply voltage and the power consumption. Furthermore, low power circuit design is greatly demanded for portable systems. However, lowering power supply imposes added constraints upon circuit design including the current mirrors which are among the most important and widely used building blocks in VLSI designs. They are aimed to exhibit low input and high output resistance, high gain accuracy, large current dynamic range, high input and output compliances, and high bandwidth. Decreasing power supply imposes some limits on these characteristics especially the accuracy and the dynamic range. Hence many researches can be found dealing with improving the problems of low voltage current mirrors [1]-[4]. Also some low voltage design techniques such as using body driven, multi floating gate transistors, sub threshold, and self cascode schemes are introduced in literatures [5]. The common widely used low voltage current mirror is the well-known low voltage (high swing) cascode (LVC) current mirror shown in Fig. 1 (a). It has rather low input and output voltage, moderately low input and high output resistance, and high accuracy. The modified version of this current mirror which provides lower input impedance and lower input voltage is shown in Fig. 1 (b), in which the input current is applied to the drain of mirror transistor M1. However, this modification degrades both accuracy and current dynamic range, and introduces some offset current to the circuit. The offset current can be removed by removing bias current from output or drain of M1 [6], but the accuracy and dynamic range problems still exist. This is due to the fact that there is a difference between drain source voltages of M1 and M2 resulted from the difference between currents of cascode transistors M1C and M2C. This problem can be reduced using regulated cascode version of the circuit (see Fig. 1 (c)) which employs an amplifier to compare drain – source voltages of mirror transistors and use to improve the current copying accuracy. In [7], [8], the comparative study of LVC current mirrors are given where in [7] are compared those possible LVC implementations in which amplifiers are not included. Then in [8] are compared those LVC structures which include amplifiers, hence, exhibit better performances. There are, however, some high performance amplifiers used in the mentioned current mirror [9], [10] providing very low input impedances of 0.012 and 0.01 ohm, low current copy errors of 0.05% and 0.1%, and very high output resistance of 2.3GΩ and 8 GΩ respectively. But these circuits suffer from higher power consumption (as are mentioned in Section III), and offset currents (due to FVF scheme). Furthermore, in these circuits the feedback loop contains a very high impedance node which degrades input impedance frequency response. Moreover, the circuit proposed in [10] uses floating gate transistors in its feedback loop which has its limits and needs expensive technology to be implemented. On the other hand, the well-known conventional method to achieve wider current dynamic ranges is using adaptive bias scheme as is used by [11], [12] which although helps the current mirror to preserve a better current copying accuracy in the provided wide current dynamic range. However, the current accuracy is not sufficiently improved. Nevertheless, these latter circuits cannot achieve good values for such parameters as input resistance and bandwidth. Furthermore, in most cases adaptive bias scheme needs extra power consumption and results circuit complexity. In addition, current copying error of all these schemes is still high (about 0.05%) and is inadequate for those high performance applications which need low current copying errors. Therefore, in this work, a very high performance current mirror is designed which combines all merits of; extremely low current copy error, low input and output voltage, very low input resistance, high output resistance, ultra-wide current dynamic range, relatively low power consumption and large bandwidth.

Hassan Faraji Baghtash is with Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran (phone: (+98)41-3345-9340; fax: (+98)41-3345-9340; e-mail: hfaraji@sut.ac.ir).

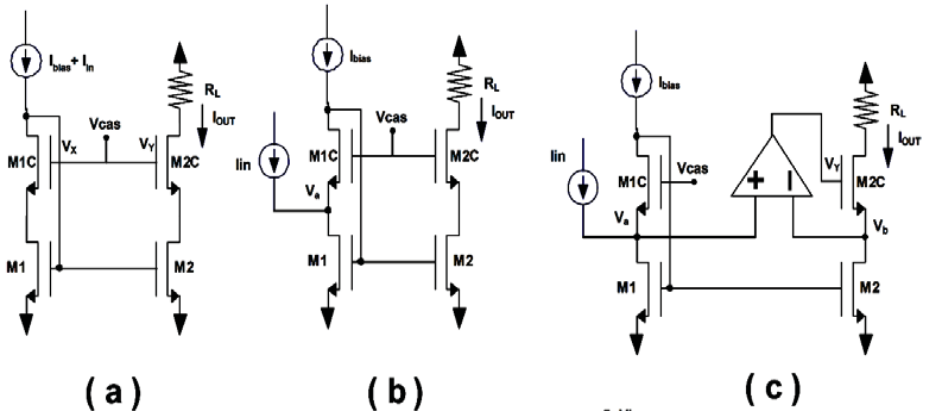

Fig. 1 Low voltage cascode current mirror (a) regular cascode (b) modified low voltage version (c) regulated cascode version

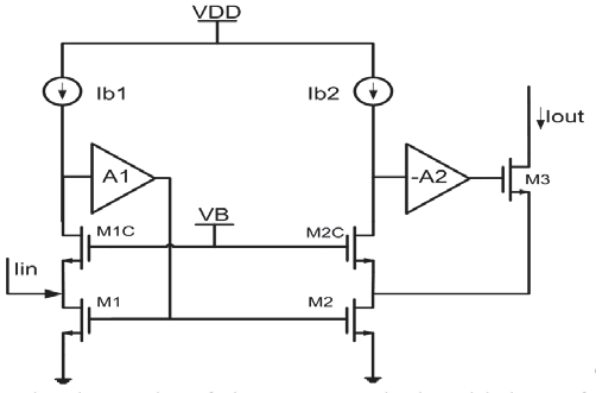

Fig. 2 Conceptual schematic of the proposed ultra-high performance current mirror

II. Principal of Operation

The conceptual schematic of the proposed high performance current mirror is shown in Fig. 2 where transistors M1-M2 and M1C-M2C form a low voltage cascode (LVC) current mirror. Bias currents of Ib1 and Ib2 are applied to the drain of M1C and M2C respectively. Input current is applied to the drain of M1 and output current is taken from the drain of M3 which its source is connected to the drain of M2. This arrangement provides very low voltages for input and output nodes. The gate of M3 is controlled by the feedback loop composed of M3, M2C, and amplifier "-A2". This feedback causes a very high output impedance due to its very high loop gain. On the contrary, at the input side, the feedback loop composed of transistors M1, M1C, and amplifier "A1" is so arranged that introduces a very low input impedance. The gate voltage of cascode transistors, M1C and M2C, is driven by the constant bias voltage of VB. This configuration has some advantages over such well known structures as low voltage regulated cascode and adaptive bias schemes as follow:

1) The gate of both cascode transistors is connected to the same voltage of VB. On the other hand, bias currents of Ib1 and Ib2 have the same value. These two conditions together set the drain-source voltages of M1 and M2 to be equal. Furthermore, using amplifiers "A1" and "-A2" equals the drains voltages of transistors M1C and M2C, too, which leads to further equality of drain voltages of M1 and M2 and significantly reduces the current copying error.
2) Any variation of input voltage due to input current, is amplified by the order of feedback loop gain and is applied to the gate of transistors M1 and M2 granting some outstanding merits as: a) very low input resistance. b) Drain voltage variation of M1C is A times smaller than variation of gate voltages of M1 and M2 which firstly certifies the equality of voltages of the drains of M1C and M2C, and secondly allows gate voltages of M1 and M2 to have rail to rail variation, resulted in an ultra-wide current dynamic range (about 8 decade from 10pA up to 1mA as is specified in Section III) and an ultra-low current coping error. On the contrary, in regulated cascode version, the gates of M1 and M2 are connected to drain of M1C making it to receive much more voltage variations to be handled with acceptable linearity. Moreover, gates voltages of M1 and M2 cannot have rail to rail range, the value which disturbs matching state of M1 and M2 and degrades gain accuracy and current dynamic range.
3) In this configuration each feedback loop consists only one high impedance node resulting a very wide bandwidth for the block.

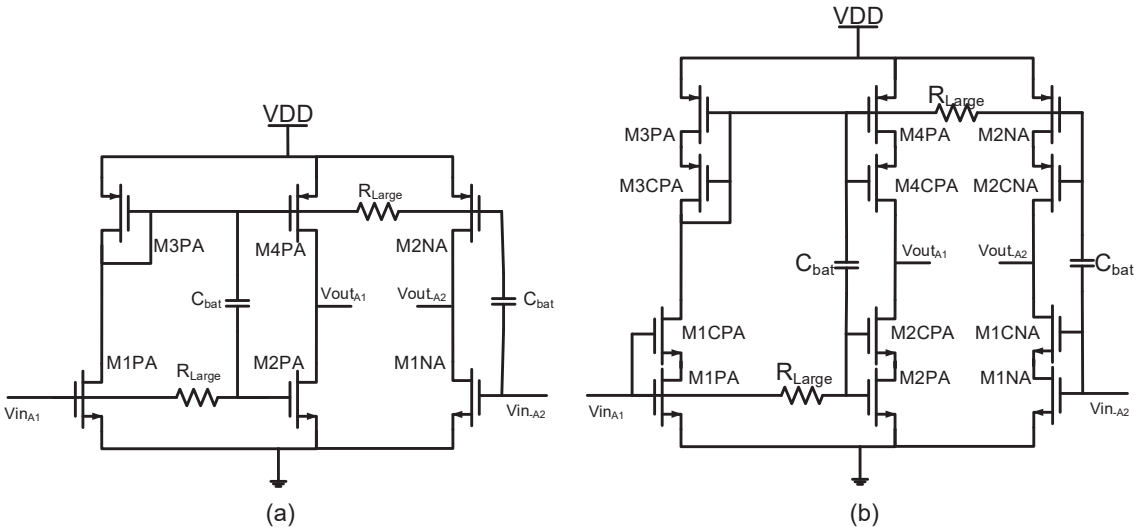

Fig. 3 Transistor level implementation of the proposed amplifier (a) simple version (b) self-cascode version

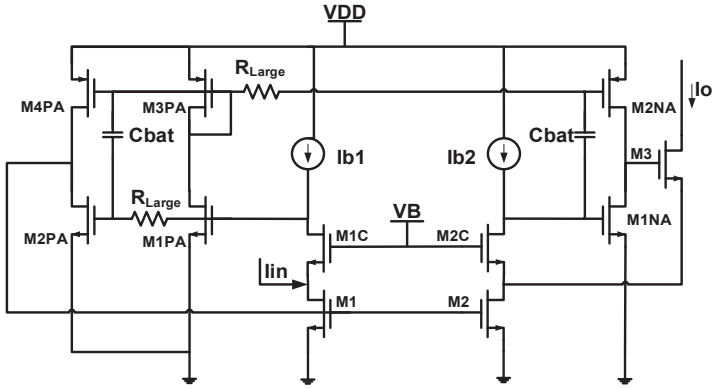

Fig. 4 Proposed current mirror employing simple amplifier

Amplifiers "A1" and "-A2" must be carefully designed to satisfy -1) Drain – source voltage equality of M1C and M2C, -2) Output of "-A2" must be float to allow M3 to so set its gate voltage to obtain a very accurate copy of input current.

Fig. 3 shows two transistor level implementations of these amplifiers. In Fig. 3 (a), transistors M1PA – M4PA configure amplifier "A1" and transistors M1NA-M2NA configure amplifier "- A2". Resistors of R_{Large} are used to adaptively bias M2PA and M2NA. Resistors of R_{Large} can be simply implemented using a transistor operating in its cutoff region which provides very large resistance in very small chip area. Using this adaptive bias scheme causes all transistors of amplifiers to have the same currents and eliminates the requirement of other biasing networks which need critical design and lead to more power consumption. On the other hand, using capacitors of C_{bat} duplicate the gain of both amplifiers. Having the same currents causes M1PA and M1NA to have the same gate - source voltages which provide equal voltages at the drains of M1C and M2C. Fig. 3 (b) shows the self cascode version of Fig. 3 (a). Since a self-cascode amplifier provides a higher gain than the simple one thus it improves such current mirror parameters as input and output resistance, and accuracy. However, it degrades the frequency response due to increasing the nodes' impedance. Fig. 4 shows transistor level implementation of the proposed current mirror

A. Small Signal Analysis

1. Low Frequency Analysis

Considering Fig. 4 and for operating frequencies of $f > 1/(2\pi R_{Large} C_{bat})$ the small signal transfer function of amplifiers "A1" and "-A2" is given by (1) and (2), respectively:

$$AV_{A1} = \frac{V_{outA1}}{V_{inA1}} = \frac{g_{m2PA}(g_{m2PA} + g_{m4PA})}{g_{m3PA}(g_{ds2PA} + g_{ds4PA})} \quad (1)$$

$$AV_{-A2} = \frac{V_{outNA}}{V_{in-A2}} = -\frac{g_{m1NA} + g_{m2NA}}{g_{ds1NA} + g_{ds2NA}} \quad (2)$$

Now using KCL in input node gives:

$$I_{in} = g_{ds1}V_{in} + g_{m1}V_{g1} \tag{3}$$

where

$$V_{g1} = AV_{A1}\left(1+\frac{g_{m1c}}{g_{ds1c}}\right)V_{in} \tag{4}$$

Substituting AV_{A1} from (1) into (3) we get:

$$R_{in} = \frac{g_{m3PA}g_{ds1c}\left(g_{ds2PA}+g_{ds4PA}\right)}{g_{m1}g_{m1c}g_{m2PA}\left(g_{m2PA}+g_{m4PA}\right)} = \frac{g_{ds1c}}{g_{m1}g_{m1c}AV_{A1}} \tag{5}$$

Relation (5) shows that the input resistance of the proposed circuit is inversely proportional to the gain of amplifier "A1" thus the input resistance can be decreased by increasing the gain of amplifier "A1". This resistance also can be reduced setting suitably the parameters of g_{m1}, g_{m1c}, and g_{ds1c}.

The same analysis can be done in the output node of circuit witch gives the output resistance of R_{out} as:

$$R_{out} = \frac{g_{m3}g_{m2c}\left(g_{m1NA}+g_{m2NA}\right)}{g_{ds1}g_{ds2c}g_{ds3}\left(g_{ds1NA}+g_{ds2NA}\right)} = \frac{g_{m3}g_{m2c}AV_{-A2}}{g_{ds1}g_{ds2c}g_{ds3}} \tag{6}$$

Relation (6) shows that the output resistance of the proposed current mirror is proportional to the gain of amplifier "-A2". Any increment in gain of amplifier "-A2" helps current mirror to achieve higher output resistance. The same argument applies for the self-cascode version (if implemented), whose R_{out} is greater than that of simple version (at least) by a Factor of ($g_{m1,2c\,NA}/g_{ds1,2cNA}$).

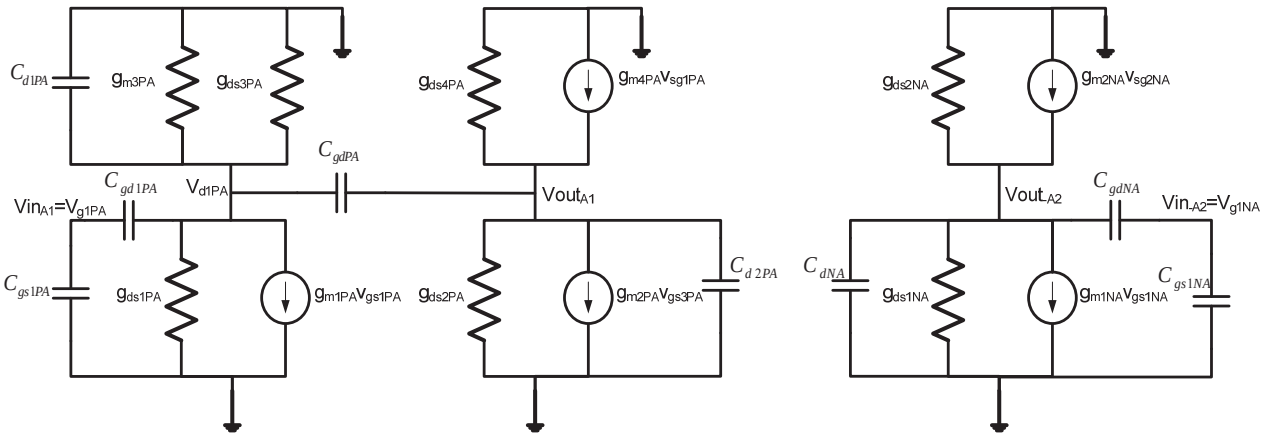

Fig. 5 High frequency equivalent circuit for the proposed simple amplifier

2. High Frequency Analysis

The high frequency equivalent circuit of Fig. 4 is shown in Fig. 5. Referring to this circuit and performing some circuit analysis and simplifications, one can get the frequency response of current transfer function as:

$$m = \frac{I_{out}}{I_{in}} = \frac{g_{m2}\left(1+\frac{1}{z_1}s\right)\left(1+\frac{1}{z_2}s^2\right)}{g_{m1}\left(1+\frac{1}{p_1}s^2\right)\left(1+\frac{1}{p_2}s^2\right)} \tag{7}$$

where

$$\frac{1}{z_1} = \frac{C_{ds1c}}{g_{m1c}},$$
$$\frac{1}{z_2} = \frac{C_{gdNA}C'_{dNA}}{g_{m2c}\left(g_{ds1NA}+g_{ds2NA}\right)}$$
$$\frac{1}{p_1} = -\frac{C_{gdNA}C_{gs3}AV_{-A2}}{g_{m3}g_{ds2c}}$$
$$\frac{1}{p_2} = \frac{C_{gd1}C'_{d2PA}}{g_{m1}\left(g_{ds2PA}+g_{ds4PA}\right)} \tag{8}$$

Relation (7) shows that if frequency of Zero is smaller than that of Poles, the response will have overshoot otherwise the frequency response will not have overshoot but this time the frequency bandwidth will be smaller than the previous case. This goal can be achieved by either adjusting the parameters given in (8) or using compensation scheme.

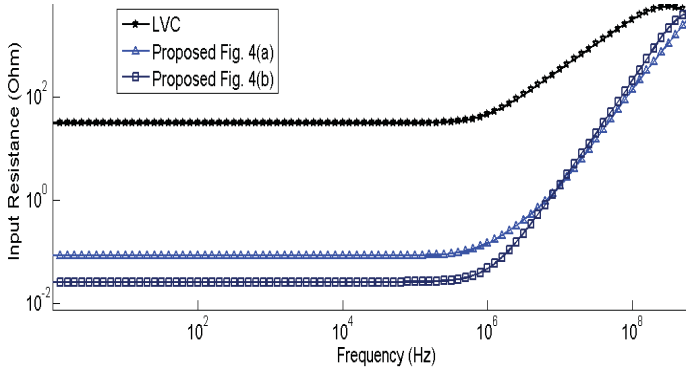

Fig. 6 Input resistance frequency response for proposed current mirror

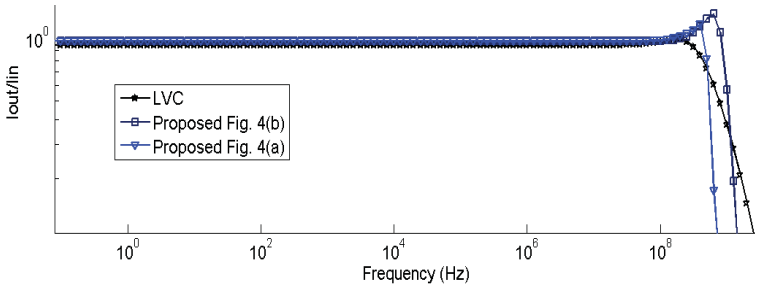

Fig. 7 Frequency response of the proposed current mirror

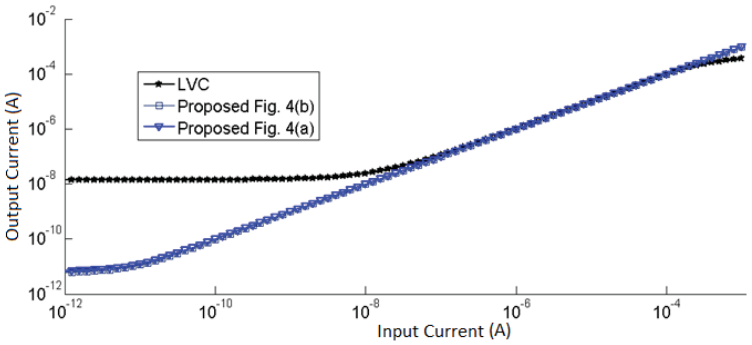

Fig. 8 DC current transfer curve Iout vs Iin

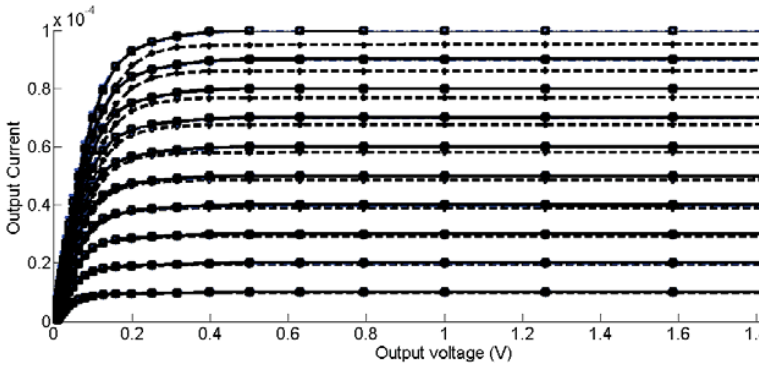

Fig. 9 Output current versus output voltage for sweeping input current from 10uA to 100uA in 10uA steps. *) LVC. ▼) Proposed Fig. 4. □) Proposed self-cascode version

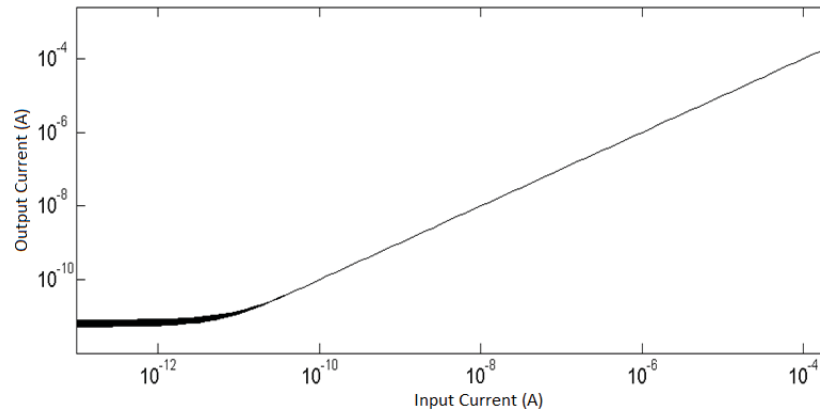

Fig. 10 Monte Carlo analysis performed on current transfer curve of the self-cascode version of proposed circuit

TABLE I
COMPARATIVE PARAMETERS OF THE PROPOSED CURRENT MIRROR WITH OTHER RECENT WORKS

Reference	[7]	[8]	[9]	[10]	[11]	[12]	This work	
							Fig. 4	Self-cascode version
Rin (Ω)	27	33	0.012	0.01	NA	NA	0.085	0.026
P (μW)	341	218	NA	NA	NA	NA	264	267
BW (MHz)	907	185	220 at I_{bias} = 50μA & I_{in}=100 μA	200	0.1	60	944	522
Vdd (V)	1	1.5	1.8	3	1.8	1.8	1.8	1.8
Vin (V)	NA	NA	NA	NA	NA	NA	0.4	0.4
Vout (V)	NA	NA	0.46	0.15	NA	NA	0.3@ Iin=30μA	0.3@ Iin=30μA
Dynamic range (dB)	NA	56.9	NA	NA	NA	NA	160	160
Offset	NA	830nA	NA	NA	NA	NA	7pA	7pA
Current transfer error (%)	0.5	2.5	0.05	0.1	0.05	NA	0.0006	0.00006
Ibias (μA)	50	50	10	25	NA	50	1	2
Technology (CMOS)	TSMC 0.18μm	TSMC 0.18μm	AMI 0.5μm	AMI 0.5 μm	TSMC 0.18μm	0.5 μm	TSMC 0.18μm	TSMC 0.18μm

III. SIMULATION RESULTS

HSPICE simulations were carried out using TSMC 0.18μm CMOS technology utilizing single 1.8 V power supply. The aspect ratios of the transistors for all structures; LVC (if used), proposed (a) and proposed (b) are as: M1PA - M4PA, M1NA - M2NA=0.9/0.54, M1CPAM4CPA, M1CNA - M2CNA=3.6/0.54, M1 - M2=9/0.54, M1C – M2C=19.8/0.54, M3=18/0.18 (Fig. 4), and M3=18/0.36 (self-cascode version).

For implementing of R_{Large} a transistor with aspect ratio of 0.36/5.4 is used. C_{bat} is chosen to have a value of 1pF which is small and is not a critical issue in chip area. In Fig. 6, the input impedance frequency responses of both versions of the proposed current mirror are compared with that of the LVC current mirror which present very low input impedance for proposed current mirror (26mΩ for the self-cascode version). It must be noted that, compared to LVC, the input resistance of the proposed circuit is reduced more than 1000 times while preserves the same frequency bandwidth. Moreover, the input resistance of the self-cascode version is smaller than that of the simple one which validates the results noted in sec II. Frequency response of the proposed current mirror is shown in Fig. 7 with -3dB frequency of 944MHz for the current mirror (including the simple amplifier) which is about twice of that of LVC current mirror. This curves prove the results obtained from (7). DC transfer function (I_{out} versus I_{in}) of the proposed current mirror is compared with that of the LVC one in Fig. 8. The curves show very vide current dynamic range of 160dB and favorably very low current transfer error of 0.6ppm for the proposed current mirror. Fig. 9 compares the output current versus the output voltage of the proposed current mirror with those of the well-known LVC current mirror when I_{IN} is swept from 10 μA to 100 μA in 10 μA steps which proves low voltage operation capability of the proposed circuit. The minimum output voltage of the proposed circuit to operate in high impedance mode is about 0.46 V for 100 μA. Monte Carlo analysis is performed to simulate the fabrication and process variation condition with applying 10% mismatch to the β and V_{TH} and is shown in Fig. 10 DC current transfer curve in terms of frequency. The Monte Carlo analysis results prove that the proposed circuit is sufficiently resistant against the process variations. In Table I, the parameters of the proposed circuit are compared with some advanced new current mirrors. It must be noted that also the dear writers of [9], [10] did not mentioned power consumption of this works but it can be estimated from currents and supply voltages that the value of this parameter is at least 288μW and 300 μW for [9] and [10], respectively.

IV. Conclusion

A low voltage high performance current mirror is presented in this work. Its operation is explained in details and its most important parameters which are improved in this work are analyzed and formulated. The proposed current mirror is simulated using TSMC 0.18µm technology while working with single power supply of 1.8V. The HSPICE simulation results confirm the theoretically proved outstanding performance of the proposed current mirror as: ultra-wide current dynamic range and extremely small current mirroring error. It also presents very low input resistance, very low input voltage and very low output voltage. Furthermore, the proposed current mirror can operate in very high frequencies consuming very low power.

References

[1] S. J. Azhari, H. Faraji Baghtash, K. Monfaredi, "A Novel Ultra High Compliance, High Output Impedance Low Power Very Accurate High Performance Current Mirror," *Microelectronics journal*, Vol. 42, pp. 432-439, 2011.

[2] S.S. Rajput and S.S. Jamuar, "A Current Mirror for Low Voltage, High Performance Analog Circuits," *Analog Integrated circuits and signal processing Kluwer Academic Publishers*, pp. 221-233, 2003.

[3] S. Sharma, S. S. Rajput, L. K. Mangotra, and S. S. Jamuar, "FGMOS Current Mirror: Behaviour and Bandwidth Enhancement," *Analog Integrated Circuits and Signal Processing, Springer Science*, pp. 281-286, 2006.

[4] SS Rajput, Jamuar, S.S, "Advanced Current Mirrors for Low Voltage Analog Designs," *Semiconductor Electronics, ICSE 2004. IEEE International Conference on*, pp. 258-263, 2004.

[5] S. Rajput and S. S. Jamuar, "Low Voltage Analog Circuit Design Techniques," *Circuits and Systems Magazine, IEEE,* vol. 2, no. 1, pp. 24-42, 2002.

[6] J. Ramírez-Angulo, R. G. Carvajal, and A. Torralba, "Low Supply Voltage High- Performance CMOS Current Mirror with Low Input and Output Voltage Requirements," *IEEE Transactions on Circuits and Systems—II: express briefs,* vol. 51, no. 3, pp. 124-129, Mar. 2004.

[7] Costas Koliopoulos, Costas Psychalinos, "A Comparative Study of the Performance of the Flipped Voltage Follower Based Low-Voltage Current Mirrors," *Signals, Circuits and Systems. ISSCS,* vol. 1, pp. 1-4, 2007.

[8] Houda Bdiri Gabbouj, Nejib Hassen, and Kamel Bsebes, "Comparative study and design of new low voltage high performance current mirrors" *Design and Technology of Integrated Systems in Nanoscale Era, 3rd International Conference on IEEE*, pp.1 – 6, 2008

[9] Milind Subhash Sawant, Jaime Ramírez-Angulo, Antonio. J. López-Martín and Ramon G. Carvajal, "New Compact Implementation of a very High Performance CMOS Current Mirror," *Circuits and Systems, 48th Midwest Symposium on IEEE*, vol. 1, pp. 840-842, 2005.

[10] A. Garimella, L. Garimella, J. Ramirez-Angulo, A.J. Lopez-Martin and R.G. Carvajal, "Low-voltage high performance compact all cascode CMOS current mirror," *Electronics Letters*, vol. 41, no. 25, pp. 1359-1360, 2005.

[11] Laura Sanchez-Gonzalez, Gladys Ducoudray-Acevedo, "High Accuracy Self-Biasing Cascode Current Mirror," *Circuits and Systems, MWSCAS '06. 49th IEEE International Midwest Symposium on*, vol. 1, pp. 465-468, 2006.

[12] Jaime Ramirez-Angulo, Milind S. Sawant, Ramon G. Carvajal, and Antonio J. Lopez- Martin, "New Compact and Power Efficient Dynamically Biased Cascode Mirrors and Telescopic Op-amps," *ISCAS*, 2006, pp. 2833-2836.

Hassan Faraji Baghtash was born in Miyandoab, Iran, in 1985. He received the B.Sc. degree from Urmia University in 2007, and M.Sc. and Ph.D. degrees both from Iran University of Science and Technology (IUST), Tehran, Iran in 2009, and 2014 in respectively, all in electronics engineering.

He was with IUST Electronic Research Center Group, from 2007 to 2010 as a Researcher, and Science and Research Branch, Islamic Azad University from 2011 to 2015, as a Fellow Lecturer. He joined Sahand University of Technology, Tabriz, Iran as an Assistant Professor in 2015. He is the author or coauthor of more than 25 national and international papers and also collaborated in several research projects and has a registered Iranian patent. Dr. Faraji Baghtash was selected as distinguished researcher of the IUST in 2011. His current research interests include current mode/voltage mode analog integrated circuit design, low voltage, low power circuit and systems, analog microelectronics and Digital System design.