A Very High Speed, High Resolution Current Comparator Design

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Abstract—This paper presents an idea for analog current comparison which compares input signal and reference currents with high speed and accuracy. Proposed circuit utilizes amplification properties of common gate configuration, where voltage variations of input current are amplified and a compared output voltage is developed. Cascaded inverter stages are used to generate final CMOS compatible output voltage. Power consumption of circuit can be controlled by the applied gate bias voltage. The comparator is designed and studied at 180nm CMOS process technology for a supply voltage of 3V.

Keywords—Current Mode, Comparator, High Resolution, High Speed.

I. INTRODUCTION

THE information carried by any electric network is represented by Nodal voltages and branch currents, former referred to "voltage domain circuits" whereas the latter are known as "current domain circuits".

Current mode circuits are becoming designer's interests now a day, as they offer many unique and attractive properties over their voltage mode complements. This includes higher speed, higher bandwidth, reduced distortion, low supply voltage requirements and lesser sensitivity to switching noise [4].

Several current comparators are proposed in recent years [5]-[15]. The first CMOS continuous time current comparator was proposed in [5], which consists of two cascode current mirrors. The drawback of this design was in terms of speed and bandwidth. A new design has been proposed [7] which uses inverter stage in feedback with source-follower stage. But the circuit shows dead band region for low values of input currents, where input impedance is quite high and thus limiting speed of operation.

Voltage-current feedback concept is used for comparison of currents [11]-[14], where a resistive feedback is applied to a voltage amplifier, which results in impedances reduction thus improvement speed performance. Current mirror concept again used in [15]; where it uses improved Wilson current mirror for current comparison, but circuit suffers from high power consumption and higher delay introduced by gain circuitry.
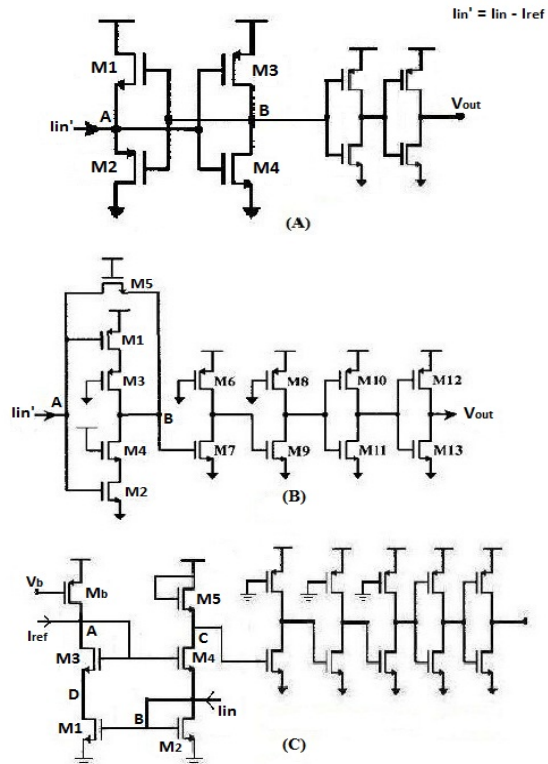

Fig. 1 Existing Current Comparators (A) H. Traff's [7] (B) L. Chen's [14] (C) V. Kasemsuwan's [15]

II. CIRCUIT DESCRIPTION

As we think of "CASCODE" topology, it is a cascade of two Common Source (CS) and Common Gate (CG) stages, providing many useful properties.

Fig. 2 shows the basic cascode configuration: where "M1" generates a small signal drain current proportional to applied voltage "Vin" and "M2" simply routes the current to "R_D". We call "M1" the input device and "M2" the cascode device [1]-[3]. Here we see that a diode connected input device "M1" will allow current input at its drain terminal, it forms the basis of this proposed idea (Fig. 3).

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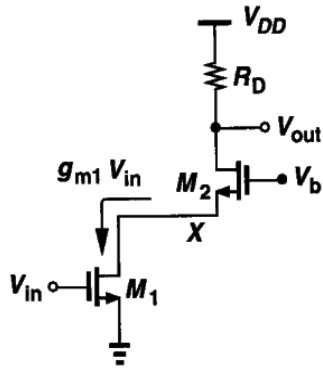
Fig. 2 A Cascode Stage [3]

Gate drain connected "M1" will give a small signal input impedance to input current as well as turns circuit in Common gate configuration; where voltage variation caused by input current at drain of "M1" works as input signal to common gate configured transistor "M2" which in turn produce amplified voltage output across "R_D".
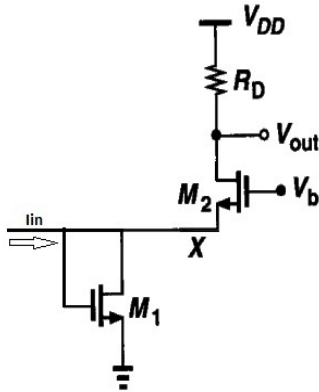

Fig. 3 Current Input to Cascode Stage

Under proper biasing conditions, we can use this circuit as a current comparator when difference of input signal & reference currents (I_{in} - I_{ref}) is applied to diode connected "M1"and the corresponding voltage output is taken across a resistive load.
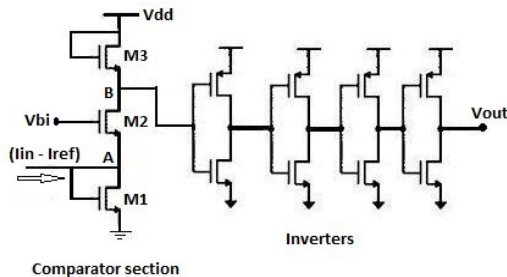

Comparator section

Fig. 4 Proposed Common Gate Current Comparator

Fig. 4 shows proposed current comparator, "M1-M2" are connected in configuration explained above for allowing current input and voltage output. "M3" is a diode connected load for making output impedance small. It uses four Inverters in additional gain circuitry to get rail to rail CMOS compatible voltage output. "V_{bi}" is the biasing voltage which is chosen so that M2 stays in "saturation" at the time of zero current.

Working: When I_{in}>I_{ref} means (**I_{in} – I_{ref}**) is positive, it increases the voltage at node "A" (V_A). As gate of "M2" biased with a constant voltage, Increase in V_A reduces the gate-source voltage of M2. This turns M2 in more saturation and its CG configuration give rise to voltage at node B. This voltage after Gain stages produce a CMOS compatible "HIGH" output. Further increase of current will continuously start decreasing of gate to source voltage of transistor M2. At the time when V_{gs2}<V_{tn} ; M2 will turn "OFF" and so the high output voltage level at node B.

On the other side When I_{in}<I_{ref} means (**I_{in} – I_{ref}**) is negative, it decreases the voltage at node "A" (V_A) and thus turns M2 in "triode" which results in decrease of voltage at node B (as voltage at node B will start following voltage at node A). This voltage after Gain stages produce a CMOS compatible "LOW" output.

By small signal analysis we can easily see:

$$V_B = \cfrac{1}{\left[g_{m3} + g_{m1}\left(\cfrac{1 + g_{m3}r_{o2}}{1 + g_{m2}r_{o2}} \right) \right]}\left(I_{in} - I_{ref} \right)$$

Considering "$g_m r_o \gg 1$"
We get,

$$V_B = \cfrac{1}{\left[g_{m3}\left(1 + \cfrac{g_{m1}}{g_{m2}} \right) \right]}\left(I_{in} - I_{ref} \right)$$

If all the "g_m's" are equal then,

$$\frac{V_B}{\left(I_{in} - I_{ref} \right)} = \frac{1}{2g_m}$$

III. SIMULATION RESULTS

For simulation, standard BSIM 0.18μm CMOS technology parameters have been used with 3V power supply. Circuit was designed optimally for values of speed, power and accuracy. DC transfer characteristics obtained for simulated design is shown in Fig. 5.
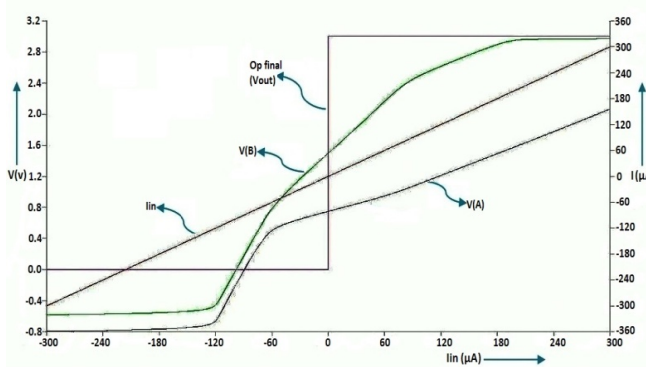
Fig. 5 DC Transfer Characteristics

Delays produced by circuit $\pm 1\,\mu A$ & $\pm 100\,\mu A$ current steps are shown in Table I; at the DC power dissipation of 1.4mW (where for flexibility we have chosen $V_{bi} = V_{DD}/2$).

TABLE I
TRANSIENT RESPONSE: COMMON GATE COMPARATOR

All delays in (ns)	+/- 1µA	+/- 100µA
Rise delay (Comparator stage)	0.1ns	0.1ns
Rise delay (Gain stages)	0.6ns	0.1ns
Total rise delay	0.7ns	0.2ns
Fall delay (Comparator stage)	0.1ns	0.1ns
Fall delay (Gain stages)	0.6ns	0.1ns
Total fall delay	0.7ns	0.2ns
Total Average Delay	**0.7ns**	**0.2ns**

To compare the performance of proposed comparator with those of Traff's [7], R. Del's [11], L. Chen's [14] and V. Kasemsuwan's [15], LTSPICE simulations of all comparators are performed using standard BSIM 0.18µm CMOS technology parameters for optimized values of speed, power and accuracy. Transistor dimensions for proposed comparator designs are as:

TABLE II
DESIGN PARAMETERS: COMMON GATE COMPARATOR

	W (Width)	L (Length)
M1, M2	0.36µm	0.18µm
M3	0.18µm	0.72µm
Inverter: PMOS	0.54µm	0.18µm
Inverter: NMOS	0.18µm	0.18µm

Transient response for all five comparators are simulated for input square-wave currents with amplitudes of $\pm 1\,\mu A$ & $\pm 100\,\mu A$. Figs. 6 & 7 show the comparison of average delay times, it can be seen that proposed design works faster for low as well as high input current values.
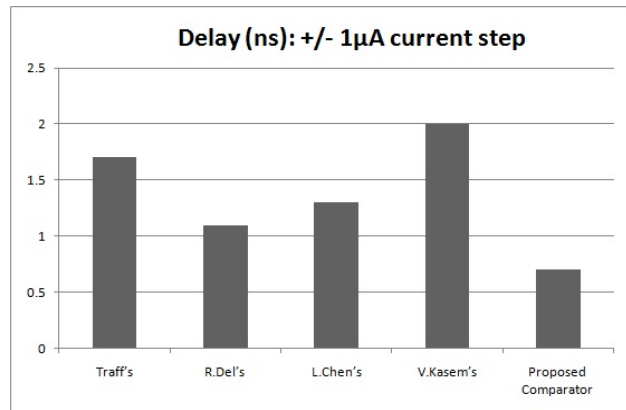
Fig. 6 Average Delay (ns): Response to +/- 1µA Current Step

The DC power consumption of proposed design is little higher from that of Traff's [7] and is comparable to that of others. But in Traff's design lower power consumption is achieved with the expense of large average delay for small input current values, also it offers initial dead band region to such current values whereas proposed comparator shows high accuracy (innA range).
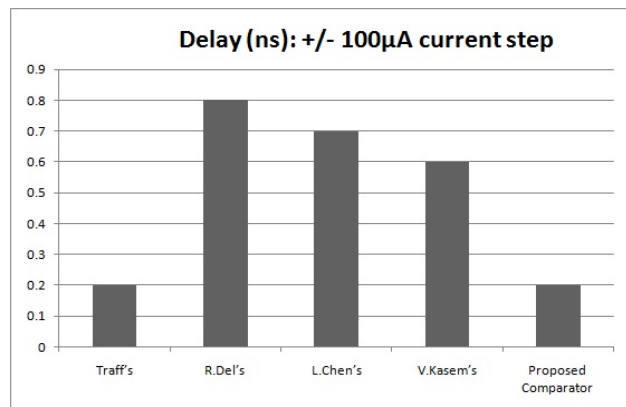
Fig. 7 Average Delay (ns): Response to +/- 100µA Current Step

IV. CONCLUSION

A high speed & high resolution continuous time CMOS current comparator is proposed whose power consumption is comparable to existing current comparators. In addition proposed design has less area, simple structure, low input & output impedances and low operational complexities. The simulation results shows propagation delay of 0.7ns & 0.2ns to $\pm 1\,\mu A$ & $\pm 100\,\mu A$, DC power dissipation of 1.4mW and resolution less than 50nA. The overall performance is better than most of the comparators nearly in terms of all design constraints and it should be useful in many digital and analog circuit applications.

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