International Journal of Information, Control and Computer Sciences
ISSN: 2517-9942
Vol:9, No:3, 2015

A Survey of Baseband Architecture for Software Defined Radio

M. A. Fodha, H. Benfradj, A. Ghazel

***Abstract*—**This paper is a survey of recent works that proposes a baseband processor architecture for software defined radio. A classification of different approaches is proposed. The performance of each architecture is also discussed in order to clarify the suitable approaches that meet software-defined radio constraints.

***Keywords*—**Multi-core architectures, reconfigurable architecture, software defined radio.

I. Introduction

THE origin of software radio idea comes from J. Mitola and it is discussed in [1]. The concept is to implement the radio functionalities at software level. The first aim of radio was the transmission of speech, then this has been enhanced by data transmission and today researches focus to increase the throughput. In this context many baseband processor architectures were proposed to meet the right SDR performance regarding the flexibility to support in the same platform different existing radio standards such as 802.11, GSM, CDMA but recently LTE, LTE-Advanced and WiMAX.

This paper gives an overview and a classification of recent researches that propose processor architecture for baseband processing. So it is a complementary and updated work for existing survey [2]-[4]. This paper gives four classification architectures proposal:

- Single core architectures.
- Homogeneous multi-core architectures.
- Heterogeneous multi-core architectures.
- Reconfigurable architectures.

The section six presents an interesting works done for memory access and scheduling optimization. In addition to these sections the paper adds a dedicated discussion section which focus on the comparison between different approaches in term of throughput, power consumption, occupied area, supported standards. Finally the paper ends with a conclusion section.

II. Single Core Architectures

Only single core architecture is not suitable to implement a baseband processing of an SDR standard due to its low performance. But there are some work deals with single core optimized for a specific functionality such as filtering, FFT processing, modulation, data coding. Even though FUJITSU has proposed a single core processor that meet full signal processing of LTE. After his reconfigurable single chip baseband signal processor [5] FUJITSU has proposed in [6] a recent single core vector processor. The architecture is composed of LX3 CPU processor of Cadence Design Systems unit and vector unit. The processor is evaluated for FFT, sum of tow arrays, FIR filter, computation of inner product and maximum value index search operations and the results show that larger improvement can be achieved with a higher array size. The peak computational performance is 12 GOPS. The power consumption can be reduced to about 30 mW on average with 28 nm process.

A dedicated processor for FFT calculation is designed in [7] to meet the requirement of FFT computation for different wireless standards. The FFT processor is composed of butterfly unit, data memory, twiddle factor memory, interconnect, address generation unit and a control unit. In the processor, two butterfly units are used to compute two outputs per clock cycle. The computation time of FFT processor which run at 200MHz range from 0.31µs and 56.88 µs for 16 N-point and 2048 N-point respectively. Regarding power consumption it has an average of 420 mW.

III. Homogeneous Multicore Architectures

This section presents research work that adopts homogeneous core architecture using well known processors such as General Purpose Processors (GPP), Graphical Processor Unit (GPU) or a dedicated new design.

A. General Purpose Processors

Intel quad core i7-2600K is used in [8] for three optimization methods: optimized algorithm is applied to cyclical redundancy check calculation (CRC), SIMD is used for MIMO detection and Intel integrated Performance Primitives (IPP) library is used for FFT. The optimized algorithm has a speedup of 20.25x but if the table size is too large, the efficiency will degrade. The SIMD has a speedup of 7.01x but sets a limit to the operand, and data rearrangement has to be done sometimes which introduces extra delay. Finally, IPP library has an optimization of FFT algorithm which gives a speedup of 8.92x.

Arm quad core Cortex-A9's NEON technology is experimented in [9]. It is a 128-bit SIMD architecture extension for the ARM Cortex-A9 series processors designed to provide flexible and powerful acceleration. It has 32 registers, 64-bit wide. NEON technology is used to

M. A. Fodha is with the Higher School of Communication of Tunis, El Ghazala Ariana, 2083 Tunisia (e-mail: fodha.mohamed.ali@gmail.com).
H. Benfradj Higher Institute of Computer Science, Raihane Bayrouni Ariana, 2080 Tunisia (e-mail: hanene_bfradj@yahoo.fr)
A. Ghazal is with the Higher School of Communication of Tunis, El Ghazala Ariana, 2083 Tunisia (e-mail: adel.ghazel@supcom.rnu.tn).

demodulate 360 bits data in 64QAM and 320 bits in 16QAM. Results prove that optimized program saves 84% time consumptions than the original one in 16QAM and 77% in 64QAM.

AMD Phenom II X4 955 quad cores processor is used in [10] for three case studies: standard DSP operation, Finite Impulse Response filter and Fast Fourier Transformation. In order to parallelize software code for these operations the application programming interface OpenMP is used by insertion of some directives at appropriate positions in the code. Depending on the frame number and the operation the parallelized version can be faster than the sequential one.

In the same context also for GPP, architectures based on PC using PCI hardware interface are also studied such as Sora platform that propose a radio system called SoftWiFi on Windows [11] and Soft-LTE in a second work [12]. With Intel Core i7 860 2.80GHz processor another research is proposed in [13] but on Xenomai operating system and using also PCI bus associated with DMA for data transfert between the hardware and PC memory. Interrupt-driven model (in contrast to time-sharing operation) is adopted to meet real time requirement. The throughput of PCIe interface is 144.56MByte/s. When the I/Q is quantized in 16 bits, the requirement of LTE 20MHz band width with single antenna configuration is 122.88MByte/s.

B. Graphic Processing Unit

NVIDIA GeForce GTX295 which has 480 CUDA (Compute Unified Device Architecture) cores, can perform 1788 GFLOP is evaluated in [14] for LTE PHY signal processing. It is proved that LTE frame processing at receiver takes 8.58ms after applying sub-blocking method of codeword in order to reduce the total processing time of turbo decoder.

C. Dedicated Baseband Processors

CEA LETI GENEPY platform [15] is based on multiple Smart Memory Engine Processing units interconnected by an asynchronous Network-on-Chip using Network Interfaces associated to a 32-bit MIPS control processor which manages dynamic reconfigurations, real-time scheduling and synchronization. This architecture provides data manipulation at 77 Gbits/s and computing at 3.2 GMAC/s at a 400MHz operating frequency. The platform has been placed and routed in 65 nm CMOS technology. The power consumption of two SMEP is 192.7 mW and the occupied area of one SMEP is 2.392 mm^2. This architecture was applied to 4x2 MIMO LTE processing.

All previous homogeneous multi-core architectures implement only some processing function such as FFT, FIR, MIMO, demodulation but not the whole standard's baseband processing except the NVIDIA GeForce processor [14].

IV. Heterogeneous Multi Core Architectures

In addition to homogeneous architectures discussed previously others researches focus on heterogeneous multi-core approaches which is the subject of this section.

MAGALI processor is illustrated in [16] for LTE standard. The architecture is organized around a 15-router asynchronous NoC that connects 22 processing units from which there are 5 VLIW cores, where each core is capable of 3.2GOPS performance using 50mW, 4 OFDM cores, 4 Data and Configuration Memory cores. The chip layout, implemented in a 65nm CMOS technology occupied an area of 29.6mm^2 has a throughput of 17Gbits/s per link and has power consumption of 477mW. The comparison of MAGALI and GENEPY platform shows that GENEPY has a smaller area for about 14%. The performance speed-up is 3% with a power saving of 18%.

The Tomahawk2 proposed in [17] is a second version of Tomahawk [18]. It is composed of 20 heterogeneous cores, connected by a hierarchical packet-switched star-mesh NoC clocked at 500MHz. The Tensilica 570T RISC core with 16kB data and 16kB instruction caches executes application control code and sends task scheduling requests to the CM (Core Manager) which is based on a Tensilica LX4 core extended with a scheduling-specific instruction set. The power rails are controlled by an adaptive voltage scaling scheme. Duo-PE is also used which is comprised of a vector DSP and a RISC core, connected to a shared local memory. Moreover tow programmable application-specific cores are included: specifically, a sphere detection (SD) core and a multi-mode forward error correction (FEC) core for convolutional, Turbo, and LDPC codes in order to accelerate computationally intensive SDR baseband algorithms. The platform has been placed and routed in 65 nm CMOS technology and provides a throughput of 80Gbits/s per link and supports LTE, WiMAX and 802.11n. The power consumption is 480mW and the occupied area is 36 mm^2.

Stream-access-oriented processor is proposed in [19]. It is composed of three baseband processing modules: SEARCH, MODEM, and CODEC responsible respectively for searching base stations and control of transmission and reception, modulating and demodulating, and coding and decoding. Each baseband module consists of a stream processor cluster (Complex Stream Processor or Bit Stream Processor) and parameterized hardware engines. Data transfer between the baseband modules is achieved via shared memories. An execution controller is used for parallel control of the modules. The architecture supports WLAN, WiMAX, W-CDMA, and LTE.

An updated version of BEAR platform [20] is proposed by The IMEC in [21] containing an ARM control processor, a Digital Front End, two BaseBand Engines (two dimensional VLIW processor which is an optimized instantiation of IMEC's ADRES processor template with 4x4 functional units featuring SIMD instructions), two Outer MoDems (ASIC), two FlexFEC decoding ASIP's, two Timers, level two memory, an interrupt controller and two DMA controllers all connected to a 32-bit segmented AMBA bus with one DMA controller per bus segment. According to this work the IMEC's SDR architecture is able to process 802.11n, LTE and WiMAX. No throughput information is mentioned.

BP-ASP [22] is a Baseband Processing Application Specific Processor based on Open Air Interface Express MIMO

platform [23]. The BP-ASP has several 512-bit SIMD data paths and a 192-bit VLIW instruction word length supporting six instructions dissipation in parallel. Additional functional units are located in the different data paths, including scalar arithmetic/logic unit, scalar memory access unit, vector arithmetic/logic unit, high performance MAC unit, vector shuffle unit, address generation unit, vector memory access unit and scalar/vector exchange unit. BP-ASP is implemented with 130 nm CMOS technology. The layout area 57.8 mm and it has 105 GOPS peak computing performance at 117.6MHz frequency, 120mW for power consumption. The processor runs 2x2 MIMO LTE standards.

X-GOLD SDR20 is introduced in [24]. The processor uses SIMD clusters each one includes 4 SIMD cores, two scalar cores, shared memory, a multi-layer local bus, and a bridge connecting to a global bus. The SIMD clusters are accompanied by a set of configurable hardware accelerators for filtering operations, ciphering, and channel encoding/decoding. Each accelerator is composed of control processor and hardware accelerator core. This architecture can support GSM, EDGE, GPRS, UMTS, HSPA, GMR1-3G, and LTE with a throughput of 2.1 Gbps.

V. Reconfigurable Architectures

Reconfigurable Multi-Thread ADRES (MT-ADRES) architecture is illustrated in [25] based on two ADRES processors with a 4x4 coarse-grained array tightly coupled by a shared memory. ADRES processor has three-issue VLIW processor and coarse-grained dynamically reconfigurable functional units. The whole processor switches between VLIW mode and CGA mode. MT-ADRES processor reaches about 1.76 times that of a single ADRES processor and it is implemented in Toshiba 40-nm CMOS technology, occupying 5.29 mm^2 and running at 420 MHz clock. The whole baseband processor has two MT-ADRES processors, digital front end, one FEC decoding engine, including two Viterbi decoders. It consumes about 500 mW and can support 802.11a, WiMAX and LTE standards.

Coarse-Grained Reconfigurable Array (CGRA) processor is described in [26] which operates at 1 GHz clock for IEEE 802.11ac and can achieve 1Gbps data rate. The processor exploit two level of parallelism, instruction and data parallelism and a software optimization was managed for computing operations.

Reconfigurable hardware architecture for modulation [27] is implemented based on FPGA. To handle both QPSK and BPSK modulation schemes hardware multiplexing approach [28] is exploited where different operations may be shared by the hardware which include common block for different standards. The work mentions HDL code generator for different processing module which can be synthetized to FPGA.

Another modulation scheme is also proposed in [29] for AM, ASK, FSK, BPSK and QPSK. It is based on signal flow graph (SFG) which is a model composed of nodes (refer to operations) interconnected by edges (flow of data). It is shown that hardware FPGA resources and the reconfiguration time are reduced due to the proposed synchronous dataflow modeling approach.

A reconfigurable architecture design based on FPGA is mentioned in [30]. Two technologies are used: partial reconfiguration and dynamic reconfigurable port to change respectively the functionality and the digital clock manager frequency. The proposed design involves modulation and IF (intermediate frequency) processing. This architecture is implemented on Virtex-5 LX110T device using the Xilinx ISE 12.4 software suite and it could achieve reductions of 70.4%, 66.3% and 69.8% in respect of slices, DSP48Es and RAMs respectively while three fewer clock oscillator inputs are required compared to traditional fixed function FPGA design. Four standards are supported LTE, WCDMA, 802.16e and 802.11n.

VI. Memory Access and Software Scheduling Optimization

Multi-Pattern Multi-Domain conflict-free access Parallel Memory architecture (MPMD- PMA) is proposed in [31] in order to optimize memory access for SIMD architecture. The memory is organized in three hierarchies: segment, domain and element. Different SDR algorithms with different access patterns and data level parallelisms can be accelerated. It is proved that the speedups of MPMD-PMA over classical PMA with Conflicted Access Serializing and Conflicted Access Assembling are 7.9 and 6.1 respectively.

Scheduling SDR application is required with the increasing number of cores in DSPs. In such context an adaptive Hybrid Flow-Shop (HFS) scheduling method is propose in [32] to schedule a 3GPP LTE physical layer algorithm onto many-core digital signal processors that are modeled as a pipeline of processing elements (PEs) with multiple alternate PEs for each pipeline stage . The HFS is compared to the List scheduler and it is shown that HFS scheduling overhead is increasing very slowly with the number of PEs. Using 256 PEs the HFS overhead is about $5x10^5$ cycles and List overhead is more than $3x10^6$ cycles.

Dataflow modeling is another field of interest in SDR for mapping of the software processes onto the MPSoC and allocation of resources, such as memories and interconnects. An analysis of some synchronous dataflow scenarios for dynamic SDR applications is studied in [33]. It shows that scenario-based worst-case throughput computation of LTE is 2 to 3.4 times more accurate than a static synchronous dataflow graph.

VII. Discussion

This paper presents single, multi-core: homogenous and heterogeneous, reconfigurable architecture, software scheduling and memory access optimization. The single core approach is not well adopted for SDR which require a high level of parallelism in order to process many functionalities such as FFT, coding, modulation. That's why instruction or data parallelism are mandatory which is the case of FUJITSU that has recently proposed its vector processor solution. For

that reason more work focus on multi-core processor to increase the parallel processing. In case of homogeneous approaches [10], [14] software parallelism was required to distribute processing tasks on different cores to increase performance and to meet SDR time constraints. The SIMD technology is also exploited in [8], [9] for data parallelism. In case of heterogeneous core architectures, regarding the cores interconnection we can find two type of interconnected cores NOC [17] or bus [21]. With or without control processor for scheduling and resources allocation [17], [19]. Hardware accelerators can be present [21] to increase the throughput. VLIW and SIMD are also used for instruction and data parallelism [23], [24]. Different metrics are used in Table I for the evaluation of mentioned architectures such as the throughput, surface, technology, power consumption and supported standards. We conclude that homogeneous cores may not address the different functionalities of signal processing for many standards as heterogeneous. Indeed, the heterogeneity of the cores reduces the flexibility but more adapts the core's architecture for the kind of processing allocated to it. So the performance is increased and the multi-core processor become able to implement the hole baseband processing of many standards with a higher throughput. In addition to hardware architecture, software optimization is also experimented for task parallelism such as CUDA, OpenMP platforms and task scheduling and resource allocation [32] that can increase performance. For reconfigurable approach, we believe that combining heterogonous cores with a dynamic and partial reconfigurability for the data path of each core may further increase the performance of an SDR processor. The reconfiguration time could be then a severe constraint.

TABLE I
HARDWARE ARCHITECTURES SUMMARY

Architecture	Throughput	Surface and technology	Power consumption	Supported standards
FUJITSU [6]	12GOPS	28nm	30mW	LTE
GeForce GTX295 [14]	8.58ms per frame	NA	NA	LTE
Genepy [15]	77Gbps	65nm CMOS	192.7mW	LTE
MAGALI [16]	17Gbps	65nm CMOS	477mW	MIMO-LTE, WiMax, 802.11n
Tomhawk2 [17]	80Gbps	36mm2 65nm CMOS	48mW	LTE, WiMAX 802.11
Stream-Access-Oriented [19]	2.7ms for LTE			LTE, W-CDMA, HSDPA, 802.11a, ISDB-T
IMEC [21]				LTE, WiMax, 802.11n
BP-ASP [22]	105GOPS	57.8mm2 130nm CMOS	120mW	LTE
X-GOLD SDR20 [24]	2.1 Gbps	NA	NA	GSM, EDGE, GPRS, UMTS, HSPA, GMR1-3G, LTE
MT-ADRES [25]		5.29mm2 40nm CMOS	500mW	LTE, WiMAX, 802.11

VIII. CONCLUSION

This paper presents different recent state-of-the-art architecture for software-defined radio. Many field are experimented such as data parallelism, instruction parallelism, optimized software algorithm, enhance task scheduling performance and parallelism, increase memory access speedup and multi-core interconnection network. As a conclusion we assume that all these aspect should be taken into account while designing software-defined radio platform.

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