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A Spatial Point Pattern Analysis to Recognize Fail Bit Patterns in Semiconductor Manufacturing

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***Abstract*—**The yield management system is very important to produce high-quality semiconductor chips in the semiconductor manufacturing process. In order to improve quality of semiconductors, various tests are conducted in the post fabrication (FAB) process. During the test process, large amount of data are collected and the data includes a lot of information about defect. In general, the defect on the wafer is the main causes of yield loss. Therefore, analyzing the defect data is necessary to improve performance of yield prediction. The wafer bin map (WBM) is one of the data collected in the test process and includes defect information such as the fail bit patterns. The fail bit has characteristics of spatial point patterns. Therefore, this paper proposes the feature extraction method using the spatial point pattern analysis. Actual data obtained from the semiconductor process is used for experiments and the experimental result shows that the proposed method is more accurately recognize the fail bit patterns.

***Keywords*—**Semiconductor, wafer bin map (WBM), feature extraction, spatial point patterns, contour map.

I. Introduction

SEMICONDUCTOR industry is one of the most important world industries and there are various automated and sophisticated manufacturing processes [1]. The semiconductor manufacturing is composed of complex fabrication (FAB) process and post FAB process. In the post FAB process, the two test steps, probe test and package test, are conducted after FAB process. The probe test is performed on each chip of the wafer to identify defect of dies and classify good dies. Then, the good dies are assembled and packaged in the assembly step [3]. After the assembly step, the package test is conducted to evaluate whether the final chips are good of defective.

One of the main concerns in the process is yield prediction and enhancement. The yield prediction is used for detection of abnormal manufacturing process, investigation of low-yield wafers, elimination of defects, and improvement of final chip yield [2]. The main cause of yield loss is defective chips on the wafer and the defects are affected by fail bits on the chip. Therefore, defects recognition and analysis can contribute to yield improvement.

In general, fail bits are identified visually in the wafer bin map (WBM) collected from the probe test step. Fig.1 shows the WBM and each chip with fail bits. The fail bit is represented by points on a chip and it is the result that the bit did not pass the probe test. Also, the property of a fail bit is marked by the depth of colors. The fail bits on a chip can affect not only low quality of the final chips but yield loss of a wafer. Therefore, it is necessary to analyze fail bit for yield enhancement.

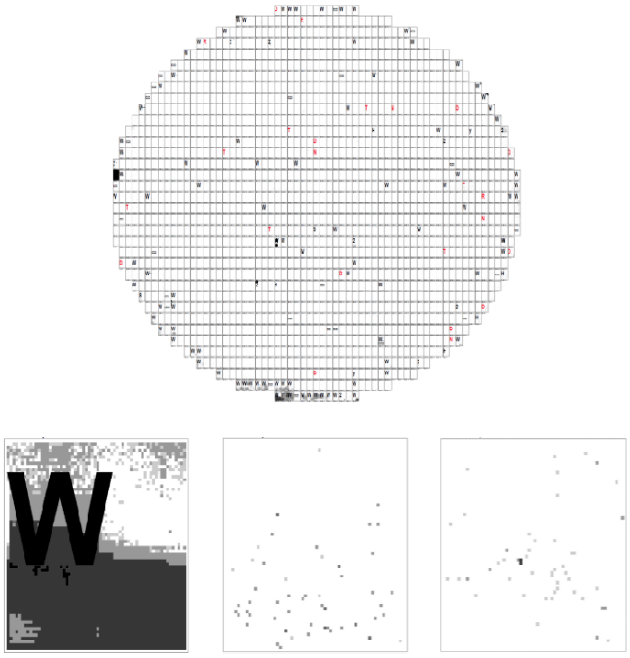

Fig. 1 Top Wafer Bin Map, Bottom: The fail bit of a chip

There have been many studies about clustering and classification methods to recognize failed chip patterns from the WBM data. Data mining methods can efficiently find fail bit patterns existed on the wafer. For example, a neural-network algorithm is used for recognize defect spatial patterns [1]. According to Li's survey [4], a hybrid algorithm of self-organizing map (SOM) neural network and support vector machine (SVM) is proposed for clustered defect spatial patterns of WBM data. Also, a hybrid method combining hierarchical clustering with K-means partitioning is applied to separation of various defect patterns, and the Gaussian EM algorithm is used for estimation of defect zones in the Wang's study [5].

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Cunningham [6] introduces statistical methods for visual defect metrology such as quadrat statistics, spatial point patterns statistics and spatial patterns recognition. In general, the statistical methods for visual defect are used at the chip level in order to estimate the size, shape, and location of large-area defects or clusters of defective chips [7]. The estimated defects can support decision making to engineers and contribute to yield enhancement.

There are many analyzing methods for recognizing defect spatial patterns at the chip level. However, these methods only use the summary data such as the location of defective chips or total fail bit count per chip instead of each fail bit. The summary data discards available information about the fail bit patterns on each chip by aggregating their counts at the chip level. The thousands of fail bits have a lot of information related to defect. Fig.2 illustrates that the same number of fail bits are distributed with different patterns. The fail bit patterns can affect quality of final chips but the total fail bit count cannot contain fail bit patterns. Therefore, it is need to consider fail bit patterns at the cell level in order to analyze defective chips more accurately.

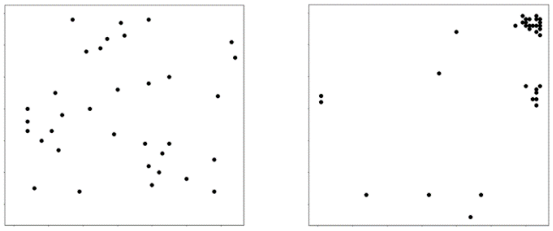


Fig. 2 Different patterns of fail bits Left: Random Patterns, Right: clustered patterns

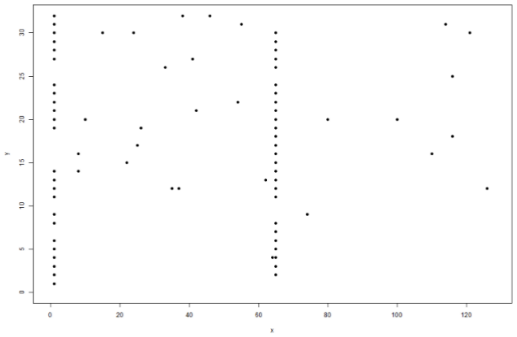
This paper describes a spatial patterns analysis method to extract features that consider fail bit patterns. The fail bit is a point in a region of the two-dimensional plane and the set of fail bits form spatial point patterns [8]. Our approach uses contour map to represent fail bit patterns and the contour map includes both location and density of fail bits.

In the next section, the feature extraction method using a contour map is proposed. We also describe the fail bit patterns of a semiconductor chip and show the result of a contour map applying to a chip. Section III validates the feature extraction method with an experiment using the real WBM data. Section IV discusses about experimental result and further studies.

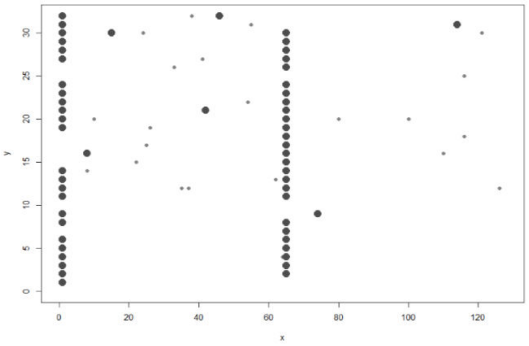
II. Feature Extraction for the Fail Bit Patterns

A. Fail Bit Pattern

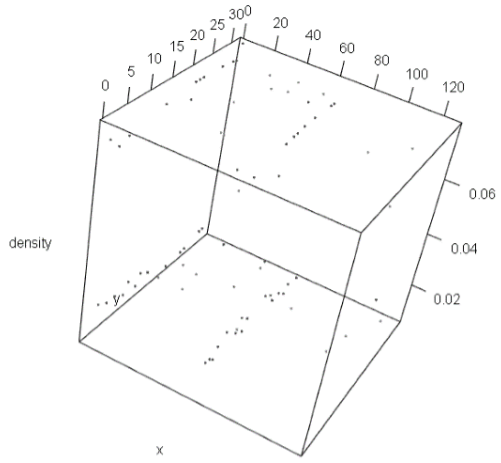
In the probe test, the WBM data are collected and the fail bits are marked by points. The set of fail bits form spatial patterns on the wafer map. Fig. 3 (a) illustrates fail bit patterns of one chip. The point represents a fail bit and the fail bit patterns form the lines at the left side and the middle of the chip. The fail bit of semiconductor chip has five levels that reflect characteristics of the fail type. Therefore, the fail levels are considered to extract features from the fail bit patterns accurately. In Fig. 3 (b), the level of fail bit is indicated by color depth and size, whereas Fig. 3 (a) indicates only fail bit position. The large point means that the fail bit is more critical than the small size fail bit point. Therefore, the fail bits located in the left side and the middle can affect quality of a chip more than other fail bits. Fig. 3 (c) shows the fail bit density by positions in the three-dimensional space. The contour map is estimated by fail bit density and the result can identify in the Fig. 3 (d). The region that the fail bit density is high has narrow contours and the region of low density fail bits has wide contours. Also, many and dense bits are located in the dark area and few sparse bits are located in the light area. Therefore, we can visually recognize the fail bit patterns through a contour map and the contours can represent the fail bit patterns on a chip.



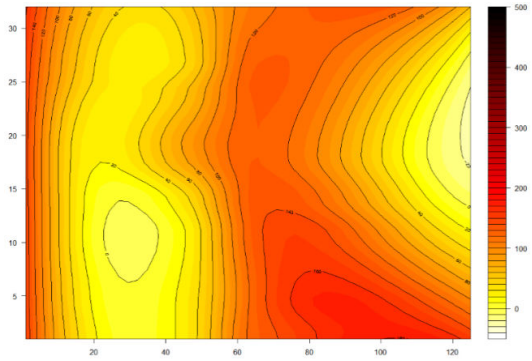
(a) The fail bit patterns



(b) The fail bit patterns considered level of fail



(c) The density of fail bit patterns



(d) The contour map

Fig. 3 The patterns of fail bit

B. Feature Extraction

In the contour map, contours illustrate the fail bit density. Fig.4 is the contour map plot divided by 32 sub-areas. The feature value of each sub-area is a maximum value of the density of contours included in the sub-area. In Fig.4, we can identify that the dark sub-areas have large values and the light sub-areas have small values. Therefore, the feature values contain information about the density of fail bits as well as the fail bit patterns and it can be used for predicting quality of semiconductor chips.

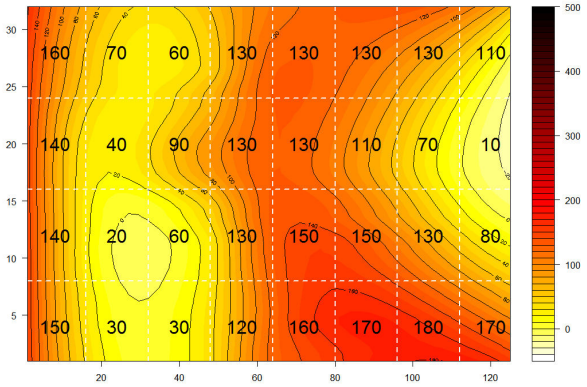


Fig. 4 The contour map consisting of 32 sub-areas

III. Experimental Results

In this section, the proposed feature reflecting the spatial fail bit patterns is compared with existing features such as total fail bit count (TFBC) and normalized total fail bit count (NFBC).

The WBM data is collected in the probe test of actual semiconductor manufacturing process. The NFBC is the feature that considers only the total count of fail bits per chip. The TFBC is the total count of fail bits that reflects characteristics of fail bit. A fail bit is consisting of characteristics such as single fail, row fail, column fail, block fail, and etc. Therefore, TFBC is calculated by weighted average of each fail bit. For the experiments, the mean of proposed feature values is used from described in (1).

$$\text{Mean Contour Density} = \frac{\sum feature\ values\ in\ sub{-}region}{32} \quad (1)$$

Training set and test set includes 1000 chips respectively and the ratio of normal final chip and defective final chip is 1:1. In order to compare the degree of reflection of the fail bits, the mean fail bit patterns density, TFBC and NFBC are sorted in ascending order. If the feature values are large, then the probability that the final chip will be defective is high. Therefore, defective ratio in (2) measures a performance of final defective chip prediction within top determined by thresholds. In this experiment, we use 5%, 15% and 25% thresholds.

$$\text{Defective Ratio} = \frac{The\ number\ of\ real\ defect\ chips}{The\ number\ of\ total\ chips} \times 100 \quad (2)$$

Table I shows experimental results. According to Table I, the defective ratio of proposed feature is higher than TFB and NF generally.

TABLE I
DEFECTIVE RESULT FOR MCD, TFBC AND NFBC

Dataset	Threshold = 0.05			Threshold = 0.15			Threshold = 0.25		
	MCD	TFBC	NFBC	**MCD**	TFBC	NFBC	**MCD**	TFBC	NFBC
1	**0.686**	0.560	0.520	**0.662**	0.480	0.457	**0.586**	0.480	0.451
2	**0.667**	0.500	0.480	**0.642**	0.480	0.480	**0.618**	0.484	0.462
3	**0.667**	0.540	0.529	**0.636**	0.553	0.500	**0.598**	0.504	0.480
4	**0.627**	0.540	0.480	**0.563**	0.533	0.563	**0.586**	0.508	0.556
5	**0.706**	0.560	0.500	**0.629**	0.527	0.507	**0.625**	0.520	0.506
6	0.627	**0.660**	0.600	0.576	**0.580**	0.530	**0.614**	0.564	0.536
7	**0.647**	0.580	0.540	**0.609**	0.540	0.517	**0.590**	0.536	0.496
8	**0.608**	0.560	0.600	**0.583**	0.547	0.530	**0.586**	0.532	0.534
9	**0.647**	0.620	0.580	**0.629**	0.553	0.529	**0.598**	0.544	0.548
10	**0.569**	0.540	0.490	**0.609**	0.593	0.487	**0.629**	0.504	0.492
11	0.569	**0.580**	0.431	**0.629**	0.533	0.586	**0.598**	0.520	0.544
12	**0.647**	0.560	0.440	**0.589**	0.507	0.493	**0.574**	0.522	0.516

Figs. 5-7 illustrate the experimental result visually and the threshold is 5%, 15% and 25% respectively. In the 5% threshold, the proposed feature can predict final defective chips more accurately in most datasets. However, performance of TFB is higher than proposed feature in the dataset 6 and 11. It seems like that the performance of prediction is some affected by property of datasets. In the 15% and 25% threshold, the prediction performances of proposed feature are higher than other features.

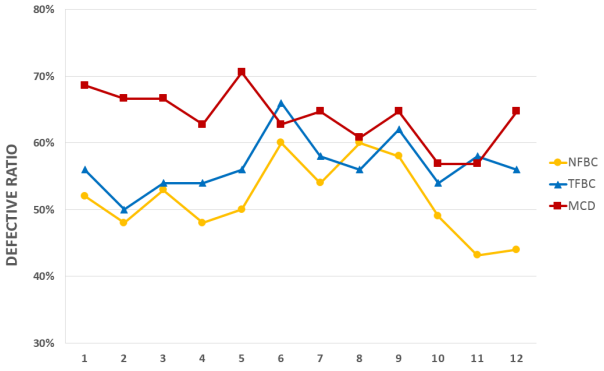


Fig. 5 Defective ratio within top 5% (Threshold = 0.05)

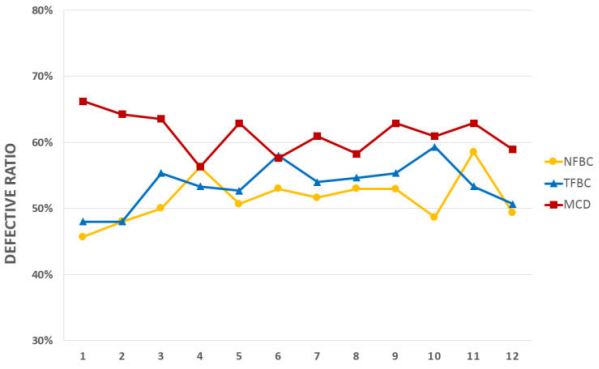


Fig. 6 Defective ratio within top 15% (Threshold = 0.15)

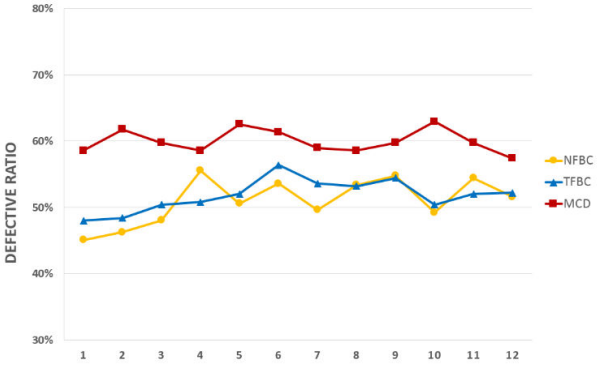


Fig. 7 Defective ratio within top 25% (Threshold = 0.25)

IV. CONCLUSION

In the semiconductor industry, it is important to analysis data collected from the manufacturing process. Especially, the WBM data is widely used for detecting defective chips and yield prediction. In practice, the summary data that is extracted at chip level such as TFB and NF is applied for yield management system despite the loss of a lot of information.

This research proposes a feature extraction method that reflects the fail bit patterns at cell level using spatial point pattern analysis. Actual WBM data obtained from the semiconductor manufacturing processes is tested through the proposed feature extraction method. In most datasets, the feature reflecting bit patterns at chip level has higher defective ratio than TFBC and NFBC that just reflecting number of bits. The fail bit pattern can affect the quality of final chip and the feature that considering fail bit pattern is useful for improvement performance of yield prediction. As the future study, it is expected to research clustering and classification methods for recognizing types of defect at chip level.

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