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A Single Phase ZVT-ZCT Power Factor Correction Boost Converter

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***Abstract*—**In this paper, a single phase soft switched Zero Voltage Transition and Zero Current Transition (ZVT-ZCT) Power Factor Correction (PFC) boost converter is proposed. In the proposed PFC converter, the main switch turns on with ZVT and turns off with ZCT without any additional voltage or current stresses. Auxiliary switch turns on and off with zero current switching (ZCS). Also, the main diode turns on with zero voltage switching (ZVS) and turns off with ZCS. The proposed converter has features like low cost, simple control and structure. The output current and voltage are controlled by the proposed PFC converter in wide line and load range. The theoretical analysis of converter is clarified and the operating steps are given in detail. The simulation results of converter are obtained for 500 W and 100 kHz. It is observed that the semiconductor devices operate with soft switching (SS) perfectly. So, the switching power losses are minimum. Also, the proposed converter has 0.99 power factor with sinusoidal current shape.

***Keywords*—**Power factor correction, zero-voltage transition, zero-current transition, soft switching.

I. Introduction

POWER factor correction (PFC) basically means to be reduced to zero reactive power and harmonics. These harmonic currents cause some problems such as higher harmonic distortion, poor power factor at AC input voltage and current. The boost converters are usually used in AC-DC PFC converters due to simple construction, easy control and high power density. These PFC converters are operated in continuous conduction mode (CCM) at high power applications. In this case, the reverse recovery current of the main diode causes to turning off loss of the main diode, turning on loss of the main switch, electromagnetic interference (EMI) noises [1], [2].

To obtain lower harmonic current, faster dynamic response and higher power density, AC-DC converters should be operated at high frequency as possible. However, the high switching frequency leads to switching power losses and electromagnetic interference (EMI) noises [3]. This problem can be solved by using the soft switching (SS) techniques instead of hard switching (HS) techniques. SS techniques are Zero Voltage Switching (ZVS), Zero Current Switching (ZCS), Zero Voltage Transition (ZVT), and Zero Current Transition (ZCT) techniques [4]-[20].

In recent years, a lot of papers have been proposed to realize soft switching for the boost PFC converter. Some of these proposed converters have major disadvantages. In [7], the main switch turns off with HS. In [8], the SS is not provided under 0.5 duty cycle and there is an additional current stress on the main switch. In [9], a magnetic coupled inductor is used in the ZVT-ZCT converter. So, parasitic oscillations occur due to the leakage inductance. In [10], there is additional current stress on the main switch. It means to be increased losses of converter increase.

A converter is proposed in order to overcome all of these problems. The proposed ZVT-ZCT PFC boost converter is shown in Fig. 1. In this converter, the main switch turns on with ZVT and turns off with ZCT. The main diode turns on with ZVS and turns off with ZCS. Also, there is no additional current or voltage stress on the main devices. The auxiliary switch and the auxiliary diode both turn on and turn off with ZCS. The proposed converter decreases EMI noise and operates even under a wide range of line and load voltages. Due to this features, the proposed converter has a high power factor and lower total harmonic distortion.

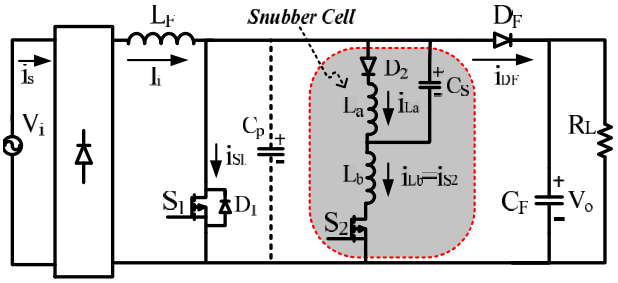

Fig. 1 The basic circuit scheme of the proposed signal phase ZVT-ZCT PFC boost converter

II. Operating Steps

The circuit scheme of the single phase soft switching PFC boost converter is given in Fig. 1. In this converter, V_i is rectified input dc voltage, V_o is output voltage, L_F is main inductance, C_F is output capacitor, R_L is output load, S_1 is the main switch, S_2 is the auxiliary switch, and D_F is the main diode. D_1 is the body diode of the main switch. C_p is the sum of the parasitic capacitors of the main switch and the main diode. L_a and L_b are upper and lower snubber inductances, C_s is snubber capacitor, and D_2 is the auxiliary diode. Also, in Fig. 1, i_s is input AC current, I_i is main inductance current, i_{S1} is current of the main switch, i_{S2} is current of the auxiliary switch, i_{La} is L_a inductance current, i_{Lb} is L_b inductance current i_{DF} is main diode current.

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The following assumptions are taken into consideration while making theoretical analysis of the proposed circuit.

- Output voltage V_o and input current I_i are constant for one switching cycle.
- All semiconductor devices and resonant circuits are ideal.
- The reverse recovery times of all diodes are not taken into account.

Twelve steps occur in the steady state operation of the converter in one switching cycle. The equivalent circuit schemes of the operation steps are shown in Fig. 2 (a)–(k).

A. Step 1 [$t_0 < t < t_1$: Fig. 2 (a)]

Before this step begins, S_1 and S_2 switches are in off state. The main inductance current I_i passes through the main diode D_F. At $t = t_0$, $i_{S1} = 0$, $i_{DF} = I_i$, $i_{S2} = i_{Lb} = 0$, $i_{La} = 0$, $v_{Cp} = V_o$ and $v_{Cs} = -V_{C0}$ are valid. When a gate signal is applied to S_2 switch, the current of D_F decreases while the current of S_2 and the voltage of C_s increase. So, S_2 switch turns on with ZCS because of L_b snubber inductance and the main diode D_F turns off with ZCS.

At the end of this step ($t = t_1$), the current of D_F falls to zero when the current of L_b reaches to input current I_i. Also, C_s capacitor is charged until a voltage value ($-V_{C1}$).

B. Step 2 [$t_1 < t < t_2$: Fig. 2 (b)]

At $t = t_1$, $i_{S1} = 0$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = I_i$, $i_{La} = 0$, $v_{Cp} = V_o$ and $v_{Cs} = -V_{C1}$ are valid. In this step, a resonance begins through C_p–C_s–L_b–S_2. The energy of C_p is transferred to L_b and C_s. Therefore, v_{Cp} voltage decreases while i_{Lb} current and v_{Cs} voltage are increasing.

At the end of this step ($t = t_2$), voltage of C_s falls to zero and current of L_b is maximum. Also, the voltage of C_s reaches to a valid ($-V_{C2}$).

C. Step 3 [$t_2 < t < t_4$: Fig. 2 (c)]

At $t = t_2$, $i_{S1} = (I_i - I_{L2\_max})$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = I_{L2\_max}$, $i_{La} = 0$, $v_{Cp} = 0$ and $v_{Cs} = -V_{C2}$ are valid. At the beginning of this step, D_1 diode turns on with ZVS and a new resonance starts through L_b–L_a–C_s. So, the energy of L_b is transferred to L_a and C_s. This step that D_1 is at on state is called ZVT area. A gate signal is applied to S_1 switch in the middle of this step. Therefore, S_1 turns on with ZVT perfectly.

At $t = t_3$, the current of L_b falls to the input current value and D_1 turns off with ZCS. Then, the current of S_1 increases and the current of L_b goes on decreasing.

At the end of this step ($t = t_4$), the current of L_b falls to zero when the current of S_1 reaches to input current value.

D. Step 4 [$t_4 < t < t_5$: Fig. 2 (d)]

At $t = t_4$, $i_{S1} = I_i$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = 0$, $i_{La} = I_{L4}$, $v_{Cp} = 0$ and $v_{Cs} = V_{C4}$ are valid. At the beginning of this step, S_2 switch turns off with ZCS since the current of S_2 is equal to zero at that moment. Additionally, the energy of L_a inductance is transferred to C_s with L_a–D_2–C_s resonance.

At the end of this step ($t = t_5$), the voltage of C_s is equal to maximum value ($-V_{C5}$) in reverse direction and the current of L_a is equal to zero.

E. Step 5 [$t_5 < t < t_6$: Fig. 2 (e)]

During this step, the main switch S_1 conducts the input current I_i. The duration of this step is a large part of the on state duration of the conventional PWM boost converter and is determined by the PWM control to provide PFC.

F. Step 6 [$t_6 < t < t_8$: Fig. 2 (f)]

At $t = t_6$, $i_{S1} = I_i$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = 0$, $i_{La} = 0$, $v_{Cp} = 0$ and $v_{Cs} = -V_{C5}$ are valid. At the beginning of this step, a gate signal is applied to S_2 and it turns on with ZCS due to L_b inductance. A resonance begins through C_s–L_b–S_2–D_1. Then, the current of S_1 switch decreases while the current of L_b is increasing.

At $t = t_7$, the current of S_1 is equal to zero when the current of L_b is equal to the input current value. Then, D_1 conducts the excess of input current. This step that D_1 is at on state is called ZCT area. The control signal of S_1 is removed in the middle of this step. For this reason, S_1 switch turns off with ZCT perfectly.

At the end of this step ($t = t_8$), the current of L_b reaches to maximum value (I_{L8_max}) when the voltage of C_s is equal to zero.

G. Step 7 [$t_8 < t < t_9$: Fig. 2 (g)]

At $t = t_8$, $i_{S1} = (I_i - I_{L8\_max})$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = I_{L8\_max}$, $i_{La} = 0$, $v_{Cp} = 0$ and $v_{Cs} = 0$ are valid. In this step, a new resonance begins through L_b–L_a–C_s. The energy of L_b is transferred to L_a and C_s. Then, the voltage of C_s begins to become positive and the current of L_a begins to increase. At $t = t_9$, D_1 turns off when the current of L_b falls to the input current value.

H. Step 8 [$t_9 < t < t_{10}$: Fig. 2 (h)]

At $t = t_9$, $i_{S1} = 0$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = i_{La} = I_i$, $v_{Cp} = 0$ and $v_{Cs} = V_{C9}$ are valid. In this step, a resonance occurs through C_p–L_a–L_b–C_s. During this step, the current of L_a and the voltage of C_s increase while the current of L_b inductance decreases.

At the end of this step ($t = t_{10}$), the current of L_b falls to zero and the control signal of S_2 is removed. So, S_2 turns off with ZCS.

I. Step 9 [$t_{10} < t < t_{11}$: Fig. 2 (i)]

At $t = t_{10}$, $i_{S1} = 0$, $i_{DF} = 0$, $i_{S2} = i_{Lb} = 0$, $i_{La} = I_{L10}$, $v_{Cp} = V_a$ and $v_{Cs} = V_{C10}$ are valid. In this step, both the parasitic capacitor C_p is charged under the constant input current and the energy of L_a is transferred to the C_s through L_a–D_2–C_s resonance.

At the end of this step ($t = t_{11}$), the main diode D_F turns on with ZVS when the voltage of C_p reaches to output voltage.

J. Step 10 [$t_{11} < t < t_{12}$: Fig. 2 (j)]

At $t = t_{11}$, $i_{S1} = 0$, $i_{DF} = I_i$, $i_{S2} = i_{Lb} = 0$, $i_{La} = I_{L11}$, $v_{Cp} = V_o$ and $v_{Cs} = -V_{C11}$ are valid. In this step, all of the energy of L_a is transferred to C_s.

At the end of this step ($t = t_{12}$), the current of L_a falls to zero and v_{Cs} reaches to $-V_{C0}$ value.

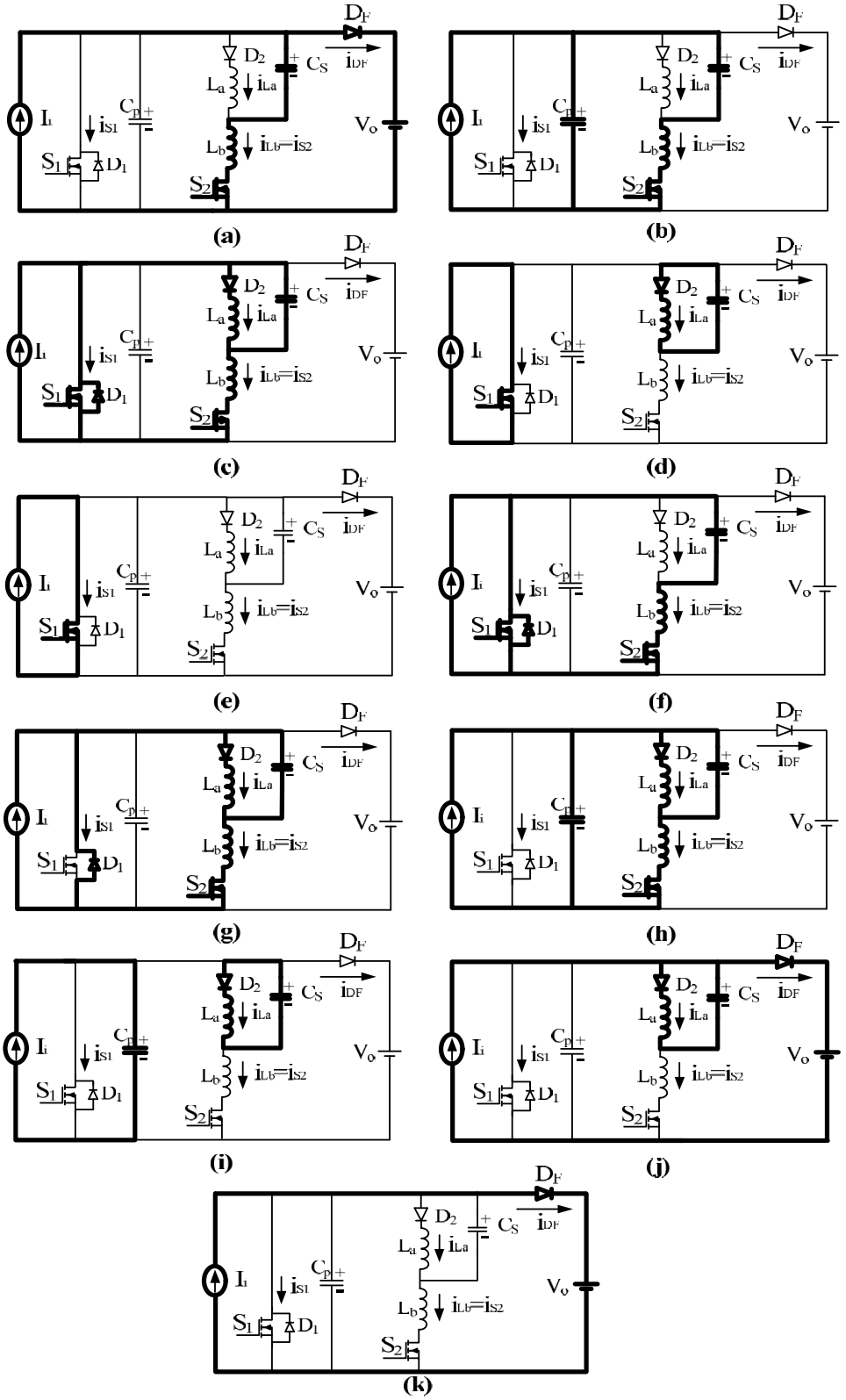

Fig. 2 Equivalent circuit of the operating steps in proposed single phase ZVT-ZCT PFC converter. (a) Step 1, (b) Step 2, (c) Step 3, (d) Step 4, (e) Step 5, (f) Step 6, (g) Step 7, (h) Step 8, (i) Step 9, (j) Step 10, (k) Step 11

K. Step 11 [$t_{12} < t < t_{13}$: Fig. 2 (k)]

During this step, the main diode D_F conducts input current I_i and the snubber circuit is not active. This time period is determined by the PWM control and large part of the off state of the converter.

At $t = t_{13}$, the operation steps are finished and it is returned to initial conditions. The steps expressed are repeated in the next switching cycle.

III. Simulation Results

It is realized a prototype of the proposed single ZVT-ZCT PFC boost converter for 500 W and 100 kHz in PSIM program. The simulation parameters and the value of the devices are given in Table I.

TABLE I
THE SIMULATION PARAMETERS AND THE VALUE OF THE DEVICE OF PROPOSED CONVERTER

Output Power (P_o)	500 W	**Upper Snubber Inductance (L_a)**	4 µH
Switching Frequency (f)	100 kHz	**Lower Snubber Inductance (L_b)**	2 µH
AC Input Voltage (V_i)	200 V	**Snubber Capacitor (C_s)**	15 nF
DC Output Voltage (V_o)	400 V	**Parasitic Capacitor (C_p)**	6 nF
Main Inductance (L_F)	500 µH	**Output Capacitor (C_F)**	470 µF

The simulation circuit scheme of the proposed converter is given in Fig. 3. The control signals of the switches are obtained with PFC average current mode controller. The block scheme is given Fig. 4. The simulation results of the converter are shown in between Figs. 5-7.

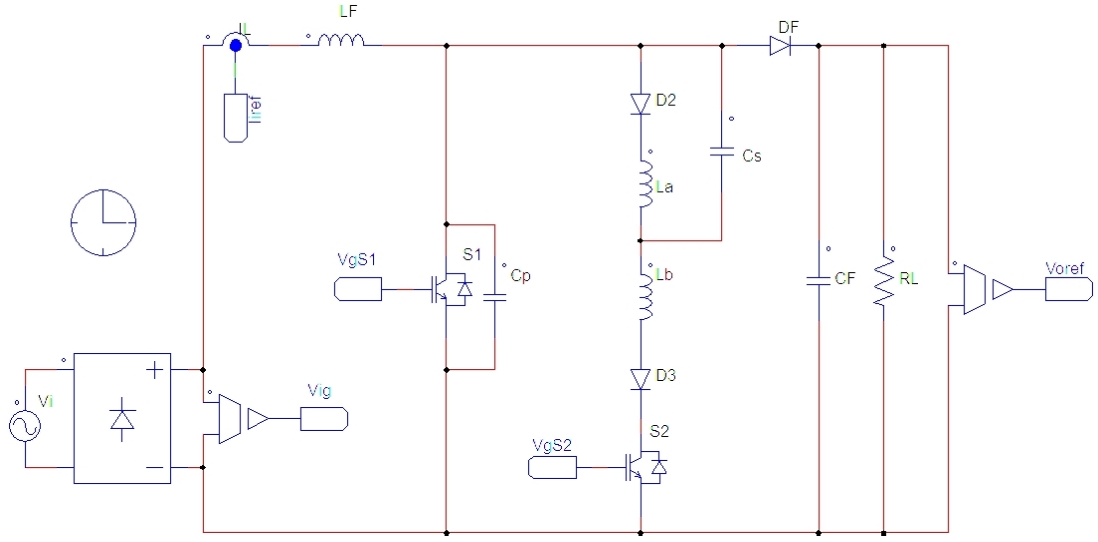

Fig. 3 The simulation circuit scheme of the proposed PFC converter

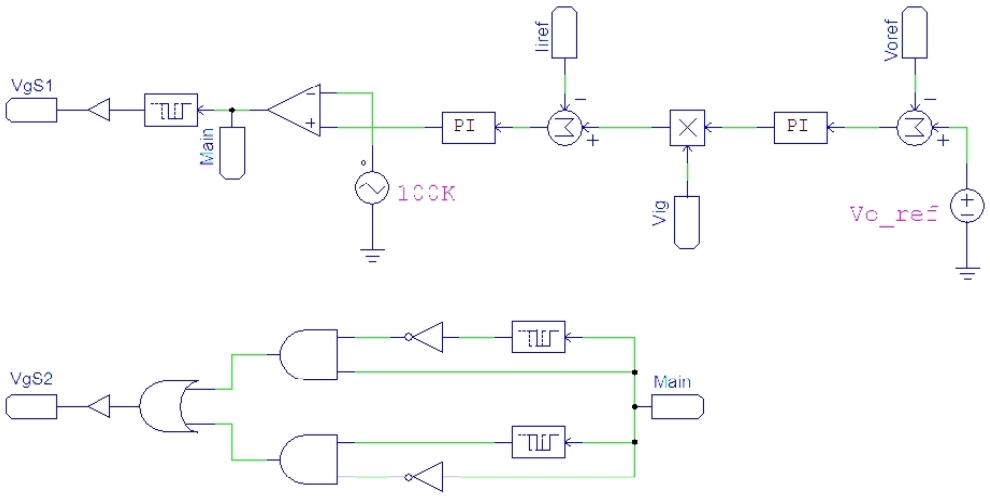

Fig. 4 The average current control block scheme for PWM control signals

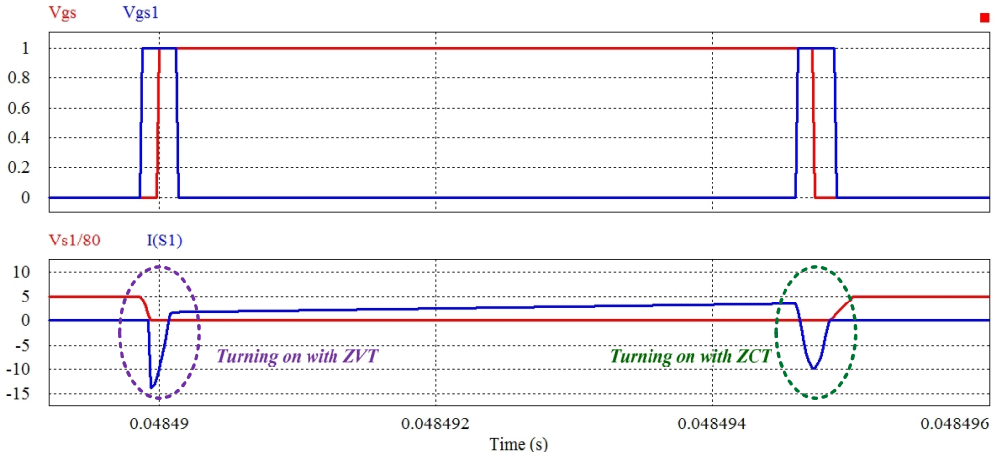

Fig. 5 Respectively; the control signals of main switch and auxiliary switch, the voltage of main switch and the current of main switch

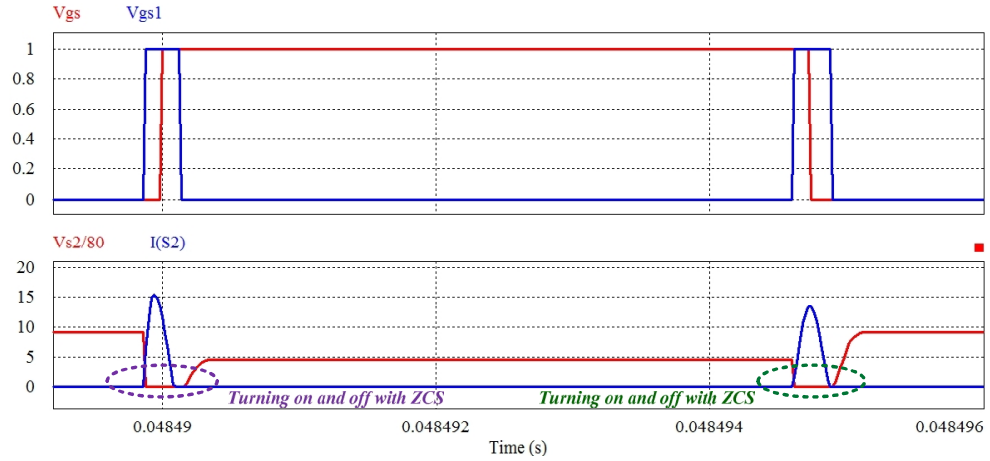

Fig. 6 Respectively; the control signals of main switch and auxiliary switch, the current and voltage of auxiliary switch

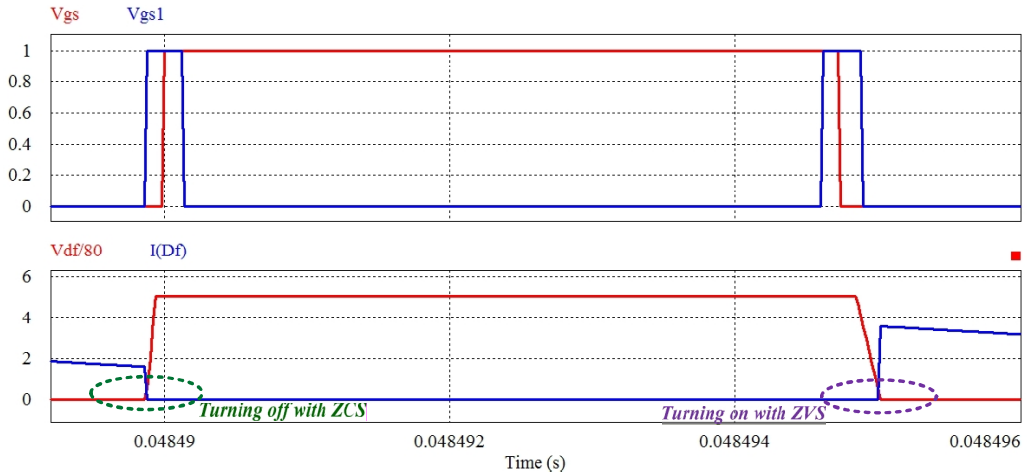

Fig. 7 Respectively; the gate signals of the switches, the current and voltage of the main diode

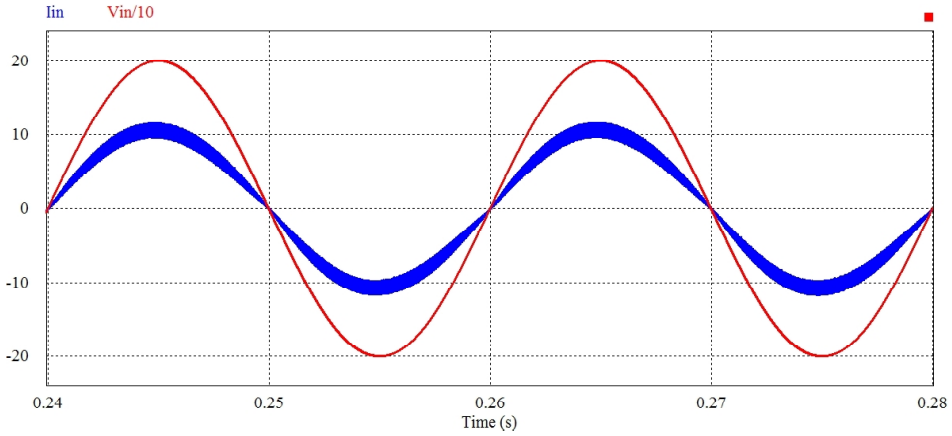

Fig. 8 The input voltage and current waveforms of proposed PFC converter

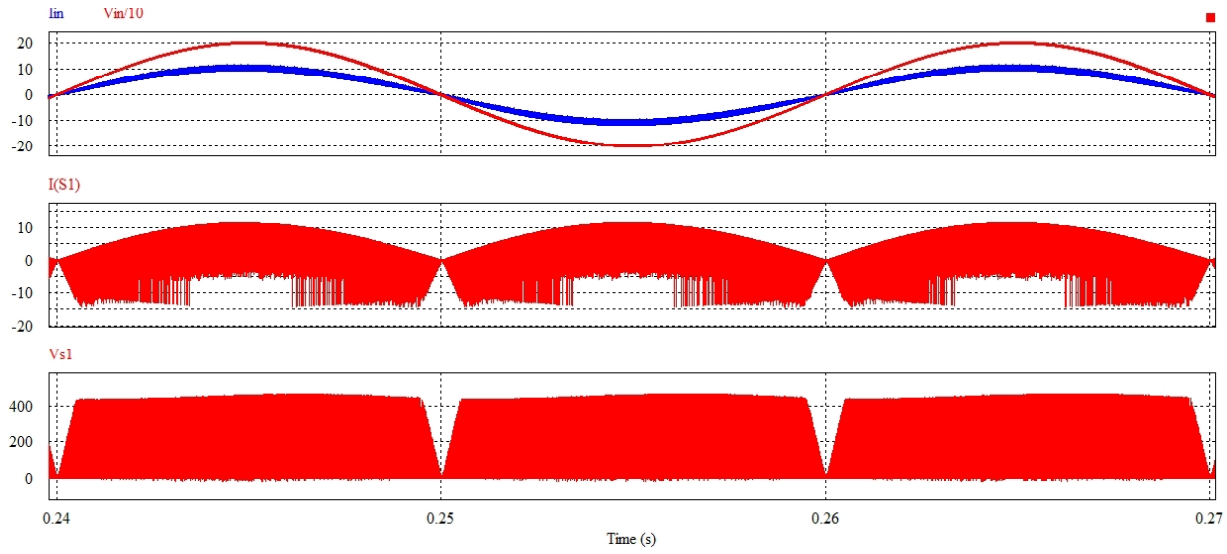

Fig. 9 Respectively; the input voltage and current waveforms of proposed PFC converter, the current waveform and the voltage waveform of the main switch

The gate signal and current–voltage waveforms of the main switch S_1 are given in Fig. 5. As shown in the figure, the voltage of main switch is fallen to zero with the aid of the snubber cell before the main switch is turned on. Then, the main switch turns on with ZVT while the body diode of main switch is on state. For turning off, the current of main switch is fallen to zero with the aid of the snubber cell. Then, the main switch turns off under ZCT while the body diode of main switch is at on state. Moreover, there is no additional voltage or current stress on the main switch during this process.

The gate signal and current–voltage waveforms of the main switch S_2 are given in Fig. 6. As shown in the figure, the auxiliary switch turns on and off with ZCS. However, there is additional voltage stress on the auxiliary switch and its value is equal to almost $2V_o$.

The gate signal of the switches and current–voltage waveforms of the main diode D_F are given in Fig. 7. As shown in the figure, the main diode turns on with ZVS and turns off with ZCS. Also, it is clear that there is not any voltage and current stress on the main diode.

The input voltage and current waveforms are given in Fig. 8. The power factor of the proposed converter is near unity with 0.99. Also, it is seen that the proposed PFC converter operates in CCM. The proposed converter is tested at universal input line voltage and very wide load ranges. It is observed that it keeps operating under soft switching conditions successfully for the whole line and load ranges. Also, the input voltage and current waveforms are given together with the voltage and current waveforms of the main switch in Fig. 9. The input voltage value is scaled 1/10 ratio in Figs. 8 and 9. The voltage value of the main switch is scaled 1/80 ratio in Fig. 9.

IV. Conclusions

In this paper, a ZVT-ZCT PFC boost converter with active snubber cell is proposed. The snubber cell provides to ZVT turning on and ZCT turning off for the main switch. It

operates in a little part of the switching period. Also, it provides ZVS turning on and ZCS turning off for the main diode. For this reason, it minimizes the reverse recovery losses of the main diode. The proposed converter does not compose any extra voltage or current stress on the main devices.

The auxiliary switch turns on and turns off under ZCS. However, extra voltage stress occurs on the auxiliary switch. The extra current or voltage stress does not occur on the other auxiliary elements and all of them operate under soft switching.

The proposed converter solves many drawbacks of the PFC converters presented earlier. All semiconductor devices in the circuit are switched with soft switching. A detailed steady-state analysis of the proposed converter is presented. The theoretical analysis of the proposed converter is exactly verified by 500 W and 100 kHz prototype. The average current mode control method is used in the proposed converter. The power factor of the proposed converter is measured nearly 0.99.

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