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A novel optimized JTAG interface circuit design

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***Abstract*—**This paper describes a novel optimized JTAG interface circuit between a JTAG controller and target IC. Being able to access JTAG using only one or two pins, this circuit does not change the original boundary scanning test frequency of target IC. Compared with the traditional JTAG interface which based on IEEE std. 1149.1, this reduced pin technology is more applicability in pin limited devices, and it is easier to control the scale of target IC for the designer.

***Keywords*—**Boundary scan, JTAG interface, Test frequency, Reduced pin

I. Introduction

As the integrate circuit developing towards large size and high integration, the IEEE 1149.1 Test Access Port (TAP) and Boundary-scan architecture commonly referred to as JTAG is becoming a popular testing method which provides an effective and low-cost way for test [1]. Meanwhile, most electric systems today are highly integrated with multiple ICs. In order to add other functional pins to the chip or reduce the package cost, the number of pins and signal lines should be decreased as much as possible.

Up to now, there are several reduced pin JTAG interface techniques. ARM Ltd has developed a two wire interface for communicating JTAG signals between a controller and target IC [2]. Debug Innovations has developed a one wire interface for communicating JTAG signals between a controller and target IC [3]. The recently announced IEEE 1149.7 standard for Advanced Test and Debug is developing, among other things, a two wire interface for communicating JTAG signals between a controller and target IC [4]. Lee Whetsel of TI Company has found another way to achieve this goal, whereas the operation frequency needs to be halved [5]. These reduced pin JTAG interface techniques can not only used for test, but also for debug operations.

Although the reduced pin JTAG interface of this paper does not offer any pin reduction advantage over those listed above, it does provide another novel optimized method which does not change the original boundary scanning test frequency of target IC. Compared with the traditional JTAG interface which based on IEEE std. 1149.1, this reduced pin technology is not affect the effective speed of test and is more applicability in pin limited devices. What's more, it is easier to control the scale of target IC for the designer.

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The rest of this paper is organized as follows. Section II introduces the scheme design of this optimized JTAG interface circuit. Then detailed descriptions are given in Section III. Section IV presents a complete operation process of this optimized JTAG interface circuit. Finally, conclusions are drawn in Section V.

II. Optimized JTAG Interface Scheme Design

Fig. 1 illustrates a conventional 5-signal interface between a JTAG controller and a boundary scan circuit within a target IC. The JTAG interface consists of the standard TDO, TMS, TCK, TDI and TRST signals. The JTAG controller is timed by a clock input signal (CLK) from a clock source, which in turn times the operation of the boundary scan circuit via the TCK signal. The target IC can be, but not limit to, a microcontroller IC, a microprocessor IC, a DSP, an FPGA/CPLD, an ASIC, and so on. The arrangement between the JTAG controller and the target IC and its use in performing test, emulation, debug, and trace operations is well known in the industry.

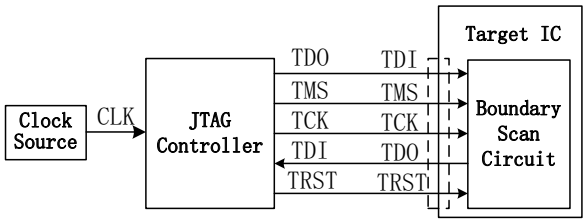

Fig. 1 A conventional 5-signal interface circuit

The novel optimized method described in this paper is able to access JTAG using only one or two pins. Fig. 2 shows the architecture of optimized JTAG interface scheme design. In order to form a new JTAG controller, the JTAG controller is interfaced to a data switching circuit (DSC), a TAP state machine (TSM1) and a simultaneously bi-directional transceiver (SBT) via TDO_0, TMS_0, CLK, TDI_0 and TRST_0 signals. The boundary scan circuit is connected to a data processing circuit (DPC), a controller, a reset and synchronization circuit (RSC), a TAP state machine (TSM2) and a simultaneously bi-directional transceiver (SBT) via TDO, TMS, TCK, TDI and TRST signals [5]–[9]. The new JTAG controller is interfaced to the target IC via a data I/O (DIO) signal and a clock (CLK) signal. The DIO wire has two transmission modes. One is simultaneously pass JTAG signals between the new JTAG controller and the target IC, the other is as a one-way input signal for the target IC. The CLK signal can

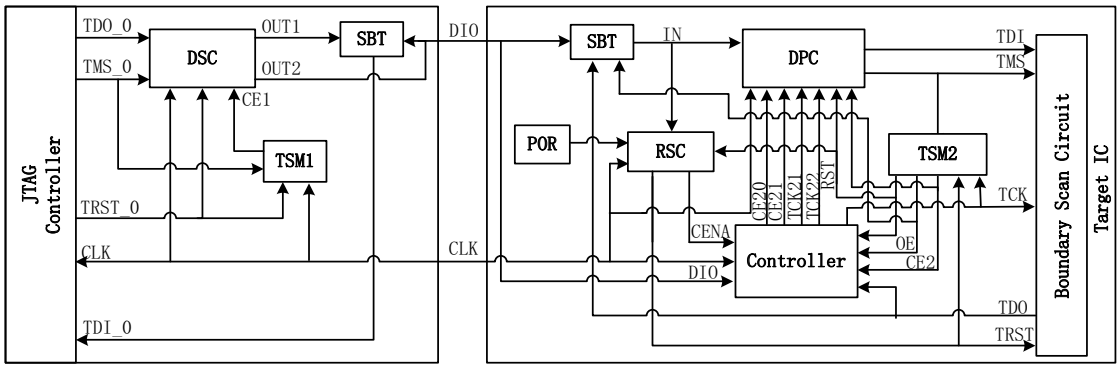

Fig. 2 Optimized JTAG interface scheme design

not only be a clock from the new JTAG controller or the target IC, but also be driven by an external clock source. If it is sourced by both the new JTAG controller and the target IC, the CLK signal can be ignored and only the DIO signal is left between the new JTAG controller and the target IC.

The DSC is used for switching the TDO_0 and TMS_0 signals output from the JTAG controller, whereas the DPC is used for providing proper TMS and TDI signals for the boundary scan circuit. As defined in the IEEE std. 1149.1, the TSM1 and TSM2 circuits are synchronous finite state machines that respond to changes at the TMS and TCK signals of the TAP and control the sequence of operations of the circuitry. The power-on reset (POR) circuit produces a temporary low active power on reset pulse whenever the target IC is first power up. The reset and synchronization of this design is insured by the RSC. Meanwhile, as will be mentioned below, the test sequence "$D_0D_1 \cdots \cdots D_{N-2}D_{N-1}$" described in this paper should be packaged to "0 $D_0D_1 \cdots\cdots D_{N-2}D_{N-1}0$".

III. Detailed Descriptions

A. TAP state machine

Fig. 3 illustrates the state diagram of the IEEE std. 1149.1 TAP state machine. As illustrated in Fig. 2, there are two TAP state machines defined in the IEEE std. 1149.1. The TSM1 circuit inputs the TMS_0 signal, the CLK signal, and the TRST_0 signal which is used for asynchronous reset. A CE1 signal output from the TSM1 circuit to the DSC is forced high whenever the TSM1 circuit is transferred into Shift-IR (SHI) state, Exit1-IR (E1I) state, Update-IR (UPI) state, Shift-DR (SHD) state, Exit1-DR (E1D) state or Update-DR (UPD) state. The TSM2 circuit inputs the TMS signal output from the DPC, the TCK signal output from the controller, and the TRST signal output from the RSC. A CE2 signal output from the TSM2 circuit to the controller is forced high whenever the TSM2 circuit is transferred into Select-IR-Scan (SLI) state, Capture-IR (CPI) state, Shift-IR (SHI) state, Select-DR-Scan (SLD) state, Capture-DR (CPD) state or Shift-DR (SHD) state. A RST signal output from the TSM2 circuit is connected to the standard "Reset*" output of the 1149.1 TSM, whereas an OE signal is forced high whenever the TSM2 circuit is transferred into Shift-IR (SHI) state or Shift-DR (SHD) state.

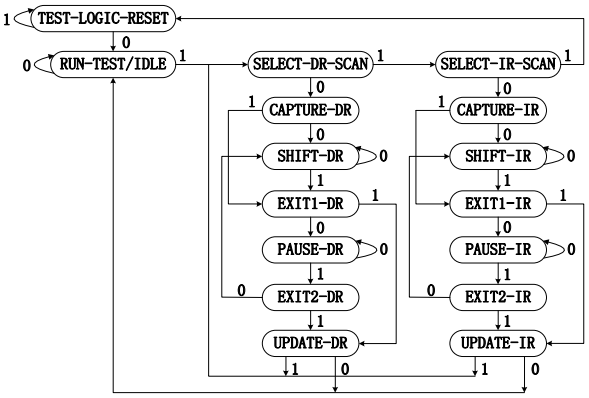

Fig. 3 State diagram of the IEEE std. 1149.1 TAP state machine

B. Data switching circuit

Fig. 4 shows the architecture of the DSC. It consists of two parallel connected Flip-Flops and two 3-state buffers. The Flip-Flops input parallel TDO_0 and TMS_0 signals from the JTAG controller, and are set to logic ones by the low active TRST_0 signal whenever the JTAG controller is first power up. When the TRST_0 signal is high, the Flip-Flops which provide data for the 3-state buffers are able to respond to the CLK input. The 3-state buffers are controlled by the CE1 signal output from the TSM1 circuit, and only one data path can be selected at the same time.

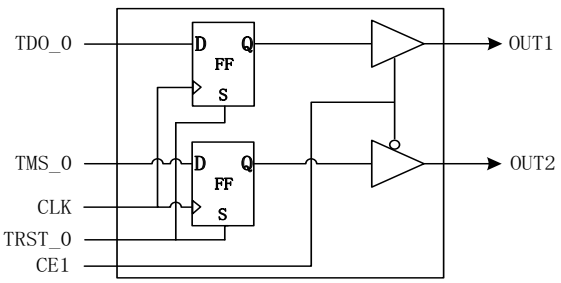

Fig. 4 Architecture of the DSC

C. Data processing circuit

Fig. 5 illustrates the DSC in more details. It consists of three Flip-Flops and two 3-state buffers. When initialized, the Flip-Flops which have a Reset input are reset to logic zeros by the RST signal, while the Flip-Flop which has a Set input is set to logic one by a CE20 signal output from the controller. These Flip-Flops have different clock signals shown in Fig. 5. The 3-state buffers are controlled by the CE2 signal output from the TSM2 circuit and a CE21 signal output from the controller respectively. The DSC outputs parallel TMS and TDI signals for the boundary scan circuit.

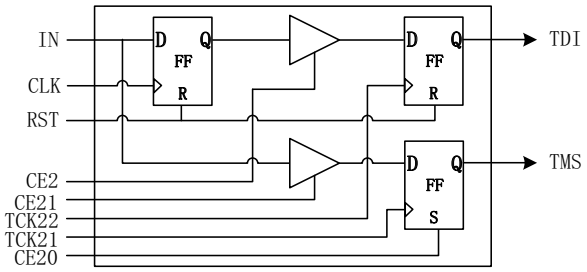

Fig. 5 Architecture of the DPC

D. Controller

Fig. 6 is an example design for the controller. The controller inputs CLK, CENA, RST, OE, TDO, DIO and CE2 signals. The controller outputs TCK, CE20, TCK21, TCK22 and CE21 signals. When the CENA signal output from the RSC or the RST signal is high, the controller is able to output the TCK signal to the boundary scan circuit. The cont signal shown in Fig. 6 is a key signal that requiring more attentions. If the cont signal is high, the following three conditions should be satisfied:

1) The OE signal should be high. It means the TSM2 circuit is transferred into Shift-IR (SHI) state or Shift-DR (SHD) state.
2) The TDO signal should be driven to logic zero. With the test sequence being controlled, it is easy to get the desired TDO value.
3) The DIO signal should be driven to high-level voltage, which means the DIO wire is transferred into one-way input mode and is driven by an OUT2 signal output from the DSC.

When the cont signal is high, the CE20 signal is forced high too. Then the Flip-Flop controlled by the CE20 signal will provide a logic one output for the TSM2 circuit, and the state of the TSM2 circuit will transfer from the SHI (or SHD) state to the E1I (or E1D) state.

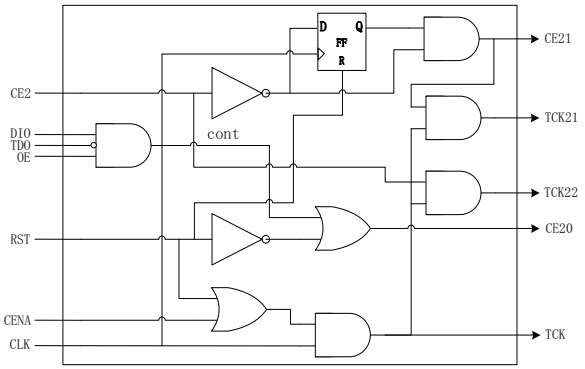

Fig. 6 Architecture of the controller

The operation of the controller based on the state transition of the TSM2 circuit is illustrated in the timing diagram of Fig. 7. As seen, the frequency of the TCK signal is equal to the frequency of the clock source driving the CLK signal. Therefore the JTAG controller and the boundary scan circuit of the target IC operate at the original frequency of the clock source. For example, if the clock source is 100MHz, the JTAG operations timed by the CLK and TCK signals will operate at 100MHz too. The SBTs shown in Fig. 2 are high speed transceivers which support DIO data transfers at these and potentially higher clock frequency [5]–[9].

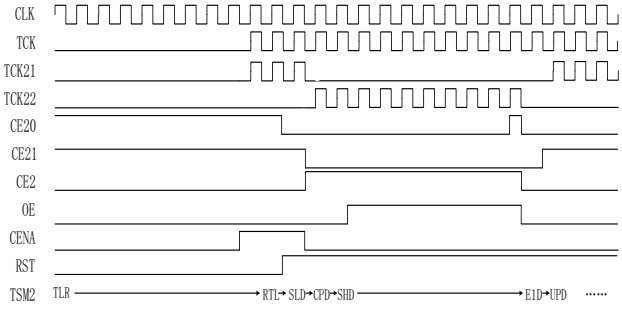

Fig. 7 Timing diagram of the controller

E. Reset and synchronization circuit

As shown in Fig. 2, the RSC inputs an IN signal from the right side SBT circuit, a temporary low active power on reset pulse from the POR circuit when the target IC is first power up, the CLK signal, and the RST signal. The RSC outputs a CENA signal to the controller, and the TRST signal to the TSM2 and boundary scan circuit. The purposes of the RSC circuit are: (1) to maintain the TSM2 and boundary scan circuit in a reset state when the target IC is operating normally in a system with no JTAG controller connected to the DIO and CLK signals; (2) to allow synchronizing the operation of the target IC to the operation of the JTAG controller when they are initially connected via the DIO and CLK signals.

The synchronization operation is achieved by the DSC outputting a synchronization code to the IN input of the RSC via the DIO signal. In response to the synchronization code input, the RSC sets TRST and CENA high to enable the

operation of the controller, the TSM2 circuit, and the boundary scan circuit. The state diagram of Fig. 8 shows the operation of the RSC. As seen, the RSC can only finish the synchronization in response to the exact input sequence of "1100". When the synchronization is done, the TMS and TDI signals are properly received by the boundary scan circuit.

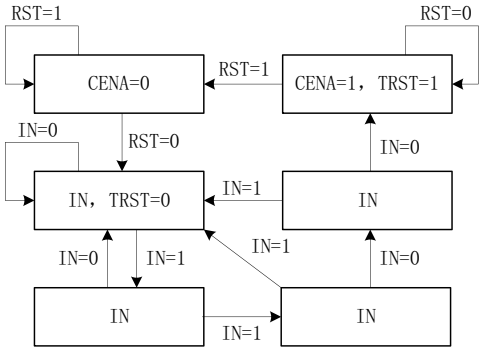

Fig. 8 State diagram of the RSC

F. Simultaneously bi-directional transceiver

Fig. 9 shows the architecture of the SBT circuits [5]–[9]. The left side SBT circuit consists of an Input circuit (I), an output buffer, and a resistor. The right side SBT circuit consists of an Input circuit (I), a 3-state buffer, a pull down circuit, and a resistor. The Input circuit of the left side SBT circuit inputs the voltage level on DIO and the OUT1 signal from DSC, and outputs an appropriate TDI_0 signal to the JTAG controller, based on the DIO voltage level and the logic level of the OUT1 signal. The Input circuit of the right side SBT circuit inputs the voltage level on DIO and the TDO signal from the boundary scan circuit, and outputs an appropriate IN signal to the DPC and RSC, based on the DIO voltage level and the logic level of the TDO signal. The PD circuit serves to pull DIO low when it is not being externally driven and when the 3-state buffer is disabled by OE. With the 3-state buffer disabled and DIO not externally driven, the PD circuit forces a logic zero on the IN input to the DPC and RSC which causes the RSC to maintain a reset condition on the controller and boundary scan circuit via the CENA and TRST signals. The resistors serve to limit the current flow on DIO when the buffers are outputting opposite logic levels and also to establish the mid-level voltage on the DIO wire [5].

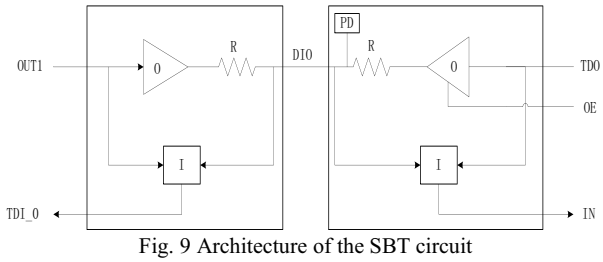

Fig. 9 Architecture of the SBT circuit

As illustrated in Fig. 2, the DIO signal can also be driven by the OUT2 signal which will establish the low-level or high-level voltage on the DIO wire. The truth table of the OUT2 signal and simultaneous input/output signals of the SBT circuits are summarized in Table I. The "X" shown in this table indicates it is a "do not care" signal.

TABLE I
TRUTH TABLE

OUT2	OUT1	TDI_0	DIO	IN	TDO	OE
X	LOW	LOW	LOW	LOW	LOW	HIGH
X	LOW	HIGH	MID	LOW	HIGH	HIGH
X	HIGH	LOW	MID	HIGH	LOW	HIGH
X	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
LOW	X	X	LOW	LOW	X	LOW
HIGH	X	X	HIGH	HIGH	X	LOW

IV. Circuit Implementation

In the timing diagram of Fig. 10, a complete operation process of the optimized JTAG interface circuit between the new JTAG controller and the target IC is illustrated. The "X" shown in Fig. 10 indicates it is a "do not care" bit.

The dotted portion of the TMS_0 signal provides the synchronization code for the RSC via the IN signal. After the reset condition for the controller, the TSM2 circuit, and the boundary scan circuit is removed, the packaged test sequence "$0D_0D_1\cdots\cdots D_{N-2}D_{N-1}0$" shown in the dotted portion of the TDO_0 signal is output from the JTAG controller. As seen, the real test sequence of the TDI signal for the boundary scan circuit is "$00D_0D_1\cdots\cdots D_{N-2}D_{N-1}$", whereas the output sequence of the TDO signal is "$D_0'D_1'\cdots\cdots D_{N-2}'D_{N-1}'00$". The dotted portion of the TMS signal indicates that the conditions forcing the cont signal to high would have been satisfied.

Relatively speaking, the operation state of the TSM2 circuit is two cycles later than the TSM1 circuit, and the input TDI sequence of the boundary scan circuit is two cycles later than the output TDO_0 sequence of the JTAG controller too. By packaging the test sequence, the sequence "$D_0D_1\cdots\cdots D_{N-2}D_{N-1}$" input to the boundary scan circuit is three cycles later than the sequence "$D_0D_1 \cdots \cdots D_{N-2}D_{N-1}$" output from the JTAG controller. Thus, there is enough time for the DIO wire switching the transmission mode from bi-directional way mode to one-way mode.

When an operation is complete, the JTAG controller can output a string of serialized TMS_0 which set to logic ones to cause the TSM1 and TSM2 circuits to transition into the Test Logic Reset (TLR) state. As defined in the IEEE std. 1149.1, the TSM1 and TSM2 circuits is designed to transition from any of its states to the TLR state whenever it receives at least 5 logic high inputs on TMS. Finally, if the operation needs to be continued, the synchronization doesn't need to be performed again.

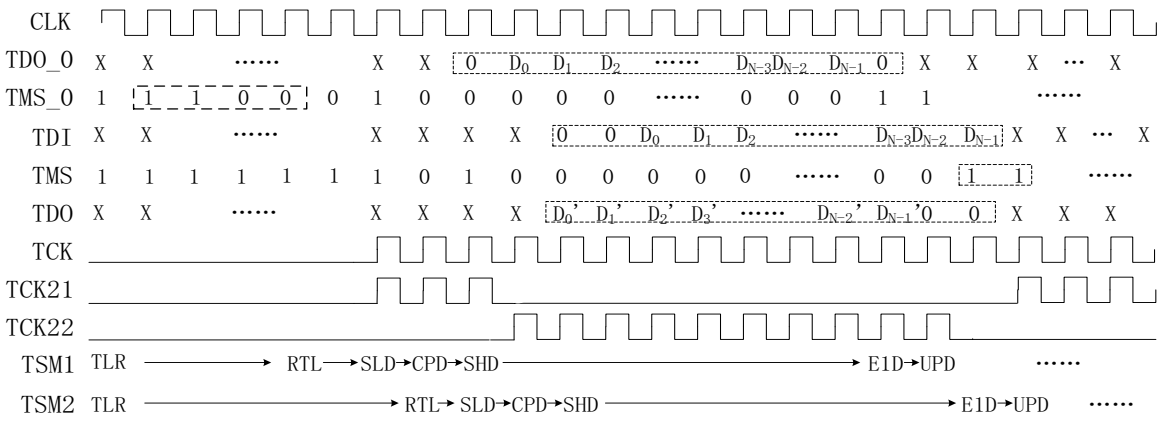

Fig. 10 Timing diagram of this design

V. Conclusions

The novel optimized JTAG interface circuit proposed in this paper is able to access JTAG using only one or two pins. Since it does not change the original boundary scanning test frequency of target IC, this reduced pin technology is not affect the effective speed of test and is more applicability in pin limited devices. By the way, since the standard TDO, TMS, TCK, TDI and TRST signals are reduced into one or two signals, it is easier to control the scale of target IC for the designer.

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