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A Novel Approach of Multilevel Inverter with Reduced Power Electronics Devices

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***Abstract*—**In this paper family of multilevel inverter topology with reduced number of power switches is presented. The proposed inverter can generate both even and odd level. The proposed topology is suitable for symmetric structure. The proposed symmetric inverter results in reduction of power switches, power diode and gate driver circuits and also it may further minimize the installation area and cost. To prove the superiority of proposed topology is compared with conventional topologies. The performance of this symmetric multilevel inverter has been tested by computer based simulation and prototype based experimental setup for nine-level inverter is developed and results are verified.

***Keywords*—**Cascaded H- Bridge (CHB), Multilevel Inverter (MLI), Nearest Level Modulation (NLM), Total Harmonic Distortion (THD).

I. Introduction

IN recent era, the multilevel inverter is state of art power conversion system for high voltage and high power quality applications. The two-level inverter with existing semiconductor technology may not suit for high voltage application which may increase the high voltage stress on switch, high Electro Magnetic Interference (EMI) and poor power quality output [1], [2]. In order to solve these issues the conventional multilevel inverters are introduced, but it may require high number of power semiconductor devices. So, the researchers are developing new multilevel inverter topologies with existing semiconductor technology to meet require high power quality with reduced power semiconductor devices [3]. Because of these advantages multilevel converters are more attractive in high power applications. However, the important benchmark for designing multilevel inverters is listed below.

- Low voltage stress on switches
- Low Electromagnetic interference.
- Low Harmonic Distortion
- Absence of LC Filter
- Modularity
- More redundant state
- Reliability
- Low Cost

The conventional multilevel inverter topologies are (i) Neutral Point Clamped (NPC) (ii) Flying Capacitor (FC) and (iii) Cascaded H-Bridge (CHB). These converters provide better output quality by increasing smaller voltage level; they are applied for commercial applications and industrial applications like AC Drives and FACTS Devices [4]. Theoretically, these topologies are capable of generating infinite number of equal stepped voltage level. Whereas, practically, the number of level increases as it requires more number of power switches, clamping diode, flying capacitor and associated components respectively. Furthermore, this may increase the installation area, cost of the converter and complex control circuits. In last few decades several authors were finding solution by introducing novel multilevel inverter topologies with reduction of power switches [5]-[8]. In symmetrical method all the dc sources voltage have unique value and it ensures good modularity. Different rating of switches are required in asymmetrical method due to different dc sources voltage magnitude, this may generate high number of output voltage with minimum dc source. But multilevel inverter modularity may reduce. An Attempt has been made in [9] to propose a new multilevel inverter topology with reduced power switches. This converter required different voltage rating of power switches. In addition, the voltage stress on the switches will be high for higher number of levels. Novel multilevel inverter topology is proposed in [10]. This topology is combination of both power diodes and IGBT. In this method, the more number of power switches is reduced but it may require more numbers of power diodes, which may produce voltage spikes at load. In such a way several multilevel inverter are proposed with own advantage and disadvantages [11]-[14]. Aforementioned literatures are considered for symmetric topology only.

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II. Proposed Topology

In this section, detailed explanation of two different basic structures of proposed topologies are introduced and mathematical expression for number of voltages level (N_{Step}), Number switches (N_{Switch}) and number of dc sources voltages calculation are presented.

A. Suggested Topology

The basic double and single source unit is shown in Figs. 1 (a) & (b). V_{dcn} & $V_{dc(n-1)}$ is connected in series with S_1 switch and Parallel with P_1. Fig. 1 (c) shows the generalized basic structure of proposed topology which is the combination of both the single and double source basic unit. N_S is the number of dc source voltages, which are separated with series connected unidirectional controlled power switches are termed as voltage adder $(S_1, S_2, S_3 \ldots S_n)$ and also each dc sources are connected with parallel switches are termed as subtractor $(P_1,$

*P2, P3…. Pn).*The n^{th} V_{dc} is represented as V_{dcn}. In proposed method V_{dcn} is not connected with any parallel switches, V_{dcn-1} and V_{dcn-2} are connected together with parallel switch of P_n, remaining each dc sources voltages are connected with series/parallel combination respectively.

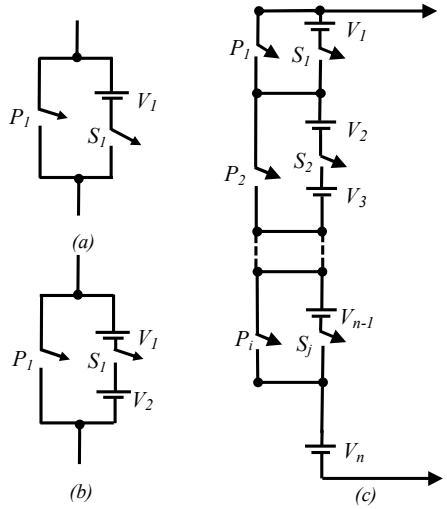


Fig. 1 Proposed Symmetric Topology (a) Basic single source basic unit (b) Basic double source basic unit (c) Generalized structure for odd and even number of sources

The corresponding switches will be fired to synthesize positive stepped waveform. The series/parallel unit is connected series with H-bridge, which is used to create a current flow in both directions at load terminals. Fig. 1 shows the generalized structure of new symmetrical topology is proposed for N_{Step} with equal dc sources Values (V_{dc}).The proposed topology constructed with unidirectional (arrangement of series/parallel connection) power switch along with series connection of equal dc sources which are connected with the H-bridge. The proposed topology is separated into two units (i) combined adder/subtractor switches with dc voltage source is termed level generator unit (ii) Polarity changer H-Bridge unit. The switch (P_n) is connected parallel with two dc sources (V_{dcn-1}, V_{dcn-2}) as shown in Fig. 2. According to Fig. 1 the IGBTs of (S_1, P_1), (S_2, P_2) · · · · · (S_{n-1}, P_n) turn on simultaneously the V_{dc1}, V_{dc2}…..V_{dcn-1} will be short circuited with same dc source. Either one of the corresponding adder/subtractor switches will turn ON and turn OFF from the Table I.

The maximum output voltage $(V_{o,max})$ is sum of all the DC source voltage is given:

$$V_{o,max} = V_{dc1} + V_{dc2} + V_{dc3} + \cdots\cdots + V_{dcn} \quad (1)$$

$$V_{o,max} = \sum_{i=1}^{n} V_{dcn} \quad (2)$$

Equations (1) & (2) illustrate the output level of adder/ Subtractor circuit. Both the positive and negative levels synthesized by the H-bridge circuit, at load $(V_{o,\ Load})$ synthesized stepped output voltage level will be obtained as mentioned below

$$V_{o,max} = \begin{cases} \sum_{i=1}^{n} +V_{dcn} & , H_{S1}, H_{S4} = 1 \\ \sum_{i=1}^{n} -V_{dcn} & , H_{S2}, H_{S3} = 1 \end{cases} \quad (3)$$

In this proposed topology, the number of output voltage levels (N_{Step}), number of IGBT (N_{Switch}) and the number of DC sources (N_s) are calculated as follows, respectively:

$$N_{Step} = 2N_s + 1 \quad (4)$$

Still, the proposed topology structure varies with the odd and even number of DC sources and therefore it is necessary to express the requirement of number of IGBT for given output levels and for given number of DC sources is given below:

$$N_{Switch} = \begin{cases} N_s + 5 & , N_s = odd \\ N_s + 4 & , N_s = even \end{cases} \quad (5)$$

B. Power Stage Operation:

In this section, 9-level symmetric multilevel inverter is explained to understand the proposed topology. In order to provide more number of output voltage steps with minimum number of switches by using proposed symmetric topology as shown in Fig. 2 The magnitude of the each steps are calculated for 9-level inverter is shown in below.

$$\left.\begin{aligned} V_{dc1} &= P_1 + P_2 \\ V_{dc2} &= P_2 + S_1 \\ V_{dc3} &= P_1 + S_2 \\ V_{dc4} &= S_2 + S_1 \end{aligned}\right\} \quad (6)$$

where $P_1 = V_{dc}$ & $P_2 = 2V_{dc}$ (i.e.) P_1 will subtract the V_{dc} voltage and P_2 will subtract $2V_{dc}$ voltage respectively. To obtain a nine level output voltage, the mathematical equations are expressed in (6). Each dc voltage sources are subtracted with corresponding ON state parallel switches (Subtractor switch). The theoretical explanations as follows: The H-bridge inverter is series connected with polarity generator which can produce possible five positive output levels from 0 to maximum peak value of $4V_{dc}$, In H-bridge inverter switches will create the current path to load in both positive and negative direction by switching corresponding switches $(H_{S1}$& $H_{S4})$ & $(H_{S2}$& $H_{S3})$. From Table I, the corresponding switches will be on and off to produce the stepped waveform. The H-Bridge should withstand for sum of all the dc sources, which may increase the voltage rating of switches and cost of the inverter. Here worth to mention that the number of IGBTs are reduced, which reduce the cost of the switches, gate driver circuits and other supporting components.

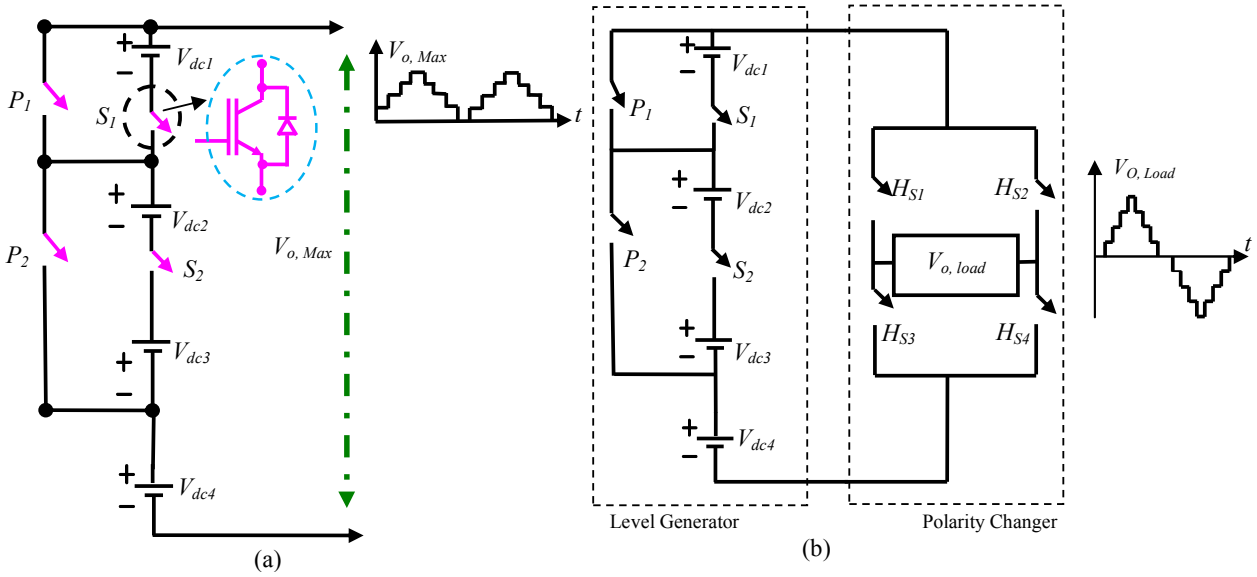


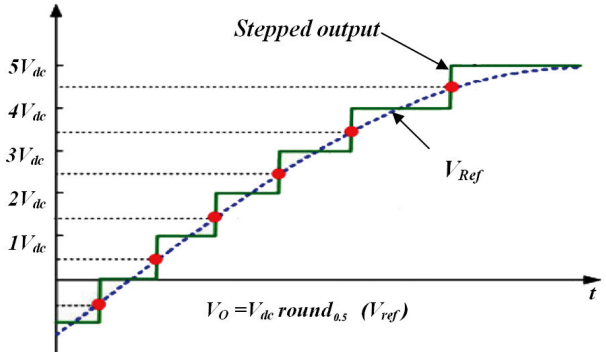
Fig. 2 Proposed 9-Level inverter (Even Sources) (a) Level generator circuit (b) with polarity changer

TABLE I
SWITCH STATES OF 9-LEVEL PROPOSED TOPOLOGY

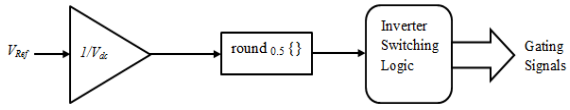
Switch States								Voltage level at $V_{o,Load}$
P_1	P_2	S_1	S_2	H_{S1}	H_{S2}	H_{S3}	H_{S4}	
1	1	0	0	1	0	0	1	$+V_{dc4}$
0	1	1	0	1	0	0	1	$+V_{dc4}+V_{dc1}$
1	0	0	1	1	0	0	1	$+V_{dc2}+V_{dc3}+V_{dc4}$
0	0	1	1	1	0	0	1	$+V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4}$
0	0	0	0	1	1	0	0	0
1	1	0	0	0	1	1	0	$-V_{dc4}$
0	1	1	0	0	1	1	0	$-(V_{dc4}+V_{dc1})$
1	0	0	1	0	1	1	0	$-(V_{dc2}+V_{dc3}+V_{dc4})$
0	0	1	1	0	1	1	0	$-(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$

III. NEAREST LEVEL MODULATION TECHNIQUE

There are several modulation techniques proposed for multilevel inverter.



(a)



(b)

Fig. 3 Nearest level selection: (a) Level synthesis and (b) control diagram

Some of the well known modulation techniques are Fundamental Swicthing Method [15], Carrier Based Pulse Width Modulation (CBPWM) Techniques [16], Space Vector Pulse Width Modulation (SVPWM) [17], Selective Harmonic Elimination Method [18], Hysteresis Modulation [19] and Hybrid Modulation Techniques [20]. These modulation techniques are successfully implemented in industrial for different applications like AC Drives [21], [22], FACTS and Renewable Energy.In this paper, the Conventional NLM is used, which is generate steps with base concept of round off technique as shown in Fig. 3. This is suitable for higher number of output voltage level. This is easily performed using the round {} function and integer closest to x. Since this is like half height method, the additional convention is that half-integers are always rounded to even number. The largest possible error is then limited by $V_{dc}/2$.

The main switching angles are determined by the following equation:

$$\alpha_i = Sin^{-1}\left(2i - 1/m - 1\right) \qquad Where\ i = 1,2,\cdots\frac{m-1}{2} \qquad (7)$$

where α_i is switching angle and m is Number of output voltage level.

IV. Comparison with Other Topologies

This paper main objective is to reduce the number of power switches in multilevel inverter. As shown Fig. 4, the comparison between N_{Step} *Vs* $N_{Switches}$ is presented. The proposed topology required less number of switches than other topologies. In [11] is required minimum number of IGBT compared to proposed inverter. But it may require high number of power diode. Addition to this, the voltage spike will occur at load side due to interloping in diode (Reverse recovery problem). To avoid this issue (i) the load R value should be higher than L value and (ii) should use LC filter at output side. So, this may not suitable for highly inductive load.

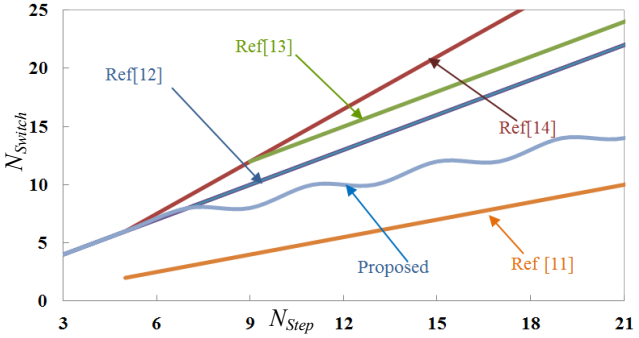


Fig. 4 Comparison of Number of Steps against Number of Switches

The proposed novel symmetric multilevel inverter has significant improvements compared to conventional Cascaded Multilevel Inverter. In Table II, the parameters such as Peak Inverse Voltage *(PIV)*, Number of switches and DC sources are listed.

TABLE II
Comparison of Power Component Requirement for Conventional Cascaded and Proposed Multilevel Inverter

Parameters	Conventional Cascaded Inverter	Proposed
No.of DC Sources	Ns	Ns
No.of Switches	4Ns	Ns+4 for even Ns+5 for odd
No.of Output Voltage Levels	2Ns+1	2Ns+1
PIV [pu]	4Ns	6Ns-2

V. Simulation and Experimental Results

To validate the good performance of the proposed 9-level inverter, the simulation studies are carried out for symmetrical multilevel inverter. The simulation has done by MATLAB/Simulink software. The switching pattern is developed based on the on state switches with K-map as shown in Fig. 5. To generate stepped waveform the conventional Nearest Level method is used. In this method the constant values *(C1,C2…Cn)* are compared with absolute sine waveform (V_{ref}) to generate appropriate signals as shown in Figs. 6 (a) & (b).

$$\begin{aligned} &C1 = 0.5 \\ &C2 = 1 + 0.5 \\ &C3 = 2 + 0.5 \\ &\text{for } n^{th} \text{ Level} \\ &Cn = n - 1 + 0.5 \qquad \text{where } n = {}^{N_{Level}} - {}^{1}\!/_{2} \end{aligned} \tag{8}$$

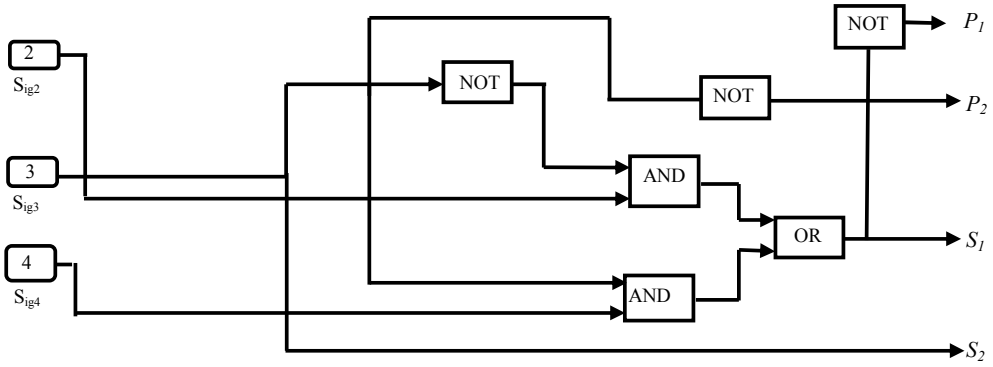


Fig. 5 Switching Pattern for Proposed Topology from generated Signals

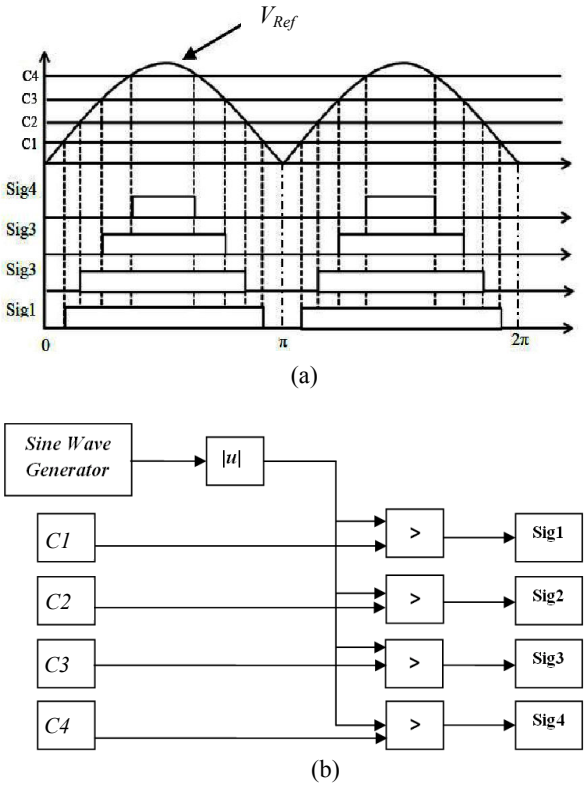


Fig. 6 (a) Nearest Voltage Level Control Technique as a sum of 9-Levels; (b) Switching Signals generation Logic

The simplified switching states are expressed as follows.

$$S_1 = Sig_2\overline{Sig_3} + Sig_3Sig_4 \quad (9)$$

$$S_2 = Sig_3 \quad (10)$$

$$P_1 = \overline{S_1} \quad (11)$$

$$P_2 = \overline{S_2} \quad (12)$$

where Sig_1, Sig_2, Sig_3 and Sig_4 are represent the signals obtained after comparison of constant values. These signals are chosen as a variable for K-map and after simplification the corresponding switching signals is obtained refer to (9) – (12). The simulated output voltage and current waveforms along with harmonic spectrum as shown in Figs. 7 and 8 respectively. In simulation the THD values for voltage and current is 9.05% and 1.82 % respectively. The experimental output voltage and current is shown in Fig. 9. In simulation each dc source has values of 55V (i.e. sum of 220V) and in hardware arrangement has the value of dc input voltage is 15V (i.e sum of 60V). But both simulation and experimental has same values of **R=100 and L=100mH**. The experimental maximum output voltage $V_{O,Max}$ is $60V$ as shown in Fig. 10.

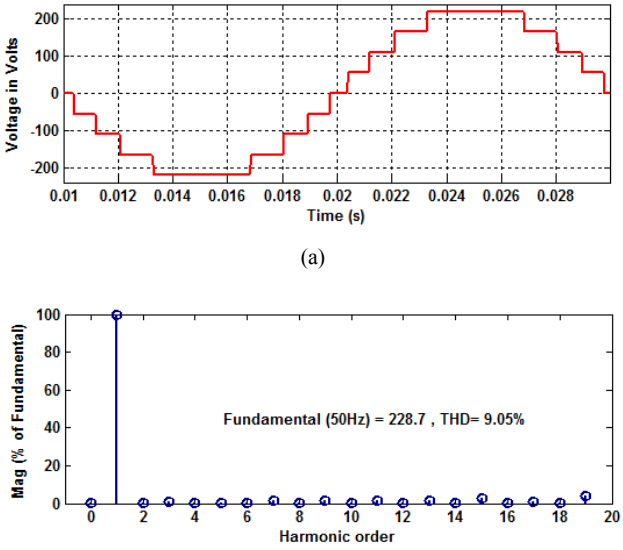


Fig. 7 (a) Simulation output voltage waveform (b) Voltage harmonic spectrum

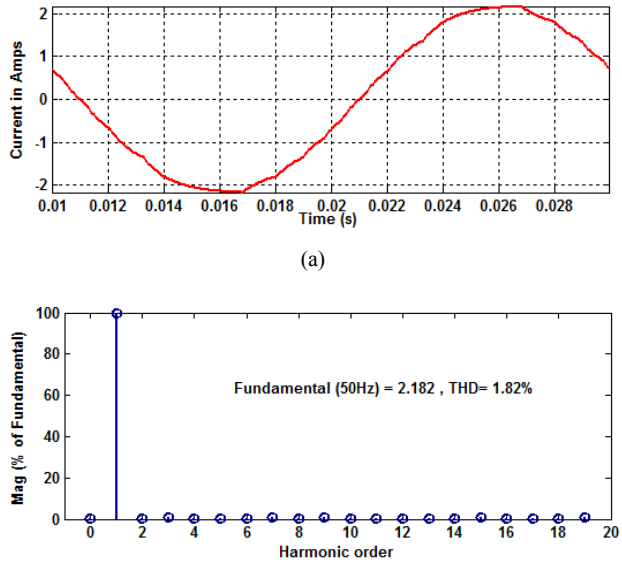


Fig. 8 (a) Simulation output current waveform (b) Current harmonic spectrum

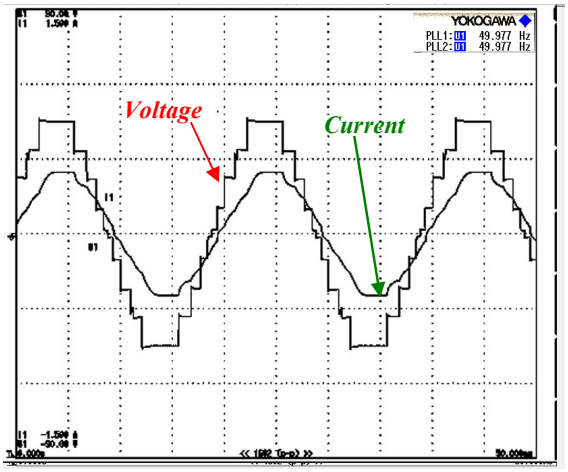


Fig. 9 Experimental output voltage & current waveform

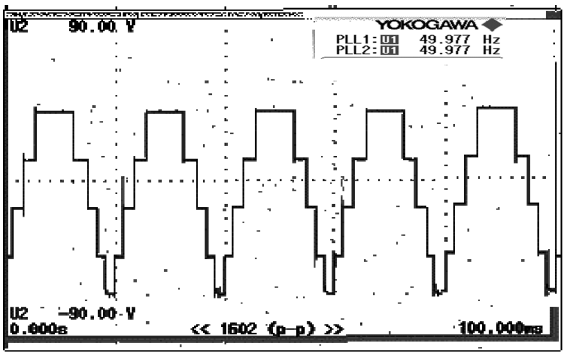


Fig. 10 Experimental level generator output voltage

In [23] presented the novel multilevel inverter topology (named as Reduced Switch Cascaded Multilevel Inverter-RSCMLI) with reduced switch count. In this, simulation based Total Harmonic Distortion (THD) is compared with Conventional Cascaded Multilevel Inverter (CCMLI). For multilevel inverter applications, carrier based PWM techniques with multiple carriers such as (i) Phase Disposition (PD), (ii) Inverted Phase Disposition (IPD), (iii) Phase Opposition Disposition (POD) and (iv) Alternative Phase Opposition Disposition (APOD) are used to generate appropriate PWM signals. These modulation techniques are implemented for different carriers such as the triangular multicarrier wave, saw tooth multicarrier wave and unipolar sine multicarrier wave. In Table III listed the comparison % THD for proposed topology with presented in [23]. In this paper fundamental switching frequency (NLM) method is used. The comparison of fundamental switching technique with other techniques is shown in Table III. In this table all the other PWM strategies are produced high % THD compared to fundamental switching technique. The control block diagram of overall system is shown in Fig. 11.

TABLE III
COMPARISON OF % THD FOR PROPOSED AND OTHER TOPOLOGIES

Topology		CCMLI	RSCMLI	Proposed MLI
Triangular (Switching Frequency 2KHz)	PD	13.75	13.43	-
	IPD	13.80	14.07	
	POD	13.92	13.83	
	APOD	14.04	13.37	
Saw Tooth (Switching Frequency 2KHz)	PD	13.45	13.87	
	IPD	13.45	14.16	
	POD	13.37	13.91	
	APOD	13.22	14.09	
Unipolar Sine (Switching Frequency 2KHz)	PD	14.56	15.79	
	IPD	14.56	13.88	
	POD	15.59	14.14	
	APOD	14.55	14.55	
Fundamental switching Frequency (50Hz)	-	13.80	13.92	9.05

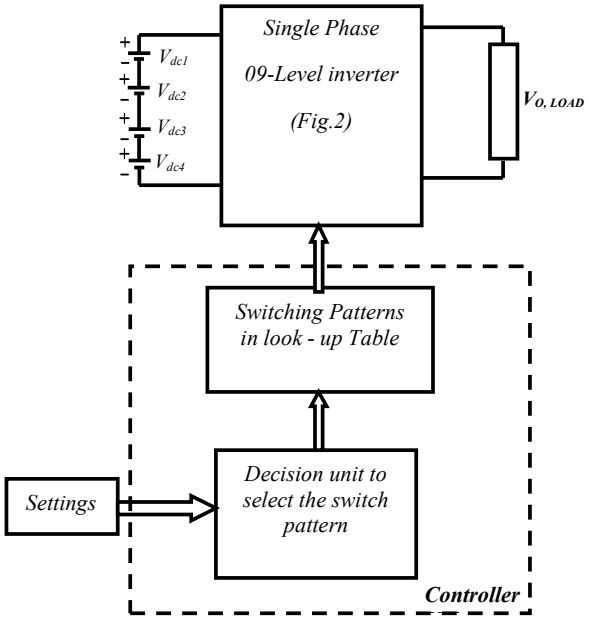


Fig. 11 Control block diagram for proposed method

VI. CONCLUSION

In this paper, the novel symmetric multilevel inverter is proposed. This multilevel inverter can be implemented in industrial where the minimum switches are required. The voltage output and current is verified to confirm the performance of proposed multilevel inverter. The nearest level modulation technique is implemented. Future work on this proposed topology considers: (i). High voltage applications by cascading the proposed topology. (ii) In practical applications such as, Induction motor drives and FACTS controllers.

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