A 24-Bit, 8.1-MS/s D/A Converter for Audio Baseband Channel Applications

N. Ben Ameur and M. Loulou

Abstract—This paper study the high-level modelling and design of delta-sigma ($\Delta\Sigma$) noise shapers for audio Digital-to-Analog Converter (DAC) so as to eliminate the in-band Signal-to-Noise-Ratio (SNR) degradation that accompany one channel mismatch in audio signal. The converter combines a cascaded digital signal interpolation, a noise-shaping single loop delta-sigma modulator with a 5-bit quantizer resolution in the final stage. To reduce sensitivity of Digital-to-Analog Converter (DAC) nonlinearities of the last stage, a high pass second order Data Weighted Averaging (R2DWA) is introduced. This paper presents a MATLAB description modelling approach of the proposed DAC architecture with low distortion and swing suppression integrator designs. The $\Delta\Sigma$ Modulator design can be configured as a 3rd-order and allows 24-bit PCM at sampling rate of 64 kHz for Digital Video Disc (DVD) audio application. The modeling approach provides 139.38 dB of dynamic range for a 32 kHz signal band at -1.6 dBFS input signal level.

Keywords—DVD-audio, DAC, Interpolator and Interpolation Filter, Single-Loop $\Delta\Sigma$ Modulation, R2DWA, Clock Jitter

I. INTRODUCTION

THE explosive growth of DVD-audio has increased the demand for an audio Digital-to-Analog Converter (DAC) to masterfully reproduce the high resolution audio quality of DVD-Audio [1][2][3][4]. This paper introduces an oversampled D/A converter (OSDAC) that meets a great optimization in order to guaranty low power consumption and high-linearity. Digital Interpolation Filters (IF), Delta-Sigma ($\Delta\Sigma$) modulation and Dynamic Element Matching (DEM) are performed in the digital domain. To improve the resolution and decrease out-of-band quantization noise of a signal, one would ideally use a multibit DAC. Multibit DACs, however, have limited linearity and resolution due to mismatch errors. Static mismatch errors occur when each DAC element is driven by slightly mismatched current sources, and static timing errors occur either when the routing to the different DAC elements has unequal electrical lengths, or if the individual DAC elements operate at different speeds. Mismatch shapers, by contrast, are algorithm-based and can shape static and timing DAC mismatch errors away from a frequency of interest. In order to demonstrate the feasibility of

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D/A conversion for a narrow band audio application, an oversampling multibit converter employing single loop digital noise shaping has been designed and modeled on MATLAB/SIMULINK environment.

The use of multibit noise shaping in a D/A converter can place stringent requirements on the subsequent analog reconstruction filtering in order to ensure adequate suppression of out-of-band quantization noise [1][2][4]. In this work, a 5-bit third order single-loop mismatch-shaped $\Delta\Sigma$-modulated DAC that can generate narrowband signals between 28.8 kHz and 35.2 kHz, with less than -144 dB intermodulation distortion in the entire frequency range. Section II focuses on practical aspects of interpolator filter design and implementation. Section III of this paper describes the modulator architecture and the system design considerations of the digital noise-shaping modulator. Section IV discusses second-order dynamic element matching (R2DWA) to address the non-linearity issue. In section V, we briefly discuss the clock jitter effect on performance of D/A conversion. A conclusion is drawn in section VI. These simulations demonstrate that the system meets the specified objectives of a dynamic range of 139.38 dB for a bandwidth of 32 kHz when operated at an output-sampling rate of 8.192 MHz.

Audio DACs [1]-[5] typically consist of four separate processing elements. The input audio data is filtered using an interpolation filter to remove out-of-band images. A Delta-sigma modulator then processes the interpolated data to produce a digital bits stream suitable for conversion into an analogue signal. The digital bits stream is passed to a DAC, and the output of the DAC is then input to an analogue filter to recreate an accurate representation of the music signal. Fig. 1 shows the signal flow diagram of the proposed multibit $\Delta\Sigma$ audio D/A converter. The Digital noise shaping in the proposed converter is accomplished with a single loop, oversampled $\Delta\Sigma$ modulator.
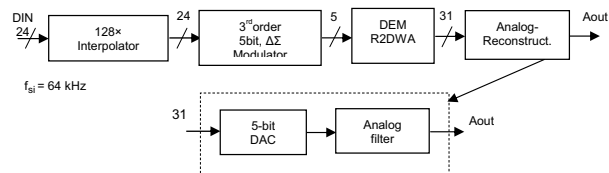

Fig. 1 Multibit delta-sigma DAC signal flow diagram

II. INTERPOLATION FILTER DESIGN AND IMPLEMENTATION

A. Interpolator design

Multirate signal processing [6] consists of using different sample rates within a system to achieve computational efficiencies that are impossible to obtain with a system that operates on a single fixed sample rate. A multirate realization of an interpolation operation is explored, this is a practical approach to the design and implementation of finite impulse response (FIR) filters with narrow spectral constraints. Multirate filters change the input data rate at one or more intermediate points within the filter itself while maintaining an output rate that is identical to the input rate. These filters can achieve both greatly reduced filter lengths and computational rates as compared to standard single-rate filter designs, and thereby provide a practical solution to an otherwise difficult problem.

Multirate FIR filters can leverage many standard FIR filter design methods [7][8]. In the current application of interpolating high resolution digital audio signals, the control of the digital filter parameters to meet certain tolerances is essential. For this reason, the optimum equiripple linear phase filter method is the preferred filter design method. As one of the requirements for proper functionality of the digital pulse-width modulator, a 24-bit digital input signal is to be upsampled 128 times. To obtain the required oversampling ratio (OSR), three separate interpolator stages were designed and performed for an optimum choice of interpolation factors [9], which require a reduced overall computational complexity [10].

Several multirate techniques have been utilized for deriving more efficient interpolator structures. Hence, the impulse response of individual interpolator filters was rewritten into its corresponding polyphase form [10][11]. This is achieved by subdividing the low pass interpolation filter into sub filters according to the upsampling rate OSR=128.

B. FIR filter design method

The Parks-McClellan method, which implements the Remez exchange algorithm, produces a filter design that just meets the design requirements, but does not exceed them. In many instances, when you use the window method to design a filter, the result is a filter that performs too well in the stop band. This wastes performance and taxes computational power by using more filter coefficients than necessary. In summary, the optimum equiripple linear-phase FIR filter design method is used [12]. It is viewed as an optimum design criterion in the sense that the weighted approximation error between the ideal frequency response and the actual frequency response. These filter design solutions are available in MATLAB software. Fig. 2 illustrates the design methods for a given FIR filter order. Fig. 3 shows the passband zoom.
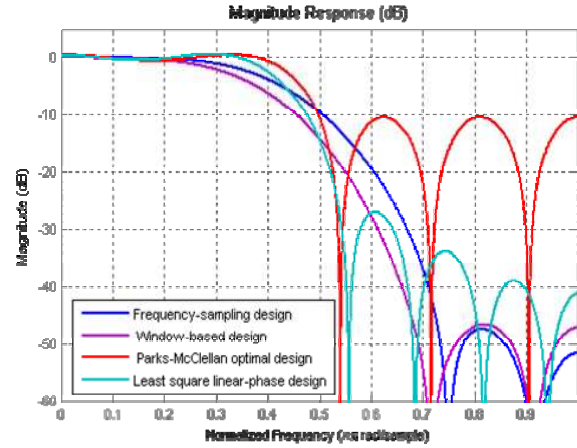

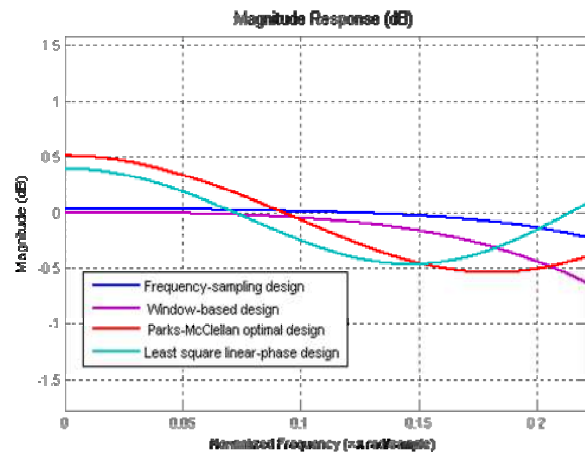Fig. 2 FIR filter design methods frequency responses

Fig. 3 Zoomed passband

The low pass FIR filter-based interpolator design with the specifications to upsample a digital audio signal at a resolution of 24-bit to its new upsampling rate of $OSRf_{si}$ given by Table I was converted to the polyphase filtering structure to efficiently interpolate audio input signals of 24-bit resolution; The polyphase structure provides an efficient architecture for the realization of multirate systems through a bank of filters operating in parallel (Fig. 4). FIR filter have finite impulse response length, it can easily be decomposed into its corresponding polyphase structure. Thus, by using the polyphase representation the transfer function H(z) of the interpolator FIR filter can be written as

$$H(z) = \sum_{k=0}^{OSR-1} z^{-k} H_k z^{OSR} = \left[Nz^{-1} \cdots z^{-(M-1)} \right] \begin{bmatrix} H_0\left(z^{OSR}\right) \\ H_1\left(z^{OSR}\right) \\ H_2\left(z^{OSR}\right) \\ \\ H_{M-1}\left(z^{OSR}\right) \end{bmatrix} \quad (1)$$

TABLE I
INTERPOLATION FILTER SPECIFICATIONS

Passband	28.8 kHz
Stopband	35.2 kHz
Passband ripple	0.00021 dB
Stopband ripple	157.1 dB
Oversampling frequency	8.192 MHz

Fig. 5 depicts the resulting magnitude response of the first interpolator stage where the interpolator FIR filter is realized using its polyphase form. This Figure illustrates, the required 157 dB images and noise attenuation in the stop band range is achieved. To illustrate the design process, we give the resulting magnitude response of the third interpolator stages cascaded in the interpolator chain is illustrated in Fig. 6. This Figure, annotates the stop band attenuation of 157 dB. The actual quantization noise generated by the interpolator chain was also estimated and appropriate system adjustments were performed.
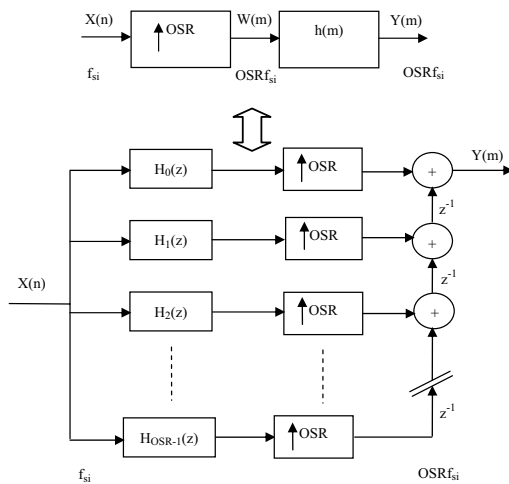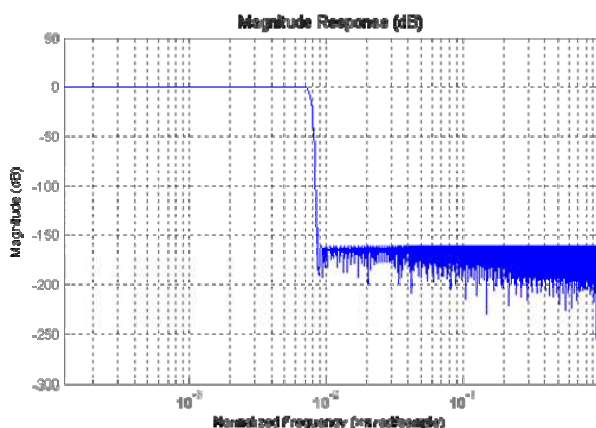

Fig. 4 Polyphase interpolation

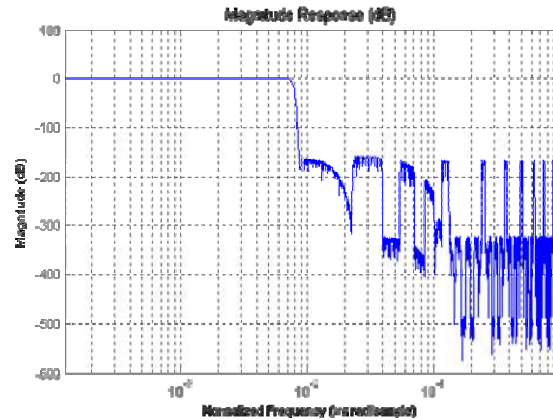Fig. 5 Single stage, FIR filter magnitude response, *OSR* = 128

Fig. 6 Magnitude response of the interpolation chain, *OSR* = 128

C. Computational cost

In order to decrease hardware resources and for an oversampling ratio of value OSR followed by a FIR filter of length N. Without polyphase techniques, each output sample will come directly from the filter, and hence require N multipliers to compute. This implementation requires (N/OSR) multipliers/output sample for FIR filter. The filtering process in the polyphase structure is done at low sampling rate f_{si}, there is therefore no need to first append OSR zeros between consecutive samples, as it is the case for direct form implementation. Each $H_i(z)$ component filter consists of delayed OSR^{th} samples of length N/OSR from the original filter, and hence (OSR.N)/OSR = N multipliers are required. To investigate the properties of these individual polyphase filters; to gain further insight into the operation of the polyphase structure; each output point passes through an oversampling factor of value OSR, generating OSR output points. These output points pass through delay elements and an adder, to produce the final sequence of OSR output samples. In terms of computation, we require N total multipliers to produce OSR output points, and hence the computational cost is reduced to (N/OSR) multiplies/output sample for FIR polyphase filter.

A comparative summary of the single-rate and three-stage multirate design in terms of multiply-accumulate operations per second (MAC) [13][12] are given in Table II. Assuming that one MAC operation is required per pair of symmetric filter coefficients, the required computational rate is N/2 MACs/sample * 8.192 Msamples/sec (MMACs/sec). Note that the three-stage design is further improved (shorter filters and reduced computational cost) by optimizing the choice of interpolation factors.

TABLE II
COMPARISON OF SINGLE- AND MULTIRATE FILTER IMPLEMENTATIONS FOR A 32 KHZ LOW PASS FILTER OPERATING AT A 64 KHZ INPUT RATE

Design technique	Total FIR coefficients	Computational (MMACs/sec)
Single-stage interpolation	9063	290.016
Three-stages interpolation	325	41.408

958

III. NOISE-SHAPED D/A CONVERSION

In this section, we explore the intensive research on design approaches and architectures that can be used to implement a ΔΣ modulator for audio application. A main issue should be concerned: which is the selecting the best architecture given the audio system specifications. A trade-off between bandwidth (BW), dynamic range (DR) and power consumption (Pd) for ΔΣ D/A converters must be achieved. A best-case estimation of this trade-off can be derived from the Figure-Of-Merit [5][1]-[4] given by equation (1)

$$FOM = \frac{P_d}{DR \cdot (2 \cdot BW)} \tag{2}$$

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right) \cdot OSR^{2L+1} \cdot \left(2^B - 1\right)^2 \tag{3}$$

To achieve a given dynamic range (equation (2)), three degrees of freedom had to be considered: the oversampling ratio (OSR), the order of noise shaping (L) and the internal quantizer resolution (B). Given the low input bandwidths of a ΔΣ D/A converter, it is necessary to increase the sampling frequency as well as to increase the oversampling ratio (OSR). However, it is necessary to reduce in-band quantization noise power to preserve performance at a higher order of the modulator L [14][15]. A low FOM can be achieved through a proper system design which requires a suited architecture and a proper choice of the implementation method, optimizing the architecture parameters and optimizing for power all building blocks.

A novel modulator structures are needed to alleviate the reduction of resolution in audio applications. In these structures the signal transfer function (STF) is unity and have many advantages such as the followings. First, that they are insensitive to the current mismatch. Second, the dynamic range is increased because the quantizer tracks the input signal through a direct path to the its input. Third, the integrators need small output swings since only the quantization noise is processed by them. Fourth, analog post filtering requirements are relaxed, because of the smaller out-of-band quantization noise. By using a high-order noise transfer function combined with multibit quantizer in the final stage, it is possible to achieve a high SNR at a given OSR. Besides these improvements, the single-loop multibit ΔΣ modulators offer an improved stability.

The disadvantage of multibit quantization is the necessity of dynamic element matching (DEM) to correct nonlinearity in the internal multibit DAC. Therefore, the overall ΔΣ converter linearity and resolution are limited by the precision of the multibit DAC. Many dynamic element matching (DEM) techniques have been proposed to improve the accuracy of the D/A converter. The best FOM has been obtained with high performance narrowband third-order single-loop 5-bit ΔΣ modulator with an OSR of 128. To reach the required specifications, a 3rd-order single-loop 5-bit ΔΣ modulator with feedback signal path was chosen.

A. System Level Architecture

The proposed Chebychev 3rd-order CRFB (Cascade-of-resonators, feedback form) single-loop multibit ΔΣ modulator shown in Fig. 7.a, which has a large input range and low integrator output swings, is used in our design. Fig. 7.b shows the Butterworth 3rd-order single-loop multibit ΔΣ modulator. The operations are performed with floating point numbers.

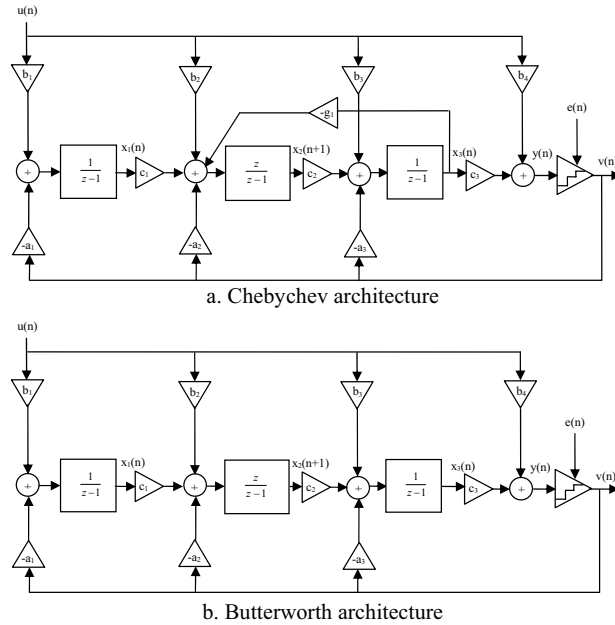a. Chebychev architecture

b. Butterworth architecture

Fig. 7 3rd-order multibit delta sigma modulators

By applying linear analysis to the architecture shown in Fig. 7.a, it can be seen that the modulator output in "z" domain is given by

$$V(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \tag{4}$$

The signal transfer function is a unity-gain, STF(z)=1 and the noise transfer function for L=3, NTF(z) is

$$NTF(z) = \frac{(z-1)^2 G(z)}{D(z)} \tag{5}$$

$$G(z) = z - 1 + g_1$$

$$D(z) = (z-1)^2(z-1+g_1+a_3c_3) + a_2c_2c_3z(z-1) + a_1c_1c_2c_3$$

In which D(Z) is 3rd-order polynomial, G(z) is the function of optimal complex-conjugate pairs of zeros. The imposed G(z) results in a flat band response at low frequency and ripples at the stop band of the signal. Thus, NTF can be improved by placing notches in the signal band for further shaping of the quantization error, while preserving its flat out-of-band gain, and therefore, the modulator stability [14]. The

selection of coefficients offers a stable converter with a high resolution of 151.7dB for an oversampling ratio of 128. All the zeros of the noise transfer function are placed at z=1 and the coefficients values were optimized to guarantee that the baseband quantization noise is independent of the input signal and for generating the maximum peak SNDR. The poles and zeros locations are shown in Fig. 8.
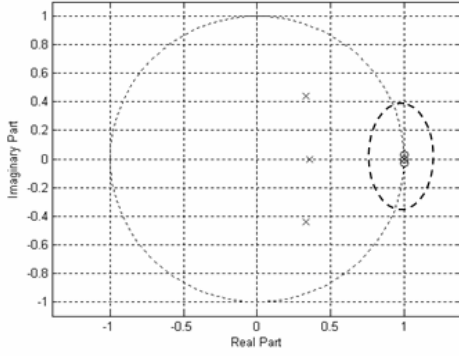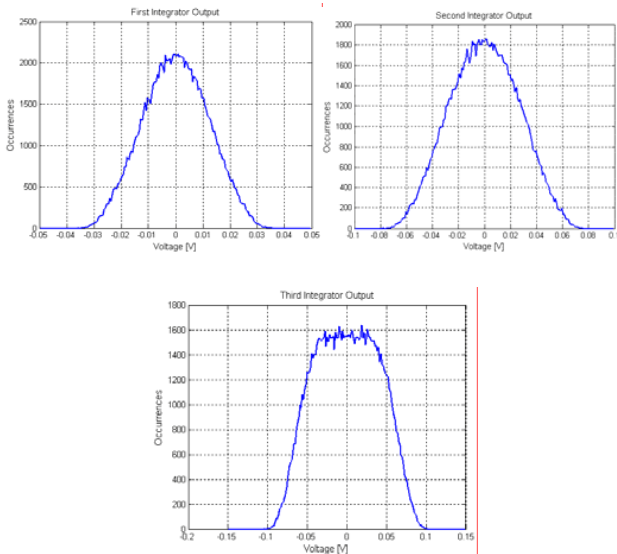

Fig. 8 Pole/zero plot

Fig. 9 Integrator output swings

B. Delta-Sigma topology with improved FIR NTF

By replacing two zeros in the NTF with one pair of complex-conjugate zeros, the theoretical achievable signal-to-quantization noise ratios of delta sigma modulators with pure FIR filter characteristics can be increased. The corresponding NTF for L≥2 becomes [15]

$$NTF\ (z) = \left(1 - z^{-1}\right)^{L-2}\left(1 - \xi\ z^{-1} + z^{-2}\right) \tag{6}$$

$$\xi = 2\ cos\ \left(2\left(f_0 / f_{si}\right)\right)$$

Where, f_0 and f_{si} are the notch frequency and the sampling frequency, respectively. The optimal placement of the notch frequency is at approximately

$$f_0 = \sqrt{(2L - 3)/(2L - 1)}\ f_{BW} \tag{7}$$

Where f_{BW} is a bandwidth frequency and L is a modulator order. The signal-to-noise-ratio improvement corresponds to a factor of $(L-0.5)^2$ compared to the case, in which all zeros of the NTF are at DC. For implementing stable 3rd-order NTFs, the NTF response of a Butterworth filter for different upsampling factors are shown in Fig. 10. Note that the X-axis is normalized to the sampling frequency. The NTF curve of Butterworth configuration shows a very poor attenuation of the quantization noise at high frequencies and is independent of OSR, since its pole locations do not depend on the OSR. With the inverse-Chebyshev filter, the zero-locations can be optimized with various OSRs. Thus, the NTF curves can be obtained, each with notche in the signal band (Fig. 11). Notches will considerably reduces |NTF(f)| at its upper edge. That, the existence of notche will cause faster decay at its upper edge of the |NTF(f)|; this, and in turn, the in-band error power. The in-band error power is reduced up to about 18 dB, for each case of OSR of 16, 32, 64 and 128, by spreading the zeros over the band in an optimum way [3]. However, the in-band noise attenuation of both alternatives is poor, not only at low frequencies but also at high frequencies, in comparison with the theoretical NTF with all zeros at DC. For each |NTF|, the average Root-Mean-Square (RMS) attenuation over the signal band is summarized in Table 3.
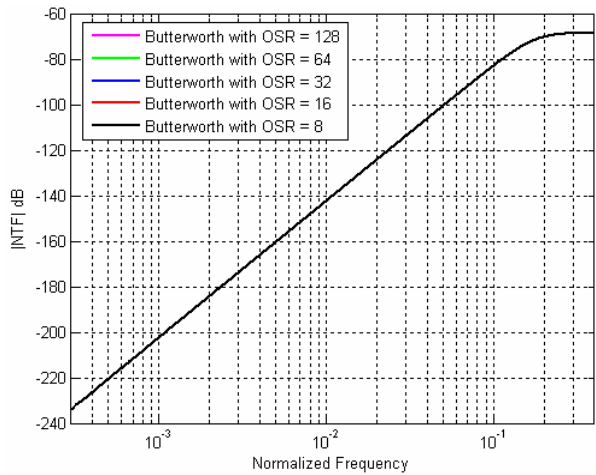
Fig. 10 The magnitude responses of the 3rd -order NTFs of Butterworth filter with various OSR
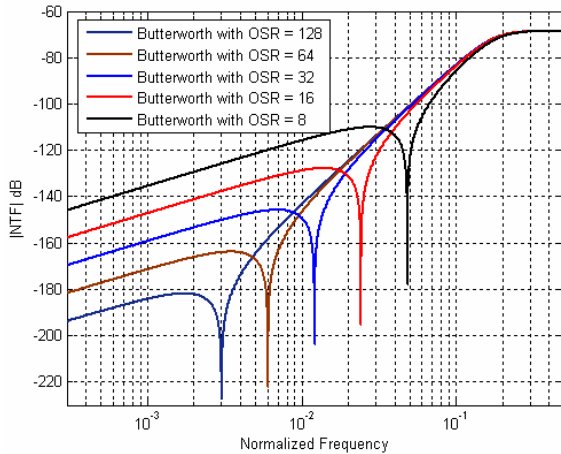
Fig. 11 The magnitude responses of the 3rd -order NTFs of Iinverse- Chebyshev filter with various OSR

TABLE III
SUMMARY OF THE AVERAGE ROOT-MEAN-SQUARE (RMS) ATTENUATIONS OVER THE SIGNAL BAND FOR VARIOUS 3RD–ORDER |NTFS|

RMS|NTF| dB NTF	OSR of 8	OSR of 16	OSR of 32	OSR of 64	OSR of 128
Butterworth filter	-22.0 dB	-40.1 dB	-58.4 dB	-76.3 dB	-94.4 dB
Inverse-Chebyshev filter	-32.0 dB	-49.8 dB	-68.1 dB	-86.2 dB	-104.3 dB
Ideal with all zeros at DC	-42.46 dB	-60.49 dB	-78.54 dB	-96.6 dB	-114.7 dB

Fig. 12 shows the frequency responses of various types of 3rd-order NTF, where the 3rd-order NTF with relaxed hors-band gain value of three is applied for the single-loop one. We found that the proposed in-band noise shaping provides the better attenuation of quantization noise than Butterworth topology.
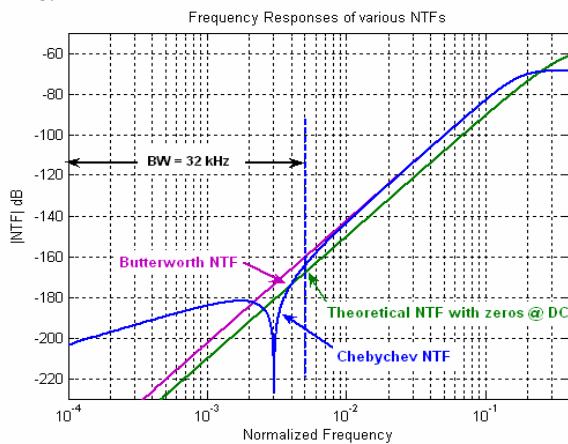

Fig. 12 The output spectra and frequency responses of various 3rd-order NTF's

Fig. 13 shows the spectrum of the 3rd-order low-distortion architectural scheme with the Chebychev NTF. The results of the modulator modelling showed that when a sound signal

frequency band is of 32 kHz the modulator's effective number of bits is 24, while the quantization noise power is minus 151.7dB. Unlike the Butterworth architectural scheme, this topology demonstrates higher attenuation of the quantization noise at the in-band frequencies due to the deep notch. The SNR is improved about 10 dB in comparison with the Butterworth 3rd-order modulator with all zeros at DC [17]. Indeed, the key advantages of the topology include: higher signal-to-quantization-noise ratios at high modulator order, decreased circuit complexity, improved robustness to modulator coefficient variations and reduced power dissipation [17].
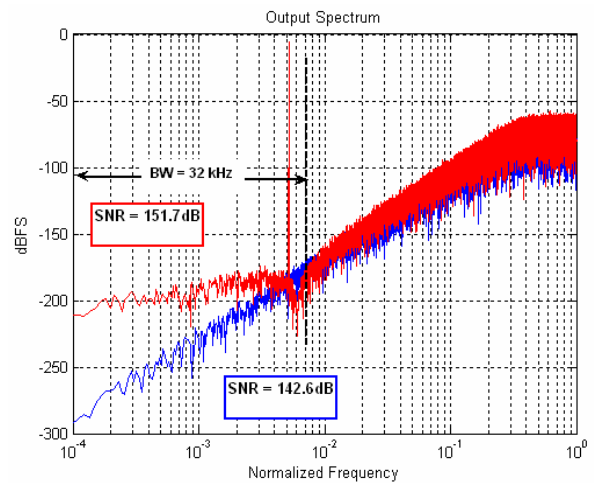

Fig. 13 The ideal output spectra of various ΔΣ modulators

For an actual implementation, it is necessary to ensure the stability of the delta-sigma modulator; that the multibit quantizer is not overloaded at any time. A_χ is defined as the ratio between the maximum amplitude of the input sinewave signal and the quantizer's reference voltage, to guarantee that the quantizer will never be overload, a sufficient condition, [18], can be expressed as

$$A_\chi \leq 1 - \frac{\|ntf\| - 2}{2^B - 1} \qquad (8)$$

Where $\|ntf\|$ is the norm of the impulse sequence ntf(n) for the noise transfer function NTF(z), B is the bit number of the quantizer. For the 3rd-order FIR NTF in Eq. (5) it exists

$$\|ntf\| = \sum_{n=0}^{\infty} |ntf(n)| = 2(2 + \gamma) \qquad (9)$$

With STF=1, the out-of-band spectral components are reduced due to the lack of input signal in the integrators of the loop-filter, therefore the stability of the delta sigma modulator is improved.

The evaluation of the performance of the proposed modulator has been done with MATLAB/SIMULINK

software. In the first time, we have simulated the SNR as a function of the relative input magnitude of the 3rd-order modulator using ideal 5-bits DAC. It was found, as shown in Fig. 14, that the proposed modulator achieves the target SNR of 157.1dB at -1.6 dBFS input level. This performance is limited by the non-ideality of the DAC. In deed, the use of non-ideal 5-bit DAC in the same architecture shows clearly that mismatch of the unit elements of the DAC can completely degrade the SNR.
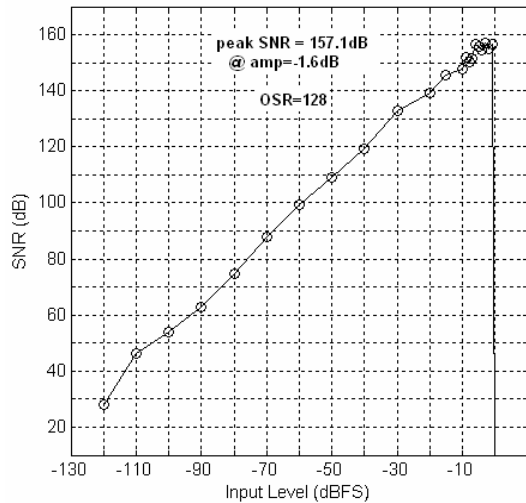

Fig. 14 Ideal SNR vs. input amplitude curve

IV. MATCHING REQUIREMENTS

In-band noise resulting from mismatch among the current sources in D/A converter is suppressed with a dynamic element-matching scheme. A simple high pass Data Weighted Averaging (DWA) scheme should be used to implement the dynamic element matching. The DWA algorithm introduced in [15] is used. As depicted in Fig. 15.b. The code is converted to thermometer code, shown in Fig. 15.a. The algorithm cycles through the DAC elements by sequentially selecting the elements based upon the input data. Through such rotational element-selection process, DWA achieves first-order high-pass shaping of the DAC mismatch errors [19],[20]. As shown in Fig. 16, on the oneside, DWA technique produces harmonic tones that degrade the SFDR, on the other side, the harmonic distortion has been turned into white noise, part of the noise energy falls inside the passband, and the overall SNR is reduced.
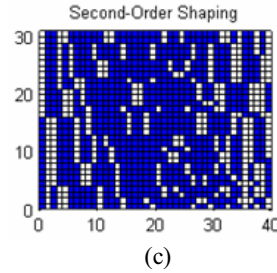

(a)   (b)

(c)
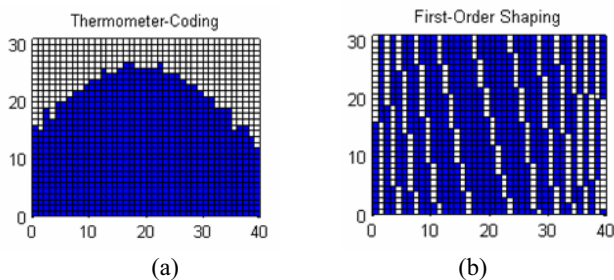
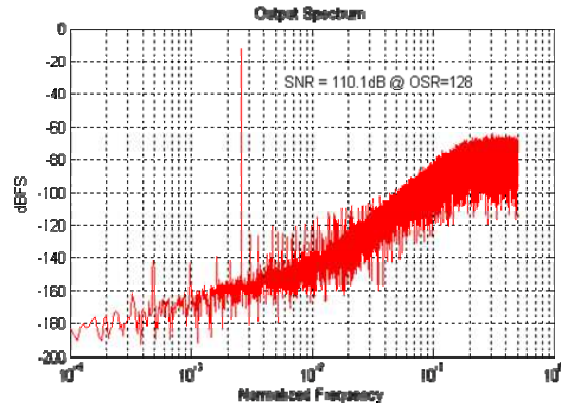Fig. 15 Thermometer-Coding and DWA element selection algorithm

Fig. 16 Illustration of tones behavior of DWA

In order to intuitively compare the impact of mismatch unit elements of the DAC on D/A conversion, the Fig. 17 illustrates the PSD curves at OSR of 128 for different σ_I of current mismatches. In the simulation examples, for a 4-bit loss in DR, σ_I should be smaller than 0.01% at OSR of 128 for single-loop one as shown in this Figure.
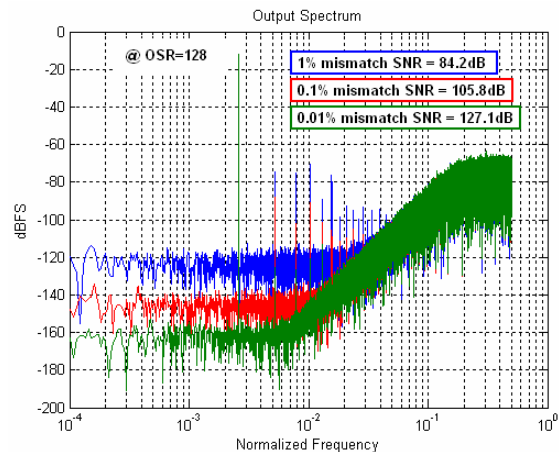

Fig. 17 PSD of the single loop (5-bit) at OSR of 128 for different current mismatches

To produce a low-distortion device, Second-order dynamic element matching (DEM) is used to address the non-linearity issue. Therefore, it is called the restricted second order DWA (R2DWA) DEM. The algorithm is depicted in Fig. 15.c. The

R2DWA DEM allows the DAC to convert a modulator output in one cycle instead of two. This means that DAC elements can be clocked with the same clock as the modulator, and each DAC element only samples two currents, making individual element contribution inherently linear [20]. This linearity is essential to produce second-order noise shaping, which makes the R2DWA DEM hard to implement. The R2DWA DEM offers superior performance compared to the first-order DWA. It allows analog circuits to dominate the overall performance. As a result, a flat noise floor over the 32 kHz band and an improved SNR about 18 dB for 0.1% σ_I current mismatch. In the simulation examples, for a 0.2-bit loss in DR, σ_I should be smaller than 0.1% at OSR of 128 for single-loop one as shown in Fig. 18.
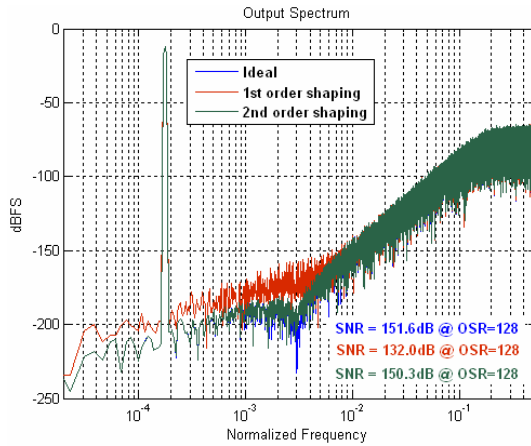

Fig. 18 Comparison between DWA and R2DWA for 0.1% current mismatch

V. DAC SAMPLE-JITTER SUSCEPTIBILITY

A. Audibility of sample-jitter

In the design of digital audio systems, the problem of jitter in the sampling interval was an overlooked factor. The clock jitter can be defined as a short-term, non-cumulative variation of the switching instant of a digital clock form its ideal position in time [21]. It results in a non-uniform sampling time sequence, and produces an error, which increases the total error power at the quantizer output. The error introduced when a sinusoidal signal x(t) with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given by

$$x\left(t+\delta\right)-x\left(t\right) \approx 2\pi\, f_{in}\, \delta A \cos\left(2\pi\, f_{in}\, t\right) = \delta\, \frac{d}{dt} x\left(t\right) \qquad (10)$$

This error can be modeled at the behavioural level as shown in Fig. 19 [22], which implements (9). The input signal x(t) and its derivative du/dt are continuous-time signals. They are sampled with sampling period T_{si} by a zero-order hold. In the model, we assumed that the sampling uncertainty δ is a Gaussian random process with standard deviation Δτ

(available in SIMULINK). Whether oversampling is helpful in reducing the error introduced by the jitter depends on the nature of the jitter. Since we assume the jitter white, the resultant error has uniform power-spectral density (PSD) from 0 to $f_{si}/2$, with a total power of $(2\pi f_{in}\Delta\tau A)^2/2$. In this case, the total error power will be reduced by the high oversampling ratio [21].
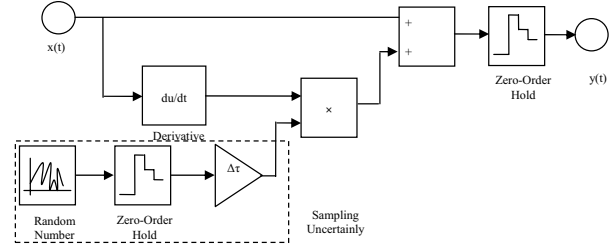

Fig. 19 Modeling a random sampling jitter

When oversampling with a factor 128 we increase the number of pulses by 128, but reduce the sample-to-sample amplitude difference with the same factor. Since the jitter error is a skew of the pulse width, we will concurrently have the same process applied to this. For random jitter, this means the jitter energy is the same, but its spectrum is spread over $128.f_{si}/2$ instead of $f_{si}/2$. Since the frequencies above $f_{si}/2$ are filtered away at the DAC output, the jitter error will ideally decrease with a factor 128. The PSD of the ideal case have a slope of 60dB/decade that indicates a third-order noise shaping of the quantization noise over a narrow band of frequency. Fig. 20 shows a plot of the jitter effect spectrum with a 1.4375 kHz full-scale input signal and 50 ns sampling jitter. The resolution of the data is 24-bits and the sampling frequency is 64 kHz. As we can see from the Figure, the noise floor increases as the jitter increases and consequently a signal-to-noise-ratio degradation. Fig. 21 illustrates the effects of jitter error on SNR of a third-order Delta-Sigma modulator. We can see that the audibility threshold decreases from 50 ns at high SNR to as little as 1 μs at 61dB. Low sample-jitter on the other hand is much more audible.
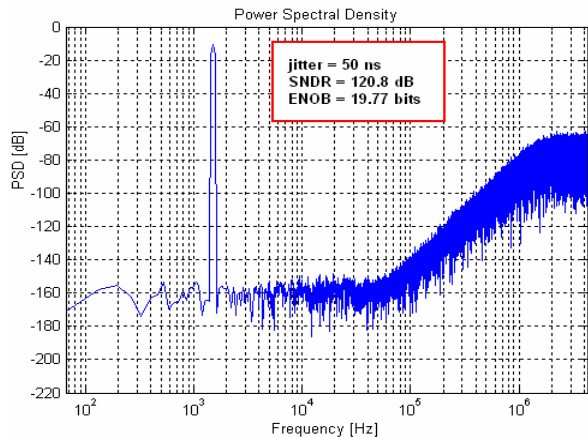

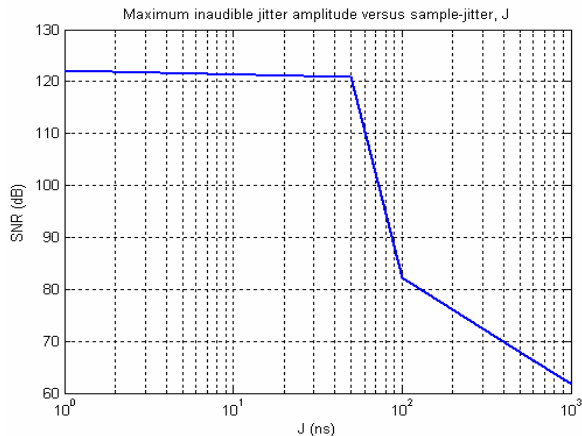Fig. 20 Jitter error effect on PSD of third-order modulator

Fig. 21 SNR vs sample-jitter

VI. CONCLUSION

In this paper, we have presented the design and a model approach on MATLAB of the digital part of the proposed ΔΣ DAC.

For interpolation filters design, we see that well-balanced distributions provide the lowest computational requirements and increased integration in systems, which is driven by continuous demand for lower total cost. This pushes more processing circuitry into digital SOCs.

For ΔΣ modulator design, we can exhibit instability, idle-tones, dynamic errors and jitter sensitivity. This is especially a problem with 1-bit output but the problem is solved with converge towards multibit ΔΣ modulators with dynamic element matching. DAC errors are not shaped by the delta-sigma modulator and need to be extremely low. Therefore, a 2nd-order mismatch shaping is complex, but performs much better correction.

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