

# A 1.8 V RF CMOS Active Inductor with 0.18 um CMOS Technology

Siavash Heydarzadeh, Massoud Dousti

**Abstract**—A active inductor in CMOS technology with a supply voltage of 1.8V is presented. The value of the inductance L can be in the range from 0.12nH to 0.25nH in high frequency(HF). The proposed active inductor is designed in TSMC 0.18-um CMOS technology. The power dissipation of this inductor can retain constant at all operating frequency bands and consume around 20mW from 1.8V power supply. Inductors designed by integrated circuit occupy much smaller area, for this reason, attracted researchers attention for more than decade. In this design we used Advanced Design System (ADS) for simulating circuit.

**Keywords**—CMOS active inductor , 0.18um CMOS technology , ADS

## I. INTRODUCTION

COMS active inductors have found increasing applications in areas where an inductive characteristic is required. These applications include LC oscillators, RF bandpass filters, RF phase shifters, RF power dividers and ultra wideband low noise amplifiers [1]. Although the performance of monolithic integrated inductors in CMOS process has enjoyed a great progress, the large space occupied by the spiral inductors and the conductive substrate, has made passive inductors an improbable option to be employed in designing high-frequency circuit in which the use of multiple inductors is requisite[2]. An active inductor typically occupies 1-5% of the silicon area of a passive inductor. Some disadvantages of using active inductors, compared to spiral inductors that limit their use in RFIC and MMIC designs, are higher noise, nonlinear behavior, power dissipation, sensitivity to process, and voltage and temperature variations [3]. The active inductor presented here provides high value, least area occupation, insensitive to temperature and low power consumption.

## II. ACTIVE INDUCTOR CIRCUITS

Researchers have introduced different kinds of circuits for active inductors. Some of these circuits are shown in Fig. 1, Fig. 2 and Fig. 3 [4],[5],[6]. The value of small-signal equivalent elements are obtained with equations (1) to (7).

For figure one:

$$C1 = C_{gs1} \quad (1)$$

$$R1 = \frac{1}{g_{o2}} \parallel \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}}$$

$$R2 \approx \frac{g_{o1}}{g_{m1} \cdot g_{m2}}$$

$$L1 = \frac{C_{gs2} + C_{gd2} + C_{gd1}}{g_{m1} \cdot g_{m2}}$$

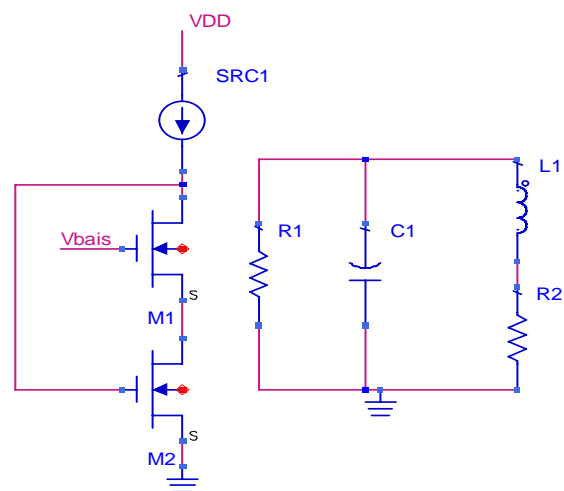


Fig. 1 Active inductor and small-signal equivalent

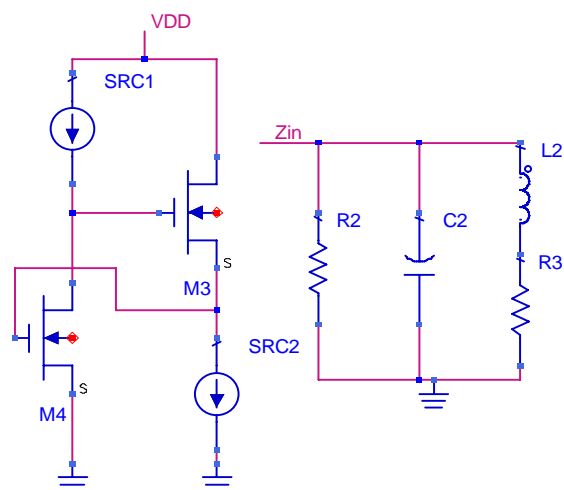


Fig. 2 Simple active inductor and equivalent circuit

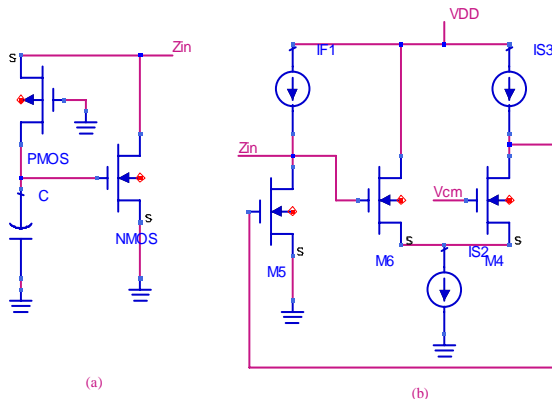


Fig. 3 (a) - Adan active inductor circuit (b)-Xiao active inductor circuit

For figure two:

$$R2 = \frac{1}{g_{ds3} + g_{m4}} \approx \frac{1}{g_{m4}} \quad (5)$$

$$L \approx \frac{C_{gs3}}{g_{m4} \cdot g_{m3}} \quad (6)$$

For figure three (a):

$$Z_{in} \approx \frac{SC}{g_{mp} \cdot g_{mn}} \quad (7)$$

### III. ACTIVE INDUCTOR SPECIFICATION

From among these active inductor circuits, figure one is selected and illustrated. The active inductor in Fig.1, as compared to other topologies, could use biasing current more proficiently. Because of using shunt feedback at the input node, the impedance is low where frequency is low. When the frequency is high enough, the gate-source capacitance will result in the drop of the feedback loop gain, the input impedance will raise with frequency. Simple structure and low noise are the most important advantages of this circuit. The active inductor in Fig.1 can work better in high frequency as compared to Fig.2 [7]. Figure 4 shows the complete circuit of inductor that simulated.

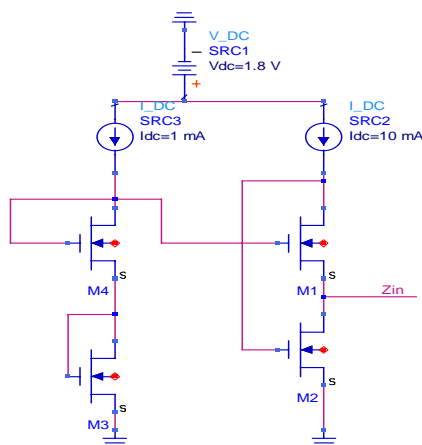


Fig. 4 The complete circuit of active inductor

Table I is presented transistors dimensions which utilized in active inductor circuit (Fig.4).

TABLE I  
TRANSISTORS DIMENSIONS

PS	L ( $\mu\text{m}$ )	W ( $\mu\text{m}$ )	AD ( $\text{pm}$ )	AS ( $\text{pm}$ )	PD ( $\mu\text{m}$ )	( $\mu\text{m}$ )
M1-M2	0.18	250	120	120	501	501
M3-M4	0.25	600	288	288	1201	1201

AD: drain diffusion area

AS: source diffusion area

PD: Perimeter of the drain junction

PS: perimeter of the source junction

$$AD = AS \cong W \times L_s \quad (8)$$

$$PD = PS \cong 2W + 2L_s \quad (9)$$

$L_s$  in equation (8), (9) depends on technology. For 0.18U COMS process  $L_s = 0.48 \mu\text{m}$ .  $L_s$  is  $0.55 \mu\text{m}$  for 0.13U CMOS process.

### IV. SIMULATION RESULTS

Table II shows the important parameters of transistors which related to bias. These parameters determine the value of inductor (L) as we mention above.

TABLE II  
TRANSISTORS PARAMETERS

	$g_m$ (mv)	$V_{gs}$ (mv)	$V_{ds}$ (mv)	$I_d$ (mA)	$V_{ds,sat}$ (mv)	$V_{th}$ (mv)	region
M1	80	667	367	10	130	503	sat
M2	57	600	232	5.3	104	495	sat
M3	20	462	462	1	57	499	sat
M4	20	437	437	1	57	473	sat

The numbers in Table II, have obtained from ADS report. Figure 5 shows the imaginary part of input impedance ( $\text{imag}(Z_{in})$ ). The frequency range of simulation is included 1GHz to 6 GHz.

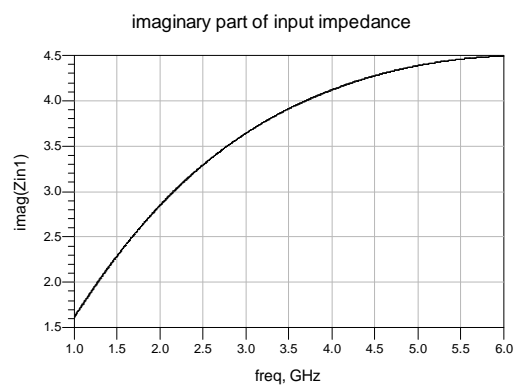


Fig. 5 Imaginary part of input impedance( $\text{imag}(Z_{in})$ ).

Input impedance smith chart is shown in Fig.6. Figure 7 represents the real part of input impedance ( $\text{real}(Z_{in})$ ) which is

related to dissipation resistance (R2 in Fig.1). S11 parameter is displayed in Fig. 8 .

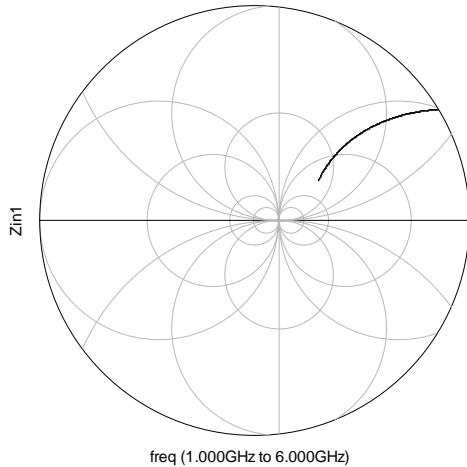


Fig. 6 Input impedance(Zin)

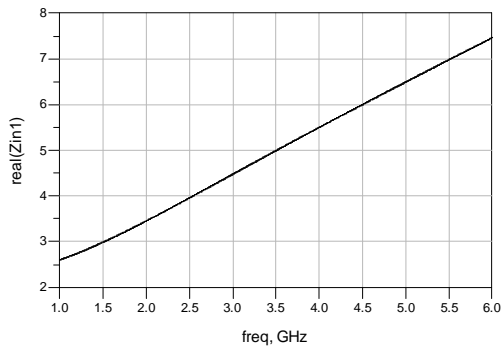


Fig. 7 real part of input impedance(real(Zin))

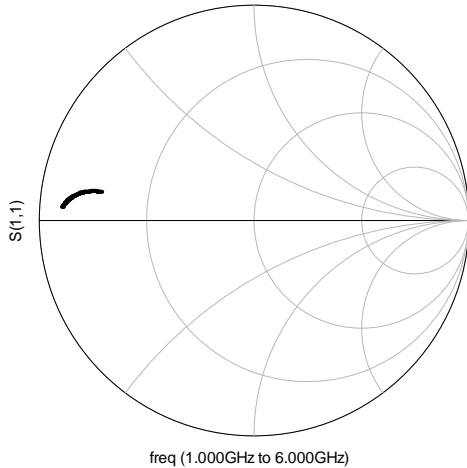


Fig. 8 S11 parameter after simulating cicuit

$$g_m = \sqrt{2 \cdot K' \cdot I_d \cdot \left(\frac{w}{l}\right)} \quad (10)$$

According to equation (4) and (10):

$$L \propto \frac{1}{g_{m1} \cdot g_{m2}} \quad (11)$$

$$g_{m1}, g_{m2} \propto \sqrt{I_{d1} \cdot I_{d2}} \quad (12)$$

$$L \propto \frac{1}{\sqrt{I_{d1} \cdot I_{d2}}} \quad (13)$$

Figure 9 displays the effect of temperature on drain source currents (Temperature VS  $1/\sqrt{I_{d1} \cdot I_{d2}}$ ). This figure represents that temperature changing won't effect on inductor value(L).

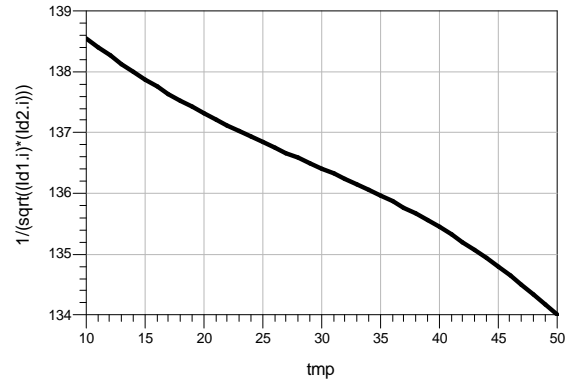


Fig. 9 Temperature effect on drain source currents

Inductor value (L) which obtained from equation (14) is displayed in Fig.10 .

$$\text{imag}(Z_{in}) = 2\pi fL \rightarrow L = \frac{\text{imag}(Z_{in})}{2\pi f} \quad (14)$$

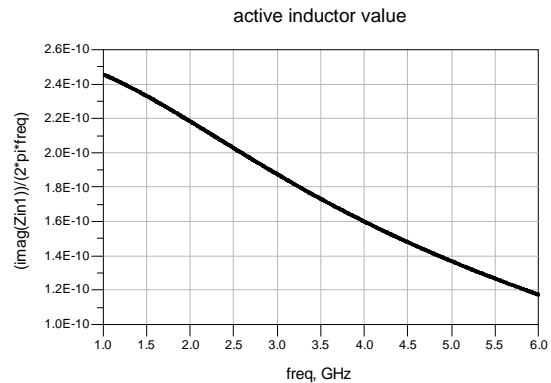


Fig. 10 Active inductor value (L)

Active inductance layout shows in figure 11. Using cadence software and 0.18um CMOS technology to produce this layout. The least area consumption are utilized.

## V.CONCLUSION

A 0.18 um CMOS active inductor with 0.12nH to 0.25nH value in high frequency was presented. The design has the capability of independent inductance value in different temperature. It consumes less than 20mW power form 1.8V power supply. The active inductor simulated in this paper had less than 8Ω loss resistance as Fig.7 showed. We used TSMC RF 0.18 um CMOS technology in simulating.

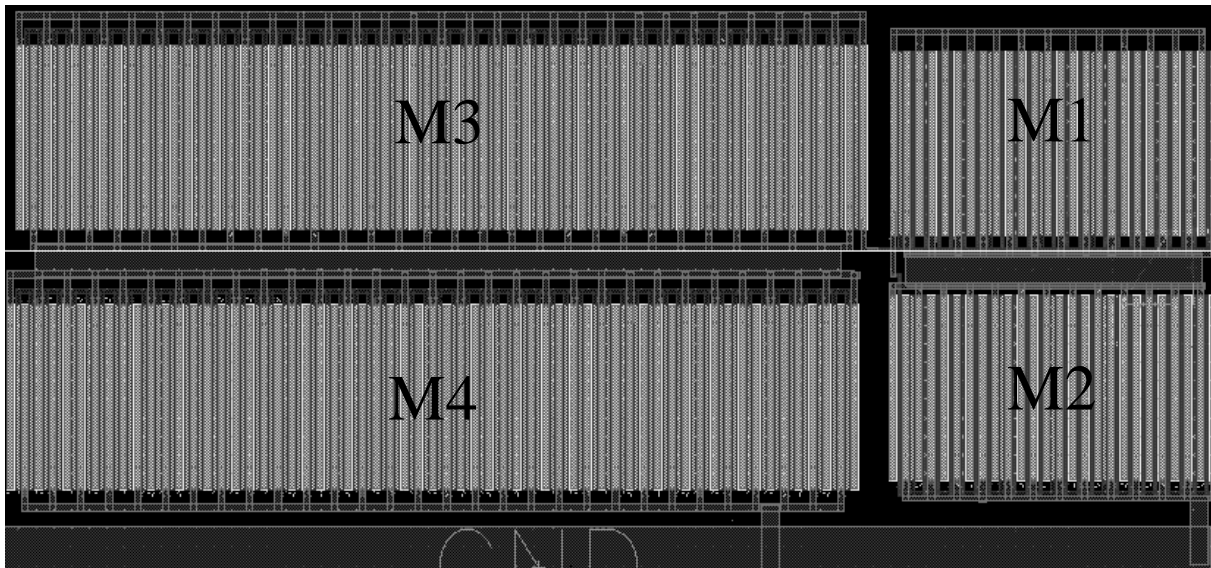


Fig. 11 Active inductance cadence layout with 0.18um technology

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