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A 1.2-ns16×16-Bit Binary Multiplier Using High Speed Compressors

A. Dandapat, S. Ghosal, P. Sarkar, D. Mukhopadhyay

***Abstract*—**For higher order multiplications, a huge number of adders or compressors are to be used to perform the partial product addition. We have reduced the number of adders by introducing special kind of adders that are capable to add five/six/seven bits per decade. These adders are called compressors. Binary counter property has been merged with the compressor property to develop high order compressors. Uses of these compressors permit the reduction of the vertical critical paths. A 16×16 bit multiplier has been developed using these compressors. These compressors make the multipliers faster as compared to the conventional design that have been used 4-2 compressors and 3-2 compressors.

***Keywords*—**Binary multiplier, Compressors, Counter, Column adder, Low power.

I. Introduction

IN recent years, power consumption, as well as area and speed, are the most important issues in VLSI design. Pass-transistor logic has been intensively studied as a breakthrough for high-speed and low-power digital circuits. Most modern arithmetic processors are built with architectures that have been well-established in the literature, with many of the latest innovations devoted to special logic circuits and the use of advanced technologies. Specifically, the design of multipliers is critical in digital signal processing applications, where a high number of multiplications are required.

Multipliers require high amount of power and delay during the partial products addition. At this stage, most of the multipliers are designed with different kind of adders that are capable to add two/three or at most 4 bits by using 4-2 compressors [1, 2]. For higher order multiplications, a huge number of adders or compressors are used to perform the partial product addition. We have minimized the number of adders by introducing different compressors. Binary counter property has been merged with the compressor property to develop high order compressors such as 5-3, 6-3 and 7-3 compressors [3].

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A. Dandapat is with the Department of Electronics and Telecommunication Engg., Jadavpur University, Kolkata, WB 700032, INDIA, phone: 91-33-2414-6217; fax: 91-33-2414-6217; e-mail: anup.dandapat@gmail.com.

S. Ghosal was with Jadavpur University, Kolkata-700 032, INDIA. He is now with the Department of Electrical engineering. Indian Institute of technology, Madras, INDIA. e-mail: sayanghosal@yahoo.co.uk

P. Sarkar was with the Electronics & Telecommunication Engineering Department, Jadavpur University, Kolkata 700 032, INDIA. He is now in ST Micro-electronics, India. e-mail: pikulsarkar@yahoo.com.

D. Mukhopadhyay was with the Department of electronics & Telecommunication engg., Jadavpur university, Kolkata-700 032, INDIA. He is now with the Electrical Engg. Department, Institute of Engineering and Management, Kolkata, INDIA. e-mail: dmukho@yahoo.com.

II. Conventional COMPRESSOR ALGORITHM

So far 4-2 and 5-2 compressors are reported. The conventional 4-2 compressor structure actually compresses five partial product bits into three [1, 2]. The architecture can be implemented with two stages of full adder (FA) connected in series as shown in Fig. 1. The outputs of 4-2 compressor consist of one bit in position j and two bits in position (j + 1). This straight forward approach has four XOR gate delays [4].

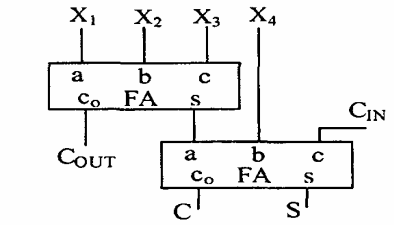

Fig. 1 Conventional 4-2 compressor

An attractive implementation using XOR gates and MUX is described in [5, 6]. This implementation is better and the delay is that of three XOR gates delays. With the similar logic 5-2 compressor is also designed in [7].

The problems of this kind of conventional compressor are:

(i) The uneven delay profile of the outputs arriving from different input paths tends to generate a lot of glitches.

(ii) Compressors do the simple operation of addition that adds more number of bits at a time. But the conventional 4-2 compressors require one more half adder of which two inputs are 'C_{OUT}' and 'C' (shown in Figure 2), to produce the final addition result. Example: if X1=X2=X3=X4=1 and C_{IN} =0 (in Figure 1) then the addition result be four i.e 100 but the conventional architecture produces C_{OUT}=1, C=1 and S=0. Now if C_{OUT} and C fed to a half adder then it produces the final result in exact form as shown in Figure 2.

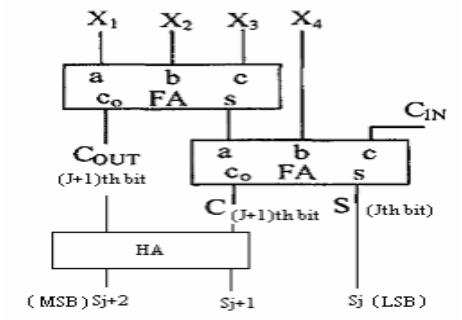

Fig. 2 Modified 4-2 compressor

(iii) For 4-2 compressor, a half adder is required but for 5-2 compressor a full adder is required because a 5-2 compressor is implemented by series connection of three full adders, that generates three carry output bits in position 'j+1' and one sum bit in position 'j', shown in Figure 3. Thus this conventional logic not only increases the critical path delay but also increases the number of output bits.

As the weightage of **sum** bit is '1' and the weightage of carry bits is '2' of conventional compressors, so the results that produced by those compressors are correct but not in proper binary form. When these conventional compressors are used in multiplier to achieve high speed then one half adder/full adder is required per compressor to process those carry bits. Thus it hampers the speed of operation. So the conventional compressors require one more half adder/full adder to get the final result and this eventually adds more delay and power to the reported results.

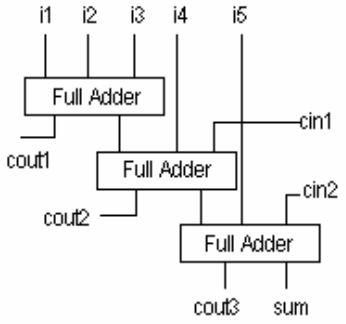

Fig. 3 Conventional 5-2 compressor

III. Proposed Compressor Algorithm

The algorithm of the conventional compressor is not sufficient enough to produce the final addition result. In this proposed compressor we have taken care of the above problems for achieving performance improvement of the multiplier [7]. We like to define the compressor as a counter of "1's" at the input bits.

A. Adder as a counter

A single bit full adder can be considered as a counter of "1,s" at the input bits. The block diagram of a single bit full adder is shown in Figure 4. Here the three inputs are "A" , "B" and "C" and the outputs are "Cout " and "Sum", where, **Cout** is the most significant bit (MSB) and the **Sum** is the Least significant bit (LSB).

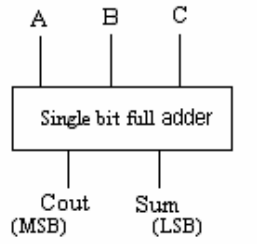

Fig. 4 Single bit full adder

When all the inputs are zero then the outputs are Cout=0 and Sum=0. It implies that there is not a single "1" at the inputs. If any one of the inputs is "1" then the outputs are Cout=0 and Sum=1. It implies that there is a single "1" at the inputs. When any two of the inputs are "1" then the outputs are Cout=1 and Sum=0, which denotes the binary two and indicating that there are two "1"s at the inputs. Finally when all the three inputs are "1" then the outputs denote: Cout=1, Sum=1, i.e there are three "1"s at the inputs. The whole phenomenon is listed in Table I.

TABLE I
ADDER AS A COUNTER

Input Condition	Outputs		Decimal Count
	Cout	Sum	
All the inputs are zero	0	0	0
Any one input is one	0	1	1
Any two inputs are one	1	0	2
All the inputs are one	1	1	3

Thus an adder can be used as a binary counter. The only condition is the MSB and LSB should be mentioned in case of counter. Also an adder compresses three bits into two bits that is why it is also called a 3-2 compressor.

B. Compressor logic

Different compressors logic based upon the concept of the counter of full adder. It can be defined as single bit adder circuit that has four/five/six/seven inputs and three outputs. It is noticed in section III (A) that as long as there are two outputs so long the circuit is able to count upto three. It means that only three inputs can be accommodated in the circuit. But now if one more output is incorporated in the circuit then it is possible to count upto seven (111 i.e decimal 7). A 4-3 compressor is designed in [3] using pass transistors logic. It is easier to access five or six bits simultaneously by using adders (half/full) only. The block diagram of the 5-3 compressor is shown in Figure 5.

The counter property of this compressor is shown in Table II. The counting limit of this compressor is zero to five. The block diagram of 6-3 and 7-3 compressors are almost similar like 5-3 compressor; only one more input to be added to 6-3 compressor and two inputs to be added to 7-3 compressor.

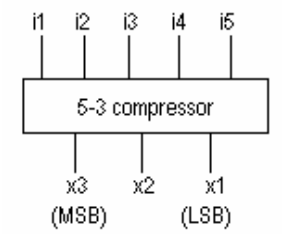

Fig. 5 Block diagram of 5-3 compressor

One more input condition to be included in Table II to get the counter property of 6-3 compressor and two more input conditions for 7-3 compressor.

TABLE II
COUNTER PROPERTY OF 5-3 COMPRESSOR

Input Condition	Outputs			Decimal Value
	X3	X2	X1	
All inputs are zero	0	0	0	0
Any one input is one	0	0	1	1
Any two inputs are one	0	1	0	2
Any three inputs are one	0	1	1	3
Any four inputs are one	1	0	0	4
All five inputs are one	1	0	1	5

C. Architecture of different compressors

The block diagrams of 5-3 and 6-3 compressors with the entire sub units are shown in Figure 6.a and Figure 6.b. Each Figure contains three circuit blocks: two adder blocks and another circuit block that performs the parallel addition operation. Here five bits are processed through one half adder and one full adder. For 6-3 compressor, six bits are processed through two full adder circuits. The outputs are then added by using a smart architecture that does the parallel addition.

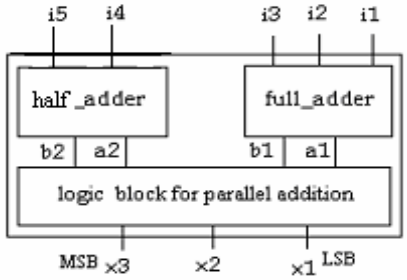

Fig. 6 (a) Block diagram of 5-3 compressor

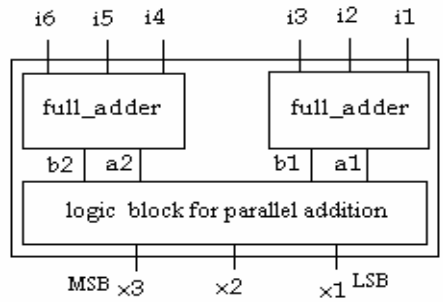

Fig. 6 (b) Block diagram of 6-3 compressor

With the similar logic 7-3 compressor is designed by using one 4-3 compressor, one full adder and parallel adder. The block diagram is shown in Figure 6.c. Here seven bits are processed through 4-3 compressor and a full adder circuit. The outputs are then added by using a smart architecture that do the parallel addition.

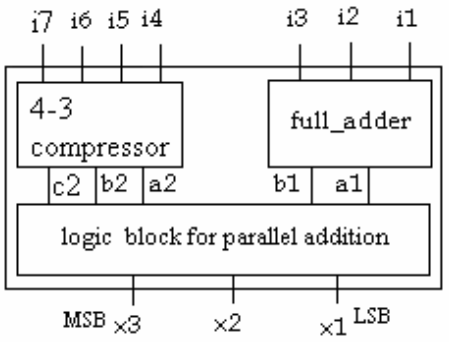

Fig. 6 © Block diagram of 7-3 compressor

IV. Multiplier Algorithm and Architecture

A 16-bit multiplier is constructed by using Wallace tree architecture [8]. The architecture has been shown in Figure 7. Partial products are added in five stages. Adders and different compressors are used to minimize the stage operations. Compressors and adders are used carefully so that minimum number of outputs would be generated. Consider the column number ten where ten bits are added at the first stage. These ten bits could be added by using two 5-3 compressors, but that will generate six (three of each compressor) outputs, instead of this we have used one 7-3 compressor and one full adder that generate five outputs only (three of compressor and two of full adder) that eventually decrease the number of bits for the next stage.

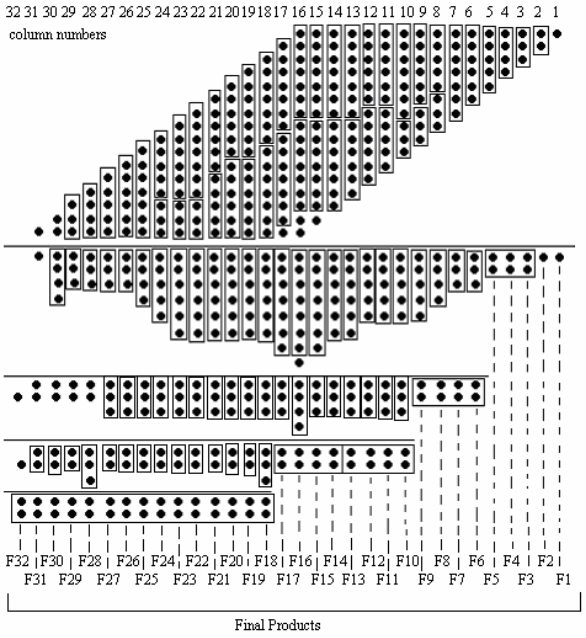

Fig. 7 Architecture of 16×16 bit multiplier

Now consider the column number sixteen where sixteen partial products are added at the first stage. Sixteen partial products could be added by using one 7-3 compressor, one 6-3 compressor and one full adder circuits, but these three architectures will generate eight outputs. Instead of this we have used two 7-3 compressors that generate six outputs and the other two bits are promoted to the second stage directly, so ultimately eight bits are left for the second stage addition without involving one extra adder. Thus by using minimum number of adders/compressors partial products are added without compromising the number of bits generation for the next stage operation.

It is to be mentioned that each compressors (4-3 to 7-3) has three outputs of bit position j^{th}, $(j+1)^{th}$ and $(j+2)^{th}$. Now if a compressor is used in column no six (say) then it's j^{th} output goes to the circuit of column no six and $(j+1)^{th}$ bit goes to the circuit of column no seven and the rest output goes to the circuit of column no eight of the next stage. Thus our compressors reduce vertical critical path more rapidly than conventional compressors [9]. An example of bit reduction using conventional compressors is shown in Figure 8. Two columns are taken in this example each of five bits. In the same figure, dot diagram and block diagram both are shown.

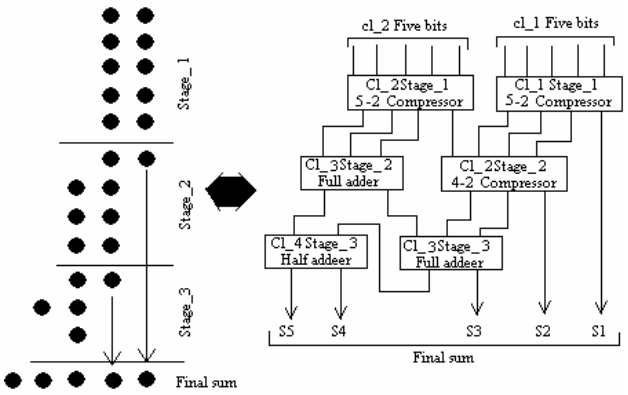

Fig. 8 Bit reduction technique using conventional compressors

Similarly in Figure 9 two columns each of five bits are taken for reduction by using our compressors. In this approach the addition becomes two-stage process whereas it is three-stage in the conventional approach. After first stage addition eight bits are produced in conventional way but in the proposed approach it becomes six.

In figure 7, each dot represents a single binary bit. Those bits are enclosed by different rectangles that contain different no of dots. One rectangle that contains four dots represents a 4-3 compressor, similarly the others. The rectangles that contain three or two bits represent full adder or half adder. Also there are some rectangles that containing two rows of bits are the parallel adders. At the final stage a sixteen bit parallel adder has been used. Carry look ahead logic has been used to develop sixteen bit parallel adder circuit.

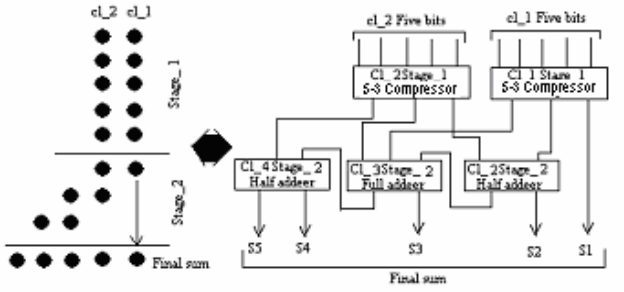

Fig. 9 Bit reduction technique using our compressors

The architecture, shown in Figure 7, is only the partial product addition stage. The total multiplication process can be divided into three stages: (i) partial product generation, (ii) partial product addition and (iii) final addition. The block diagram is shown in Figure 10.

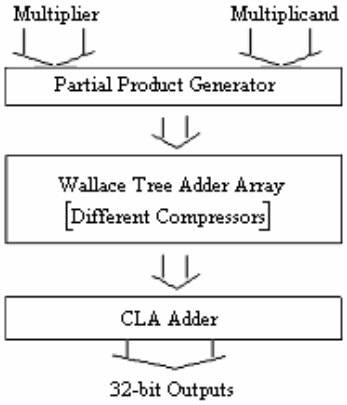

Fig. 10 Overall architecture of 16×16 multiplier

The first block is designed using TG AND gates only. Adders and compressors are used in the second block for Wallace tree addition. The final addition is done using hybrid CLA adder (designed with TG and CMOS), to minimize the critical path gate stages.

V. Multiplier Performance and Comparison

Use of higher order compressors reduces multiplication delay and power consumption. These compressors are more effective for high order multiplication. The performance results of the 16-bit squarer are shown in Table III. The delay and the power measured using the worst-case pattern and from the output where the delay is maximum.

TABLE III

SIMULATION RESULTS OF THE 16-BIT MULTIPLIER

Simulation mode	Power Dissipation		Delay (ns)	EDP (10^{-24} J-sec)
	Dynamic Power (uw)	Leakage Power (uw)		
High-V_T	72	09.6	1.45	151
Low-V_T	183	039	1.07	209
Dual-V_T	98	14.2	1.19	138

Simulation has been performed for three different modes of transistors: (i) all High V_T transistors, (ii) all Low V_T transistors, (iii) Dual V_T transistors. In Dual threshold technology, high threshold transistors are used in non-critical path to reduce leakage and low threshold transistors are used in critical path to reduce delay [10]. Dual threshold technology has been used in different way in case of transmission gates. The two types of threshold voltages are assigned by incorporating two sleep transistors to the main circuit [11,12].

The simulation results show that Dual V_T offers the minimum EDP. The optimum placement of the high-V_T and low-V_T transistors into the circuit has been found to achieve almost 65% reduction in the leakage power as compared to the scheme using all low-V_T transistors and 20% reduction in delay with respect to the high-V_T case. Since leakage power becomes an important concern in sub-90 nm circuits, the method of DTCMOS seems a plausible choice in future technology.

A comparative study of delay and power for different multiplications using high-speed compressors and the conventional way where full-adders (FA) & half adders (HA) are used is shown in Table IV. Simulation results show that the multipliers in our proposed scheme offer minimum energy delay product (EDP). In this scheme EDP can be reduced by almost 50% for higher order multiplication.

TABLE IV
DELAY AND POWER COMPARISON OF DIFFERENT MULTIPLIERS

Multiplication	Conventional process			Using Compressors		
	Delay (ns)	Power (uw)	EDP (10^{-24} J-sec)	Delay (ns)	Power (uw)	EDP (10^{-24} J-sec)
4×4	0.19	3.78	0.14	0.19	4.56	0.16
6×6	0.53	4.16	1.17	0.42	5.34	0.94
8 ×8	0.83	10.1	6.96	0.52	8.92	2.41
16×16	2.21	64.0	313	1.45	72	151

The graphical presentations of the comparison as listed in Table IV are shown in Figure 11 and Figure 12. Delay has been compared in Figure 11 and power has been compared in Figure 12. It is evident from the simulation results that the use of compressors in multiplier reduces the operation time as well as the energy delay product (Dynamic power × $Delay^2$).

The compressors become effective from 8 ×8 multiplication. Use of these compressors not only reduce delay but also reduce the stage of operations. It becomes five-stage operation for 16 ×16 multiplication by using compressors as shown in Figure 7. The same multiplication becomes seven-stage operation in the conventional process. This stage reduction eventually reduces the glitches and so on the glitch power.

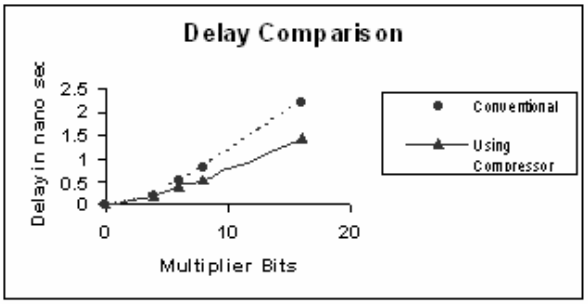

Fig. 11 Delay comparison between conventional and proposed process

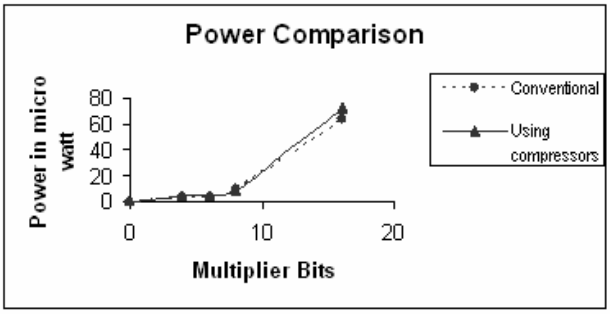

Fig. 12 Power comparison between conventional and proposed process

The difference of multiplication time delay between conventional approach and proposed approach increases as the number of multiplication bits increases. But the consumed power remains almost same for the both process. Thus, by using these compressors high order multiplication can be made faster without providing extra power.

VI CONCLUSIONS

Different compressors are used to speed up the multiplication process. 4-2 compressors and even 5-2 compressors are reported earlier but those are not used in multiplier successfully. Here we have used our compressors in multiplier circuits successfully. Performances of multipliers are compared with the conventional approach where only adders are used to add the partial products. For the conventional approach our modified adders are used and that is why the consumed power for both the cases becomes comparable.

Use of compressors not only reduce the vertical critical path but also reduce the stage operations simultaneously. Using dual-threshold voltage technique is seen to reduce energy delay product noticeably and leakage power dramatically, making this as one of the important power aware design technique for the future sub-90 nm generation.

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