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Nano-Texturing of Single Crystalline Silicon via Cu-Catalyzed Chemical Etching

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***Abstract*—**We have discovered an important technical solution that could make new approaches in the processing of wet silicon etching, especially in the production of photovoltaic cells. During its inferior light-trapping and structural properties, the inverted pyramid structure outperforms the conventional pyramid textures and black silicone. The traditional pyramid textures and black silicon can only be accomplished with more advanced lithography, laser processing, etc. Importantly, our data demonstrate the feasibility of an inverted pyramidal structure of silicon via one-step Cu-catalyzed chemical etching (CCCE) in Cu $(NO_3)_2$/HF/H_2O_2/H_2O solutions. The effects of etching time and reaction temperature on surface geometry and light trapping were systematically investigated. The conclusion shows that the inverted pyramid structure has ultra-low reflectivity of ~4.2% in the wavelength of 300~1000 nm; introduce of Cu particles can significantly accelerate the dissolution of the silicon wafer. The etching and the inverted pyramid structure formation mechanism are discussed. Inverted pyramid structure with outstanding anti-reflectivity includes useful applications throughout the manufacture of semi-conductive industry-compatible solar cells, and can have significant impacts on industry colleagues and populations.

***Keywords*—**Cu-catalyzed chemical etching, inverted pyramid nanostructured, reflection, solar cells.

I. Introduction

SINGLE, crystalline silicon texture is an interesting subject of current technology and science, especially throughout the solar energy field [1], [2]. Through anisotropic etching (100)-oriented crystalline silicon (c-Si) in alkaline solutions, random pyramid arrays with reduced reflectivity of 10% can be easily obtained [3], commonly used in the manufacture of c-Si photovoltaic (PV) cells [3], [4]. Black silicon (B-Si) with even low reflectivity is typically obtained via metal-assisted chemical etching, under to 2% [6]. However, B-Si is still not ideal for PV cells due to its high levels of cell division owing to nanoparticles [7]. Importantly, the complication of additional costs and associated costs obstruct the introduction of mass production pyramid nanostructures, not only does it help us offer a particular technological solution; we also demonstrate multidisciplinary core processes as well. In specific, a Cu-NPs population connected to c-Si tends to be a variable of crystallographic plane orientation due to a low Cu^{2+} electron capture potential and a difference in Si (100) and (111) aircraft electron supply concentration. Tuning the density of Cu-NPs on Si (100) and (111) planes naturally permits the anisotropic etching of sui generis carrier transport balance. In particular, our technique is consistent with most manufacturing lines of PV and can, therefore, hold a new age of using Si inverted pyramids texture.

Among the various B-Si nanostructures [8], the inverted pyramids structure used in passivated emitter rear locally diffused (PERL) cell and achieved the world record of PV transformation efficiency in 2001 [9], which led to widespread publicity. Low surface area and good light absorption capacity can be achieved by the inverted pyramid nanostructures [10], [11]. It is also reported that the inverted pyramid structure is better able to balance the improvement of anti-reflectance and the recombination of the photo-generated carrier surface [12]. The difficult process and the related extra costs are impeding the application of inverted pyramids structure in the mass production process.

Here, through the one-step CCCE process, we introduced an easy option to the inverted pyramids structure on the silicon surface. The effects of the etching parameters (etching time and reaction temperature) on morphology and reflectance spectra of silicon wafers were systematically investigated. The large-scale inverted pyramids structure has been obtained from single c-Si with excellent anti-reflection, which is crucial for the preparation of a solar cell with high efficiency.

II. Experimental

The P-type diamond wire sawing (DWS) single c-Si wafers, resistivity of 1~3 Ω·cm, (100)-oriented was used in this study, and the wafers were sliced to a size of 20×20 mm^2. The wafers are washed under ultrasound for 10 minutes in acetone, ethanol, and deionized water, respectively, before etching.

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And then the samples to remove the native SiO_2 were immersed in 10% HF solution for 10 min. Such wafers were subsequently placed in the etching solution, and the detailed experimental processes were shown in Fig. 1. The inverted pyramid structure was obtained when the wafers were etched for different etching time (3, 6, and 9 min) at different reaction temperatures (30, 40, and 50 °C) with 0.05 mol/L concentration of Cu $(NO_3)_2$, 2 mol/L concentration of HF, and 1 mol/L concentration of H_2O_2. The spectrum of reflection and inverted pyramids structure obtained via one-step copper assisted chemical etching for 3 min, 6 min and 9 min. During at least 20 minutes in a sonication bath, residual Cu-NPs were extracted using concentrated nitric acid. The Si wafers are rinsed thoroughly with deionized water and dried under nitrogen flow. A TESCAN VEGA3 scanning electron microscope (SEM) was used to characterize the morphology of as-fabricated surfaces of samples. The surface reflectivity of wafers was measured by a UV-2600 spectrophotometer.

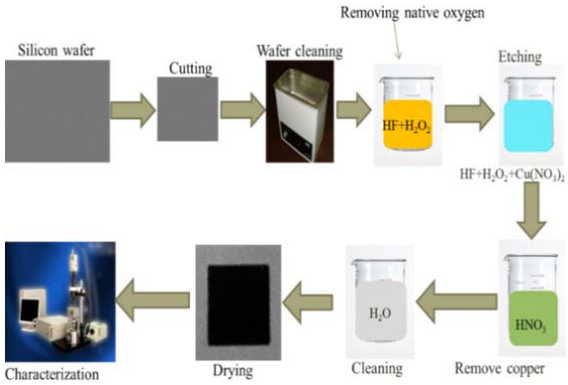

Fig. 1 Scheme of experimental processes

III. Results and Discussion

In the process of one-step CCCE, many parameters affect the surface nanostructure of the silicon wafer. In these experiments, the effects of etching time and reaction temperature on surface morphology wafer and light trapping ability were investigated. We used the control variable method in the etching process. It means that when one parameter influence is studied, the values of other parameters are fixed at specific values, and the value of the studied parameter is changed to different values to know the extent of the impact of this parameter on the reaction process rate.

In the etching process, mainly the effect of etching time and reaction temperature on the surface of silicon is studied. In the experiment, concentrations of H_2O_2, Cu $(NO_3)_2$, and HF were set as 1 mol/L, 0.05 mol/L, and 2 mol/L respectively, and the main experiments were taken as etching times (3 min, 6 min, and 9 min) and different temperatures (30 °C, 40 °C, and 50 °C) under three different groups, each group contained three samples of silicon wafer.

We have investigated the effects of different etching time on the surface morphology of the inverted pyramid-like structure. Three groups (9 samples) were prepared at different etching times set as the first group at 3 min, second group at 6 min, and third group at 9 min, with different reaction temperatures (30 °C, 40 °C, and 50 °C). And the H_2O_2 concentrations, amount of Cu $(NO_3)_2$, and concentration of HF were respectively set as 1 mol/L, 0.05 mol/L, and 2 mol/L, and samples were put in the etching solution, followed by SEM-characterized samples. Figs. 2 Aa, Ba and Ca are the DWS raw single crystal silicon; on the surface of raw DWS silicon, there are several brittle grooves and holes, as well as parallel plastic saw lines. According to previous research, amorphous surfaces caused by plastic friction during the DWS process filled the region of flat saw marks [14]. Compared to Fig. 2 Aa raw wafer, Figs. 2 Ba and Ca were found on the silicon surface to have some large inverted pyramid-like pits. When the reaction temperature was 3 min, it indicated that the CCCE method was a fast process. When the etching time increased, the etching surface becomes inverted pyramid-like structure; meanwhile, the formed inverted pyramid structure became more regular and with more uniform and smoother surface size, as shown in Fig. 2 Ad. When the etching time exceeded 9 min, as shown in Figs. 2 Cb and Cc, the morphology of the etched silicon wafer becomes slightly disordered. The excessive etching leads to the disorder [15] and the silicon wafer with a more oxidized surface that suggested that when the temperature and time were high at the same time, it would be impossible to achieve a regular and more uniform and smoother surface size.

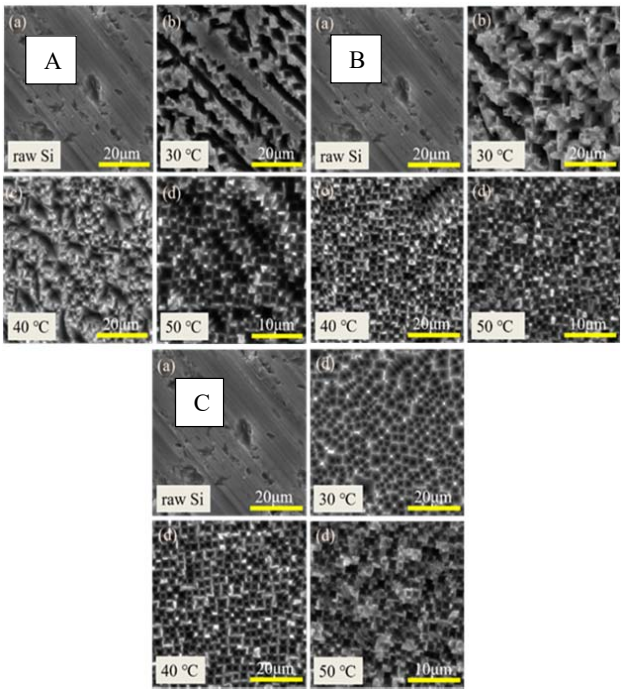

Fig. 2 SEM images of raw silicon wafers (a) in each (A, B, and C) figures and inverted pyramid structure silicon surface under different Etching Times: A 3 min, B 6 min, and C 9 min, respectively

Fig. 3 shows the spectrum of reflection the inverted pyramids on the silicon surface under various etching times; the surface anti-reflection ability of the silicon covered

inverted pyramids was improved. As the etching time reaches 9 min, the average reflectivity dramatically reduces from 27.3% to 4.2%. The designed inverted pyramid-like structures have increased the characteristics of light absorption in the wider spectrum of 300~1000 nm, that is good than other nano-texturing structures in previous reports [14], [16], [17], nano-silicon energy band change is linked to the excellent anti-reflection capability [18].

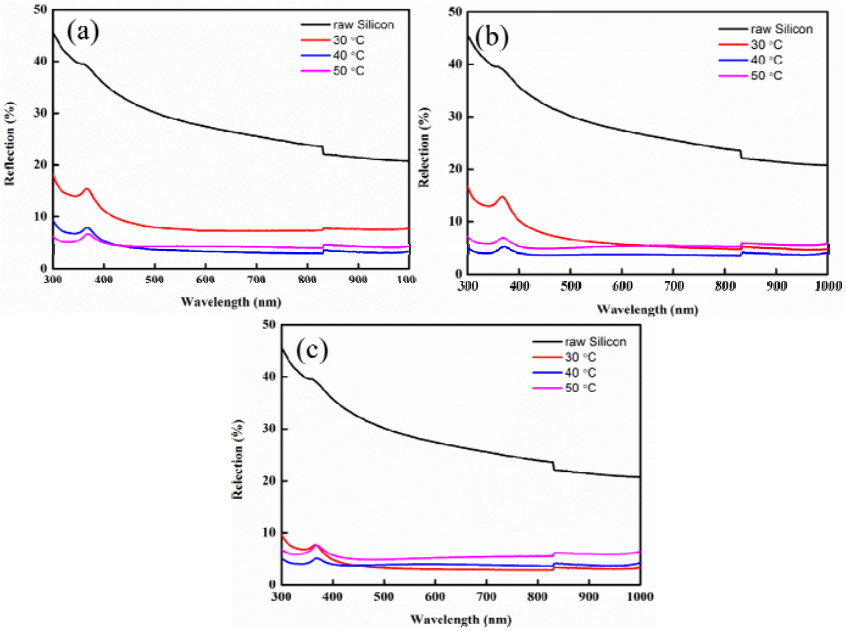

Fig. 3 Spectra of under different etching time (a) 3 min, (b) 9 min, (c) 9 min, respectively

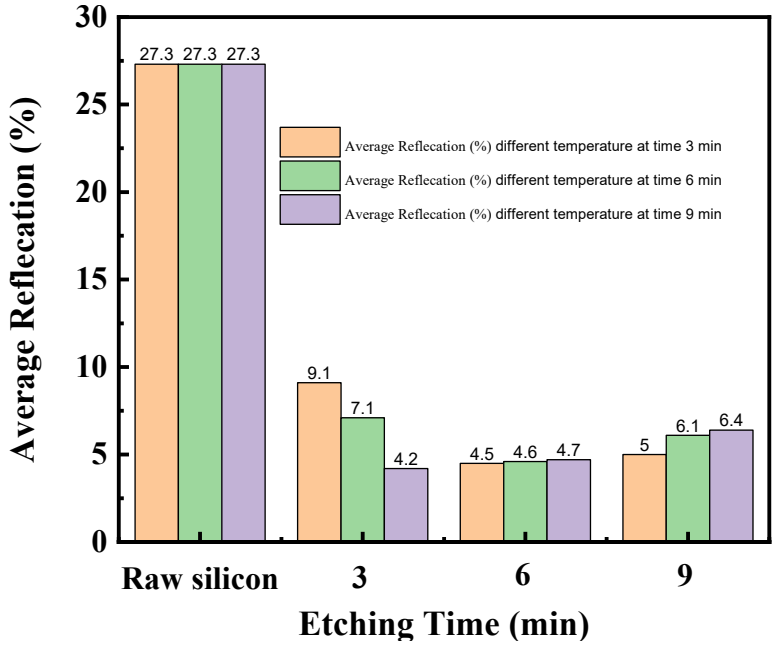

Fig. 4 Spectra of under different etching time and average reflectivity

We have explored the effects of different reaction temperature on the surface morphology. Three sample groups are prepared of different reaction temperature (30 ℃, 40 ℃ and 50 ℃), and under different etching times (3 min, 6 min, and 9 min). And the H_2O_2 concentrations, Cu $(NO_3)_2$, and concentration of HF were respectively put as 1 mol/L, 0.05 mol/L, and 2 mol/L. The reaction rate increases gradually as the temperature of the reaction increases. Because the injection holes' rate increased when the temperature of the reaction increased, i.e. the silicon wafer is oxidized more

quickly; the solution reaction rate naturally increases with increasing etching temperature. At 30 ºC, the etched silicon was the sparse, shallow etching pits cover the surface. When the temperature is 40 ºC, the surface of the silicon wafer gradually becomes the inverted pyramids structure. When the temperature reaches 50 ºC, the etched surface becomes slightly disordered, and some etching pits-merging phenomenon between the independent inverted pyramids is observed. The injection holes in the silicon wafer are slow when the etching temperature is low, that is, the reaction rate of oxidation is slow, and the etched pits are sparse and shallow. With an increasing etching temperature, the silicon wafer is oxidized more quickly, and excessive etching leads to a merging phenomenon.

Fig. 6 displays the reflection of silicon wafers at different temperatures of reaction. Temperatures show that the silicon wafer's reflectivity continues to decline with increased reaction temperature; the lowest reflectance was obtained at 30 ℃. The average reflectivity in the wavelength range of 300~1000 nm drops dramatically from 27.3% to 4.2%.

A representative sample of less than 0.05 mol/L Cu $(NO_3)_2$, 2 mol/L HF, 1 mol/L H_2O_2 concentration, at 30 °C for 9 min, was characterized for careful study of the inverted pyramid structure. The top view shows a regular inverted pyramid profile, and the inverted pyramid is 1.5~3 μm wide and 1~2 μm deep. The magnified cross-sectional image of SEM shows that there are numerous etching pits on the sidewalls of the inverted pyramid that attributed to the nucleation and dissolution of silicon sidewall by the copper nanoparticle, Fig. 8.

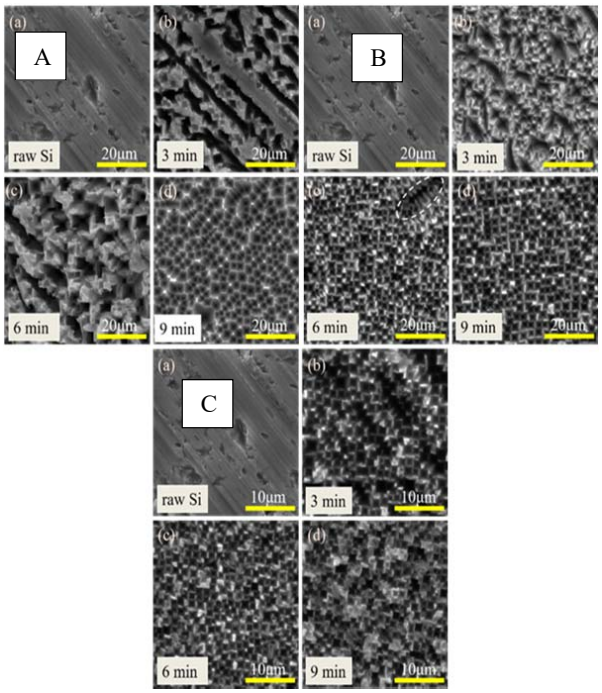

Fig. 5 SEM images of raw silicon wafers (a) in each (A, B, and C) figures and inverted pyramid structure silicon surface under different reaction temperatures: A 30 ℃, B 40 ℃ and C 50 ℃, respectively

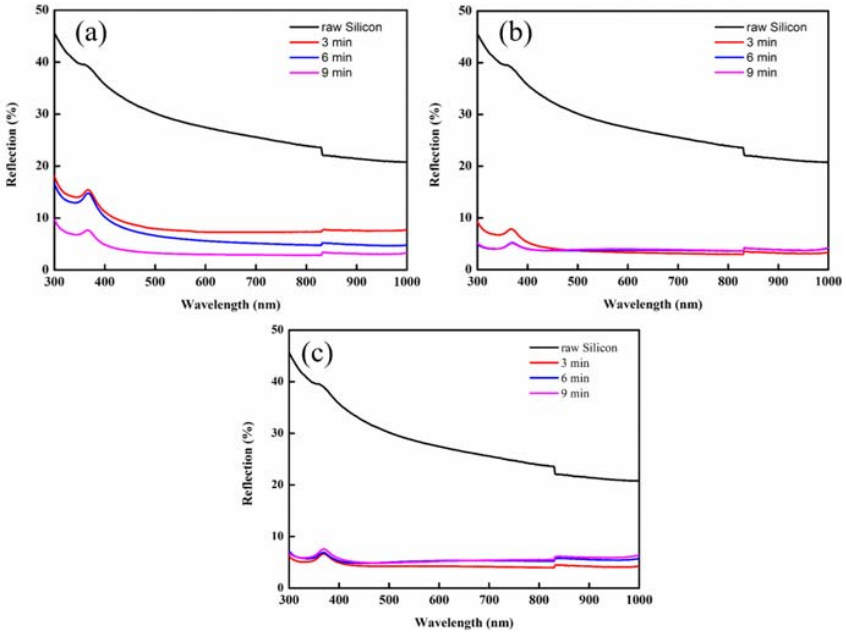

Fig. 6 Spectra of at different reaction temperatures (a) 30 ℃, (b) 40 ℃ and (c) 50 ℃, respectively

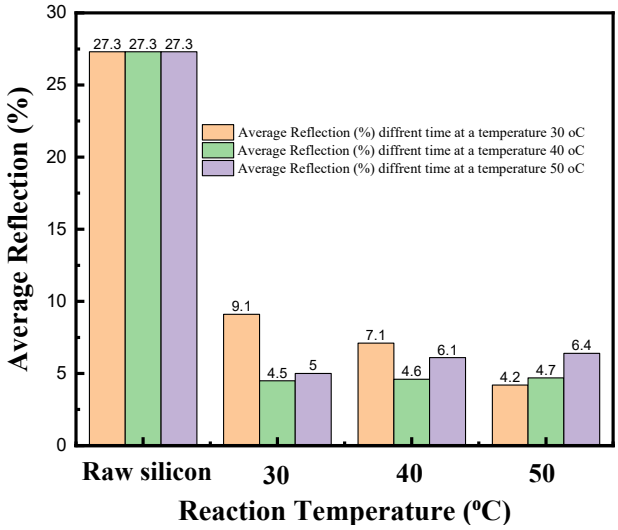

Fig. 7 Spectra of under different reaction temperatures and average reflectivity

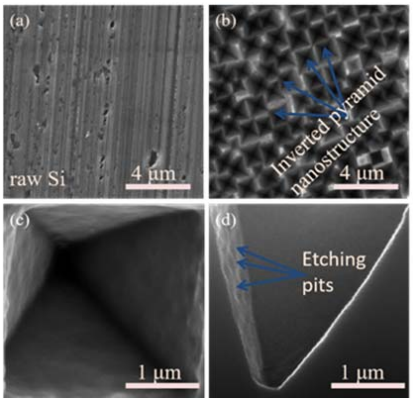

Fig. 8 Top view SEM images of raw silicon (a), and top view (b) and cross-sectional image (c) (d) of the representative inverted pyramid arrays under etching conditions: 0.05 mol/L Cu $(NO_3)_2$, 2 mol/L HF, 1 mol/L H_2O_2, 9 min, and 30 °C

IV. Etching Mechanism

Fig. 9 shows the formation schemes of inverted pyramid structures by one-step CACE; the silicon-inverted pyramid wafer-scale was formed in a mixture of Cu $(NO_3)_2$/HF/H_2O_2/ H_2O at 50 ℃ using a Cu-NPs. The basic principles were based on the electrochemical reaction of Si-Cu^{2+}/Cu-NPs [19], [20]. The main factor of this electrical response is the difference in electrochemical potential between Si and Cu^{2+}/Cu-NPs. The reaction can be viewed as two half-cell reactions similar to the well-known process of metal-assisted chemical etching used to produce different Si nanoparticles [21]–[23].

Cathode reaction:

$$Cu^{2+} + 2e_{VB}^{-} \rightarrow Cu^{0} \quad (1)$$

$$H_2O_2 + 2H^{+} \rightarrow H_2O + h^{+} \quad (2)$$

Anode reaction:

$$Si(s) + 2H_2O \rightarrow SiO_2 + 4H^{+} + 4e_{VB}^{-} \quad (3)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (4)$$

The Si/Cu $(NO_3)_2$/H_2O_2/HF system, in this case, consists of a redox corrosion-type combination: the cathodic reduction of Cu^{2+} ions with H_2O_2 as well as the anodic oxidation and dissolution of Si under the deposited Cu-NPs. Cu^{2+} ions absorb, accumulate and form NPs from the vicinity of the Si substrate. In this way, originally nucleated Cu-NPs attract electrons from Si and become negatively charged as Cu is more electronegative than Si. By attracting the Cu^{2+} ions from the solution, these negatively charged Cu-NPs expand further [19], [20]. During this cycle, the HF continually oxidizes and etches Si atoms below the Cu-NPs. At the same time, it is important to reduce H_2O_2 in the Cu-NPs to induce anisotropic Cu-NPs deposition on the Si surface and to ensure the development of inverted pyramid structures to be interpreted in the following sections. Concentrated nitric acid was used in a sonication bath for at least 20 minutes to wash the inverted pyramid structures to eliminate any residual Cu-NPs. No Cu-NPs was found after the nitric acid bath and no Cu-NPs spectra of the inverted pyramid structures during SEM.

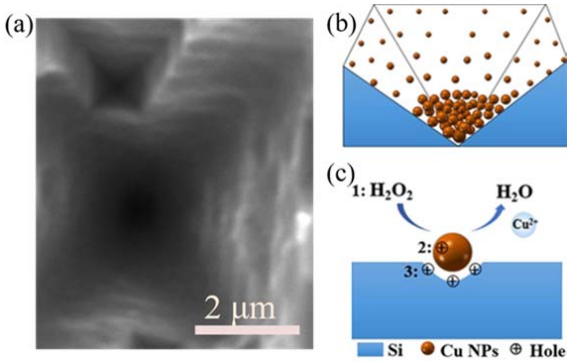

Fig. 9 SEM image of the CCCE and schematics: (a) SEM top-view image of an individual inverted pyramid structure, (b) deposition schematics of Cu NPs. (c) H_2O_2 reduction process schematics and holes injection mechanisms

Acknowledgment

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