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A 0.9 V, High-Speed, Low-Power Tunable Gain Current Mirror

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***Abstract*—**A high-speed current mirror with low-power method of adjusting current gain is presented. The current mirror provides continuous gain adjustment; yet, its gain can simply be programmed digitally, as well. The structure features the ever interesting merits of linear-in-dB gain control scheme and low power/voltage operation. The performance of proposed structure is verified through the simulation in TSMC 0.18 µm CMOS Technology. The proposed tunable gain current mirror structure draws only 18 µW from 0.9 V power supply and can operate at high frequencies up to 550 MHz in the worst case condition of maximum gain setting.

***Keywords*—**Current mirror, current mode, low power, low voltage, tunable circuit, variable current amplifier.

I. Introduction

NOWADAYS, current-mode signal processing has gained a significant interest due to the low voltage and low power concerns imposed by technology down scaling trend [1]-[3]. The reason is that, even though the voltage dynamic range is extremely limited in low voltage supplies, the current dynamic ranges in several orders of magnitude can still be achieved. Current mirrors are very promising active building blocks for realizing current-mode circuits. One desirable feature of current mirrors is the capability of electronically adjustable gain. This feature finds its application in circuits with highly accurate current transfer ratio or in the current amplification/attenuation circuits. A number of tunable current mirror topologies have been already introduced to address this (tunable gain) merit [4]-[10]. However, there are some drawbacks related to these works. For example: I) The operating bandwidth of [4], 85] are limited due to the implementation of subthreshold devices. II) The gain tuning range of [6], [7] are limited. III) The implementation of PMOS transistors for handling AC signals reduces the maximum operating frequency in [4], [5], [8]-[10].

An all-NMOS tunable current mirror is presented in this work. The proposed circuit offers linear-in-dB gain control scheme along with high-speed and low-power operation.

II. Proposed Current Mirror Structure

The schematic of the proposed tunable gain current mirror is shown in Fig. 1. The structure is composed of mirroring transistors of M1-M2 and cascode transistors of MC1-MC2. In addition to improving the current transfer accuracy and the output impedance of current mirror, the cascode transistors also are used to adjust the gain of current mirror, as well. In the proposed structure, the gain adjustment can simply be done by applying a differential voltage to the gate nodes of MC1-MC2. This way, the mirroring gain of structure changes exponentially with applied control voltage, VC. The gain adjustment capability can be expressed by

$$M=\frac{I_{out}}{I_{in}}=\frac{k_2}{k_1}\times\frac{\left(V_{gs2}-V_{th}\right)^2}{\left(V_{gs1}-V_{th}\right)^2}\times\frac{\left(1+\lambda V_{ds2}\right)}{\left(1+\lambda V_{ds1}\right)},\ k_i=\frac{\mu C_{ox}W_i}{2L_i},i=1,2 \quad (1)$$

Relation (1) can be rewritten as (2) assuming that $\alpha=\lambda/(1+\lambda V_{ds0}+\lambda V_{gs})$.

$$M=\frac{k_2}{k_1}\frac{\left(1+aV_C\right)}{\left(1-aV_C\right)}=e^{2aV_C} \quad (2)$$

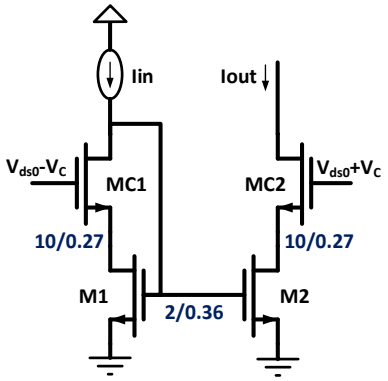

Fig. 1 Proposed high speed low power adjustable gain current mirror

As can be seen from (2), the variation of gain versus control voltage is exponential (linear-in-dB), which is a very interesting feature in variable gain structures. The minimum required voltage for the circuit to proper operation is a little more than $V_{th}+2V_{ds,sat}$. This is another interesting property of the proposed structure that makes the structure very interesting for low voltage applications. The distinct property of the proposed adjustable gain current mirror is that no extra circuitry is used to accomplish the variable gain function. Instead, the gain tuning is simply performed by applying a control voltage to the gates of cascode transistors which are already a part of current mirror structure. Therefore, no extra circuitry, extra power, or any other penalty is required. In other words, transistors MC1-MC2 play two important roles. First, they suppress the unwanted drain-source voltage changes in the drains of M1-M2 which caused from signal swing or output voltage changes. This, however, improves the

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linearity and also the output impedance of current mirror. Second, they are used to apply the gain control voltage to the drain nodes of M1-M2 transistors. Therefore, by varying the drain-source voltages of M1 and M2 with respect to each other, the gain adjustment can easily be accomplished.

III. Simulation Results

The Spectre RF simulations are performed with TSMC 0.18 µm standard CMOS technology. The proposed circuit draws 18 µW DC power from 0.9 V power supply. The control voltage of VC varied 10 mV over its 550 mV DC common mode component to adjust the mirroring gain of proposed structure.

The DC and AC transfer function of the presented structure is shown in Figs. 2 and 3, respectively. As depicted in these figures, the gain changes exponentially with control voltage. From Fig. 2, it can be observed that the current amplification/ attenuation ratio is greater at higher DC currents. The reason behind this fact is that the value of α increases at higher DC currents. From Fig. 3, it can be found that the operating bandwidth of the structure is interestingly almost-constant and remains higher than 550 MHz for all operating gain settings. Fortunately, the operating bandwidth over power consumption is very high, which makes the circuit very suitable candidate for high-speed low-power applications.

The time domain behavior of proposed structure is depicted in Fig. 4, where, the sinusoidal signal with amplitude of 1 µA and the frequency of 10 MHz is applied to the input of structure. Again, Fig. 4 proves that the proposed circuit is stable and well-performs the current amplification at different gain settings.

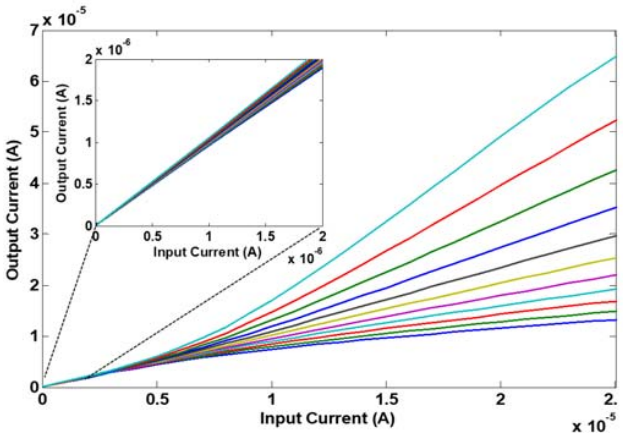

Fig. 2 DC current transfer function at different gain settings

The current gain versus control voltage is depicted in Fig. 5. This figure shows that the current gain varies linearly (in dB scale) with control voltage, which is very interesting merit in variable gain amplifier structures. From Fig. 5, the claim that the current mirror structure can deliver more than 15dB linear-in-dB gain control range is defendable. This figure shows very little gain error of the proposed circuit. Another study that may show a strong value is to plot the 3-dB cutoff frequency of structure at various gain settings. This plot is depicted in Fig. 6. This figure shows that, although the bandwidth remains almost constant over the various amplification gains, it linearly decreases as the current gain increases. Fig. 6 shows that the minimum operating bandwidth of the circuit starts from 550 MHz for maximum gain setting of about 9 dB and increases linearly up to 1.7 GHz for minimum gain setting of about -6 dB.

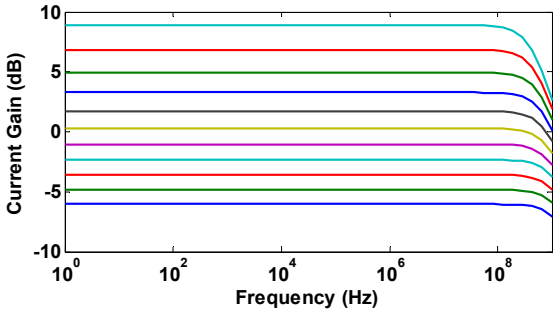

Fig. 3 The frequency performance of the presented adjustable gain current mirror

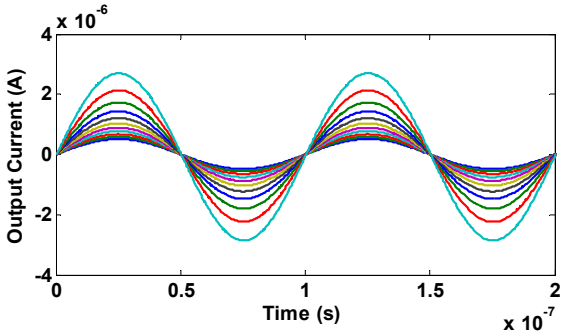

Fig. 4 The time domain output current waveforms for IIn,ac = 1 µA at different gain settings

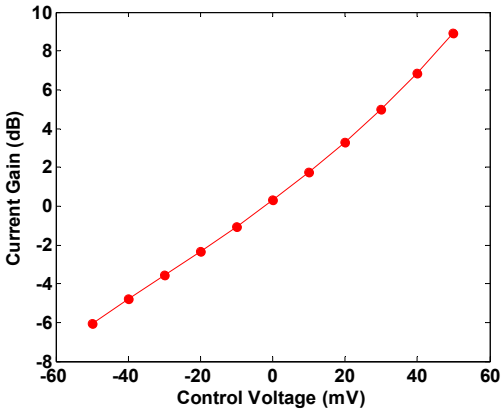

Fig. 5 The current gain versus control voltage

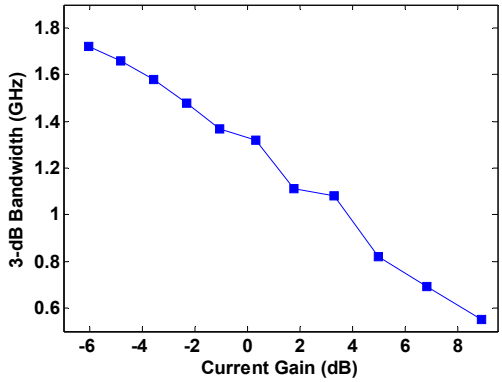

Fig. 6 The 3-dB bandwidth of proposed circuit versus current gain

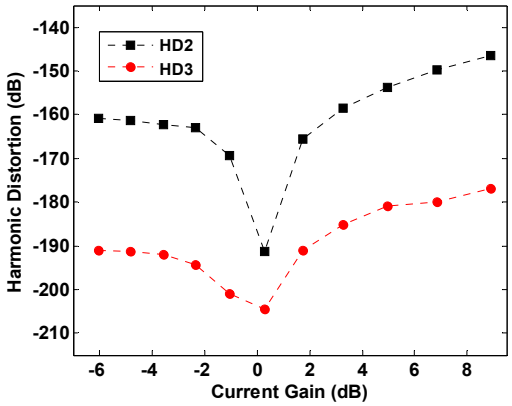

Fig. 7 The harmonic distortion of proposed circuit at various current gains

The linearity performance of circuit is investigated through simulating HD2 and HD3 parameters. The HD2 and HD3 parameters at various current gains are plotted in Fig. 7 These plots show that, at balance condition (M≈0 dB), the HD2 and HD3 are well below -191d B and -204 dB, respectively. This figure also shows that both HD2 and HD3 worsen when signal experience amplification or attenuation. Nevertheless, the HD2 and HD3 respectively remain below -144 dB and -176 dB at worst operating conditions of maximum gain setting, which are acceptable in most of the applications. The reduction of linearity when circuit leaves balance condition (M≈1), was however predictable. The reason is that at balance condition the circuit and its parameters and elements are best matched, which delivers the most available linearity. However, beyond this, some nonlinear effects arise that degrade the linearity performance of structure.

The noise performance of structure is depicted in Fig. 8. This figure plots the input referred noise current at different gain settings while the operating frequency is swept from 1 Hz to 2 GHz. In Fig. 9, the input referred noise current of circuit is plotted versus the current gain, changing the operating frequency from 1 kHz to 1 GHz. This figure shows that the input referred noise current of circuit decreases with increasing the current gain and operating frequency and remains less than 5 pA for operating frequencies higher than 1 MHz.

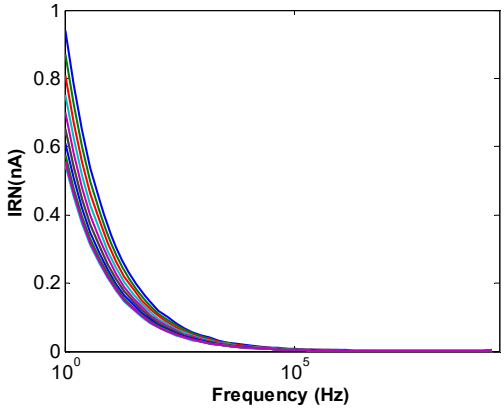

Fig. 8 The input referred noise performance of proposed circuit at various frequencies

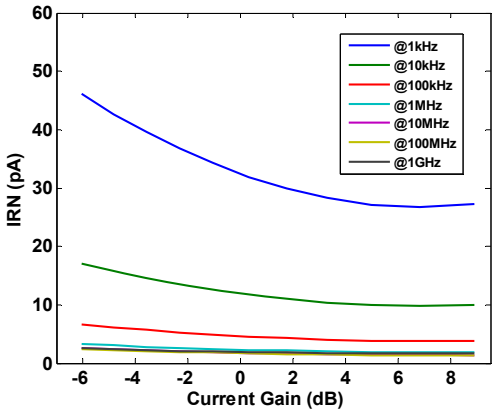

Fig. 9 The input referred noise current versus current gain at different operating frequencies

The performance comparison of proposed structure with some other similar works is presented in Table I. As Table I shows, the proposed structure outperforms the other works in terms of operating frequency and dissipation power, substantially.

TABLE I
THE COMPARATIVE RESULTS OF THE PROPOSED WORK WITH SOME OTHER SIMILAR WORKS

Parameter	VDD (V)	3-dB BW (MHz)	Power (µW)	Tuning Range (dB)	Process (µm)
* [7]	1.5	1.7	45	#2	0.35 AMS
[11]	1.3	100	780	20	0.18 TSMC
This Work	1.8	550	18	15	0.18 TSMC

Evaluated from Fig. 3
* Measurement Results

IV. CONCLUSION

A high speed, low voltage, low power tunable gain current mirror was presented in this paper. The performance of structure was shown with simulation using TSMC 0.18 µm technology. The simulations proved the well operation of the

proposed structure.

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He was with IUST Electronic Research Center Group, from 2007 to 2010 as a Researcher, and Science and Research Branch, Islamic Azad University from 2011 to 2015, as a Fellow Lecturer. He joined Sahand University of Technology, Tabriz, Iran as an Assistant Professor in 2015. He is the author or coauthor of more than 30 national and international papers and also collaborated in several research projects and has a registered Iranian patent. Dr. Faraji Baghtash was selected as distinguished researcher of the IUST in 2011. His current research interests include current mode/voltage mode analog integrated circuit design, low voltage, low power circuit and systems, analog microelectronics and digital system design.