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A Thirteen-Level Asymmetrical Cascaded H-Bridge Single Phase Inverter

P. Varalaxmi, A. Kirubakaran

Abstract**—**This paper presents a thirteen-level asymmetrical cascaded H-bridge single phase inverter. In this configuration, the desired output voltage level is achieved by connecting the DC sources in different combinations by triggering the switches. The modes of operation are explained well for positive level generations. Moreover, a comparison is made with conventional topologies of diode clamped, flying capacitors and cascaded-H-bridge and some recently proposed topologies to show the significance of the proposed topology in terms of reduced part counts. The simulation work has been carried out in MATLAB/Simulink environment. The experimental work is also carried out for lower rating to verify the performance and feasibility of the proposed topology. Further the results are presented for different loading conditions.

Keywords**—**Multilevel inverter, pulse width modulation, total harmonic distortion, THD.

I. Introduction

IN recent years the development of multilevel inverters with reduced part count is becoming more popular for photovoltaic cells, High-Voltage Direct Current (HVDC), vehicular technology and industrial drives applications etc. This is mainly due to reduction in device counts, gate driver circuits, cost guarantee of high efficiency and control complexity. However, the existing conventional multilevel topologies of diode clamped, flying capacitor and cascaded-H-bridge continue to be preferred for industrial applications. But increased device counts such as clamping diodes, flying capacitors and dc link voltage balancing problem limit the use of diode clamped and flying capacitor inverters to a maximum of three-level operation only. However, H-bridge inverter is getting popularity due to its improved performance, less stress across switching devices and their modularity with increased DC source. Therefore, newer topologies based on reduced part count have been proposed in many literatures [1]-[11]. Also development has been taken in view of symmetrical as well as asymmetrical based configurations. Generally, the source voltages are equal in symmetrical configuration. In asymmetrical configuration different rating of DC sources is used. A seven-level model using 3 DC sources, 6 switches and 2 diodes is proposed in [4]. A single dc source based cascaded seven-level inverter consisting of many switching devices and passive elements is given in [5]. Reduced device count multilevel inverter for DVR applications is also proposed in [7], [10]. Capacitor charging is one of the major concerns in balancing capacitor voltages and many topologies [12], [13] have been proposed with improved quality despite reduction in components. But reduction in part count indirectly increases device rating, reduces redundant states and lowers complex control structures. This motivates the authors to select a suitable topology with reduced part count and more levels, which will produce a better solution. Therefore, in this paper, an asymmetrical thirteen-level topology is proposed. A cascaded-H Bridge with auxiliary switches and DC sources is used to produce the desired output. The complete operation of the proposed topologies is presented elaborately. Moreover, the proposed topology is compared with the recently proposed topologies in terms of part count. To validate the feasibility of the proposed topology, the model is tested for different loading conditions using MATLAB software. Here the model is tested for different loading conditions. Finally, the simulated results are presented and compared with the experimental results to verify the effectiveness of the proposed topology.

P. Varalaxmi is with the Department of Electrical and Electronics engineering, Narayanamma Institute of Technology and Science, Hyderabad, India (e-mail: varalaxmiprathapagiri@gmail.com).

A. Kirubakaran is with the Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India (e-mail: a_kiruba81@rediffmail.com).

II. Proposed Topology

The proposed topology is simple in design and it has better performance when compared with other topologies. The schematic arrangement of the proposed thirteen-level asymmetrical cascaded H-bridge single phase inverter is shown in Fig. 1. It consists of twelve switches, four voltage sources and a load. The input DC sources are defined as V1=V2=Vdc and V3=V4=2Vdc. The sources having the same voltage are connected in series fashion to obtain the desired output voltage level. This is achieved with the help of four auxiliary switches T1, T2, T3 and T4, which are used to develop the levels and eight main switches are used for positive and negative level production. This can be further expanded by adding additional DC sources. The different switching states for the positive level production including zero stages is clearly expressed in Figs. 2 (a)-(g). The switching requirements for a cascaded H-bridge single phase inverter are shown in Table I. The switching sequence, current path and source combinations for the corresponding output voltage generation for different modes of operation are given in Table II. Assume,

- Number of switches = S
- Number of levels = N
- Number of dc voltage sources = V
- Number of H-bridges = n

The generalized expression for number of levels is given by: N = {V*(n+1)}+1.

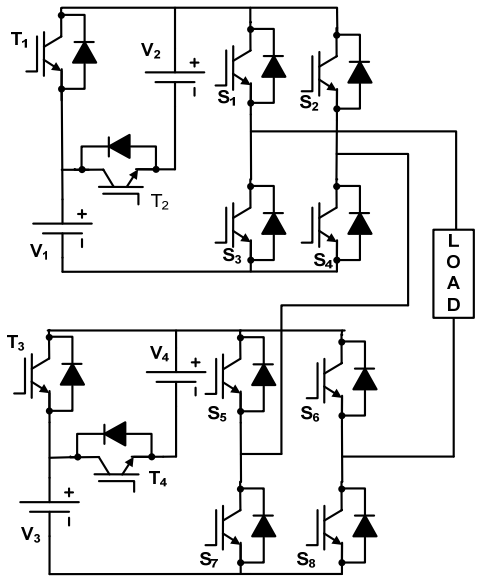


Fig. 1 Proposed thirteen-level inverter topology

TABLE I
SWITCHING REQUIREMENTS FOR CASCADED H- BRIDGE SINGLE PHASE INVERTER

No. of switches (S)	No. of levels (N)	No. of dc voltage sources (V)	No. of H-bridges (n)
6	5	2	1
12	13	4	2
18	25	6	3
24	41	8	4
30	61	10	5

The generalized expression for number of switches is given by: S= V*3

The output voltage is obtained by the sum of all DC voltage sources using:

$$V_{out} = V_1+V_2+V_3+V_4+\ldots\ldots\ldots\ldots+V_n \quad (1)$$

Mode 0: In this mode of operation, switches S_1, S_2 and S_5, S_6 are in ON state while the remaining switches are in OFF state. The voltage applied to the load is 0 V. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_6. The current path is shown in Fig. 2 (a). The combination of voltage sources is shown in Table II.

Mode 1: In this mode of operation, switches S_1, S_4 and S_5, S_6 are in ON state and the remaining switches are in OFF state. The voltage applied to the load is V_{dc}. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_6. The current path is shown in Fig. 2 (b). The combination of voltage sources is shown in Table II.

Mode 2: In this mode of operation, switches S_1, S_4 and S_5, S_6 are in ON condition while the remaining switches are in OFF condition. The voltage applied to the load is $2V_{dc}$. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_6. The current path is shown in Fig. 2 (c). The combination of voltage sources is shown in Table II.

Mode 3: In this mode of operation, switches S_1, S_4 and S_5, S_8 are in ON state while the remaining switches are in OFF state. The voltage applied to the load is $3V_{dc}$. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_8. The current path is shown in Fig. 2 (d). The combination of voltage sources is shown in Table II.

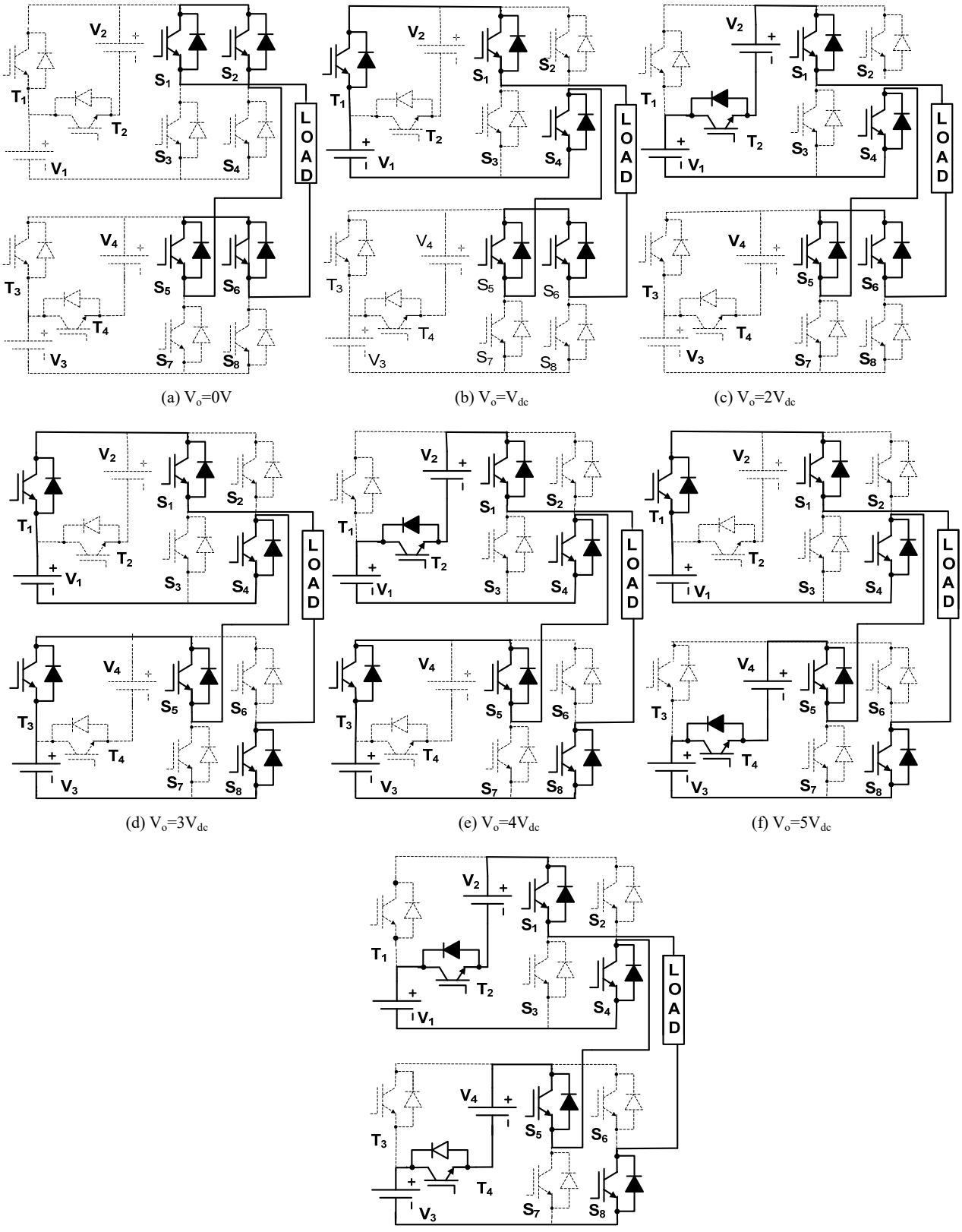
Mode 4: In this mode of operation, switches S_1, S_4 and S_5, S_8 are in ON state while the remaining switches are in OFF state. The voltage applied to the load is $4V_{dc}$. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_8. The current path is shown in Fig. 2 (e). The combination of voltage sources is shown in Table II.

Mode 5: In this mode of operation, switches S_1, S_4 and S_5, S_8 are in ON state while the remaining switches are in OFF state. The voltage applied to the load is $5V_{dc}$. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_8. The current path is shown in Fig. 2 (f). The combination of voltage sources is shown in Table II.

Mode 6: In this mode of operation switches S_1, S_4 and S_5, S_8 are in ON state while the remaining switches are in OFF state. The voltage applied to the load is $6V_{dc}$. The positive terminal of the load is connected to switch S_1 and the negative terminal is connected to switch S_8. The current path is shown in Fig. 2 (g). The combination of voltage sources is shown in Table II.

III. COMPARISON OF PROPOSED TOPOLOGY WITH OTHER RECENTLY PROPOSED TOPOLOGIES

This section shows the effectiveness of the proposed topology, for which a comparison is made with conventional topologies and also some recently proposed topologies. Table III clearly shows that the proposed topology has more significance in terms of component count as well as level generation when compared with other topologies. One can understand that the topologies proposed in [2] and [4] have significance when compared to the proposed topologies. However, the use of single H-bridge demands full voltage rating of switches and the voltage stress is also high. This problem is alleviated with the proposed topology and results in reduction in cost, volume and better performance of the proposed topology. Moreover, efficiency of the proposed topology is always high due to fewer number of conducting switching devices for every level generation as per Table II.



(a) V_o=0V (b) V_o=V_{dc} (c) V_o=$2V_{dc}$

(d) V_o=$3V_{dc}$ (e) V_o=$4V_{dc}$ (f) V_o=$5V_{dc}$

(g) V_o=6Vdc

Fig. 2 Different switching states of a thirteen level inverter circuit during positive half cycle

TABLE II
MODES OF OPERATION: SWITCHING SEQUENCE, CURRENT PATH, SOURCE COMBINATION AND OUTPUT VOLTAGE

Topology	NPC	FC	CHB	Topology [7]	Topology [8]	Topology [2]	Topology [4]	Topology [3]	Proposed topology
Output voltage levels	13	13	13	13	13	13	13	13	13
Clamping diodes	120	0	0	0	0	0	0	0	0
Flying capacitor	0	66	0	0	0	0	0	0	0
DC_ link capacitors	11	12	0	0	0	0	0	0	0
Main Switches	24	24	24	15	14	12	12	14	12
DC source	1	6	6	6	6	4	4	4	4

TABLE III
COMPARISON BETWEEN PROPOSED TOPOLOGY AND OTHER TOPOLOGIES

Modes		Switching Sequence												Current path	Source combination	Output voltage
		T_1	T_2	T_3	T_4	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8			
Positive level	1	1	0	0	0	1	0	0	1	1	1	0	0	T_1-S_4-S_5-S_6-S_1	V_1	V_{dc}
	2	0	1	0	0	1	0	0	1	1	1	0	0	T_2-S_4-S_5-S_6-S_1	V_1+V_2	$2V_{dc}$
	3	1	0	1	0	1	0	0	1	1	0	0	1	T_1-S_4-S_5-T_3-S_8-S_1	V_1+V_3	$3V_{dc}$
	4	0	1	1	0	1	0	0	1	1	0	0	1	T_2-S_4-S_5-T_3-S_8-S_1	V_1+V_2+V_3	$4V_{dc}$
	5	1	0	0	1	1	0	0	1	1	0	0	1	T_1-S_4-S_5-T_3-S_8-S_1	V_3+V_2'+V_1	$5V_{dc}$
	6	0	1	0	1	1	0	0	0	1	1	0	1	T_2-S_4-S_5-T_3-S_8-S_1	V_1+V_2+V_3+V_4	$6V_{dc}$
Zero level		0	0	0	0	1	1	0	0	1	1	0	0	S_2-S_5-S_6-S_1	-	0
		0	0	0	0	0	0	1	1	0	0	1	1	S_4-S_7-S_8-S_3	-	0
Negative Level	1	1	0	0	0	0	1	1	0	1	1	0	0	T_1-S_2-S_5-S_6-S_3	V_1	V_{dc}
	2	0	1	0	0	0	1	1	0	1	1	0	0	T_2-S_2-S_5-S_6-S_3	V_1+V_2	$2V_{dc}$
	3	1	0	1	0	0	1	1	0	0	1	1	0	T_1-S_2-S_7-T_3-S_6-S_3	V_1+V_3	$3V_{dc}$
	4	0	1	1	0	0	1	1	0	0	1	1	0	T_2-S_2-S_7-T_3-S_6-S_3	V_1+V_2+V_3	$4V_{dc}$
	5	1	0	0	1	0	1	1	0	0	1	1	0	T_1-S_2-S_7-T_4-S_6-S_3	V_1+V_3+V_4	$5V_{dc}$
	6	0	1	0	1	0	1	1	0	0	1	1	0	T_2-S_2-S_7-T_4-S_6-S_3	V_1+V_2+V_3+V_4	$6V_{dc}$

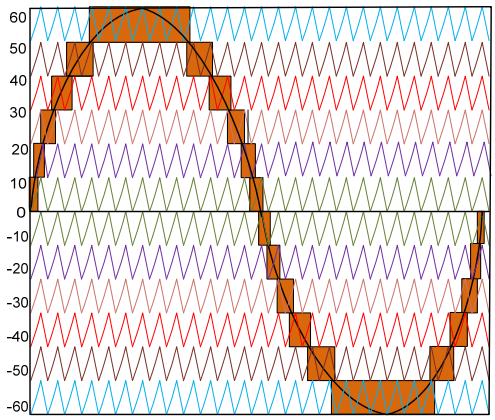
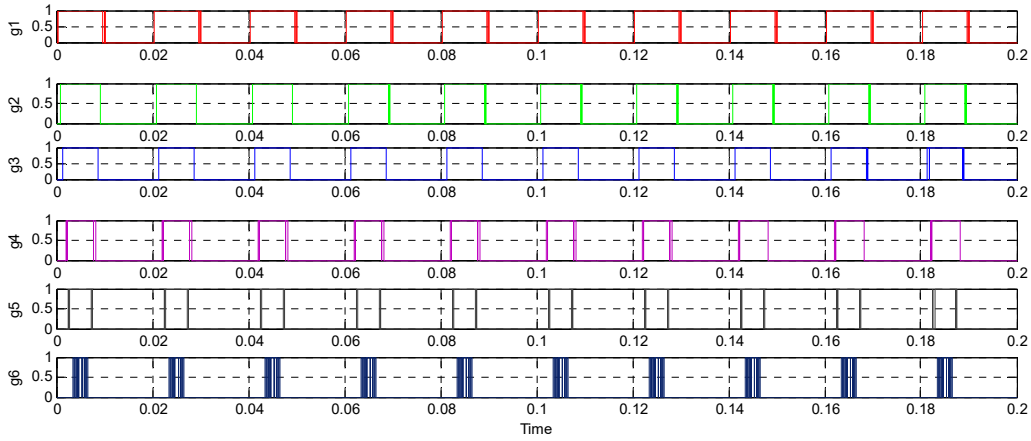


Fig. 3 The output voltage waveform along with twelve carrier waveforms

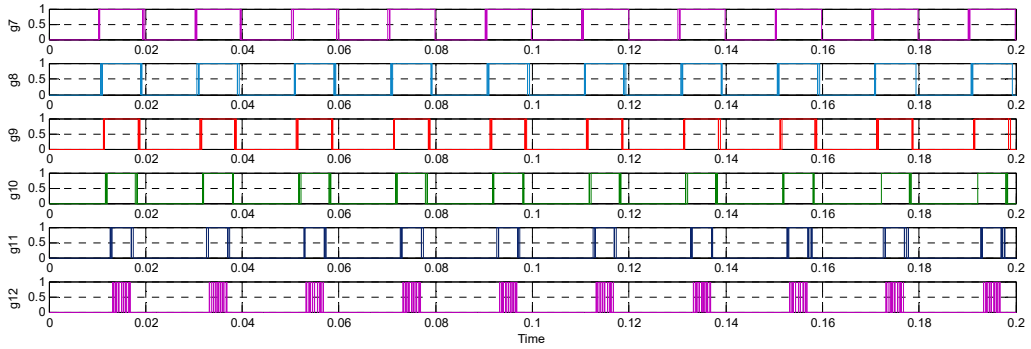
IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the feasibility of the proposed model, the simulation work is carried out in MATLAB simulation software. The proposed model is developed with DC source voltages of V1=V2=Vdc and V3=V4=2Vdc, Vdc of 10 V and a switching frequency of 5 kHz. The MOSFET switch used in this topology is IRF640. The fundamental sample time of 5 micro second is considered and the modulation index value of 0.98 is taken with fundamental frequency of 50 Hz and the same is compared with the twelve carrier signals to produce the required output level.

Figs. 6 (a) & (b) depict the control pulses generated for various switches during positive and negative half cycle respectively. Fig. 7 shows the simulated inverter output voltage and current waveforms for R load of 20 Ω. Similarly, Fig. 8 shows the simulated output voltage and current waveforms for RL load of 20 Ω and 10 mH. The %THD of the simulated output voltage and current waveform is given in Figs. 9 (a) & (b). The dominating voltage THD can be eliminated by using a suitable filter between inverter output and load components. However, the current THD is within limits. Further, an experimental setup is developed with the available lower rating components in the laboratory as shown in Fig. 10 (a). An attempt is made to prove that the level generation is more efficient based on theoretical and simulation analysis. IRF640 Mosfet devices have been used to develop the power circuit, and the control pulses generated using Spartan 6 FPGA using Xilinx system generator blocks in MATLAB environment. The FPGA output control pulses are stepped up to 15 V pulses using TLP250 opto-coupler ICs to amplify as well as to provide isolation between the signals. Fig. 10 (b) illustrates the experimental output voltage and current waveforms, and Fig. 10 (c) shows %THD of current waveforms. From these results we can say that the simulated and experimental waveforms are almost same, so that better performance of the topology can be ensured.



(a)



(b)

Fig. 6 Switching pulses for (a) positive and (b) negative half cycles

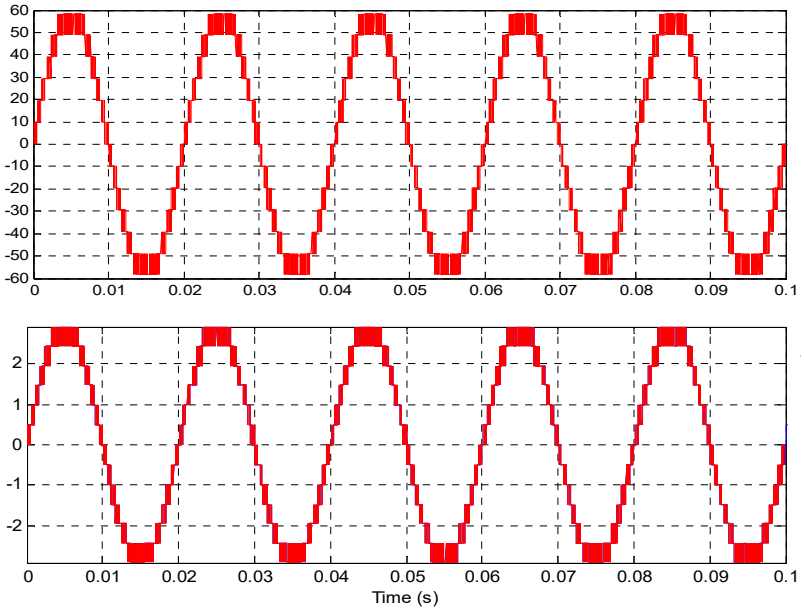


Fig. 7 Output voltage and current waveforms for R=20 Ω

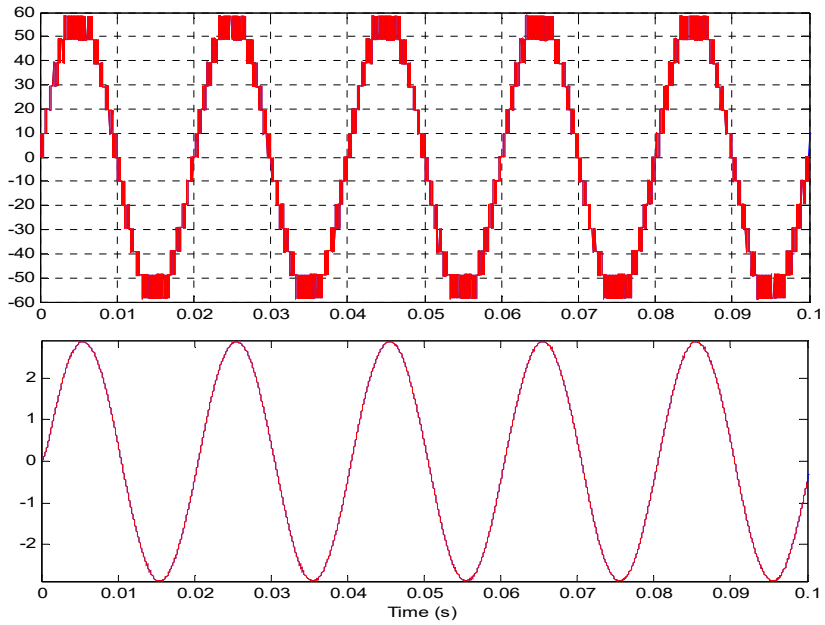
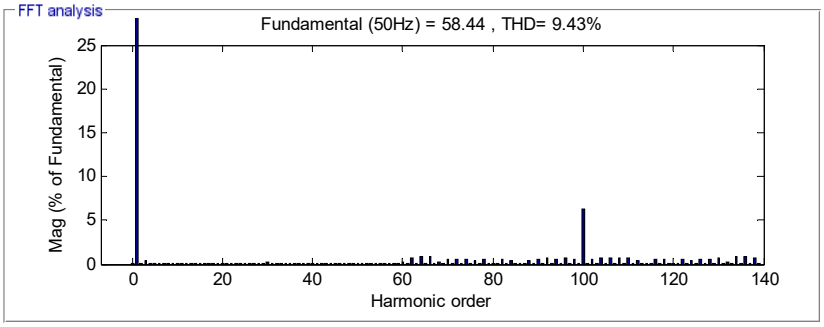
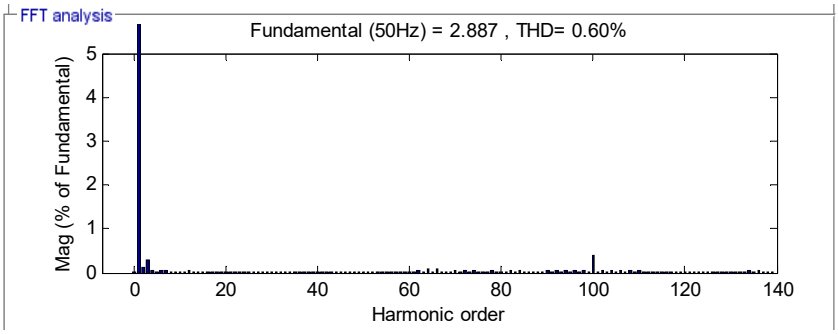


Fig. 8 Output voltage and current waveforms for R=20 Ω & L=10 mH

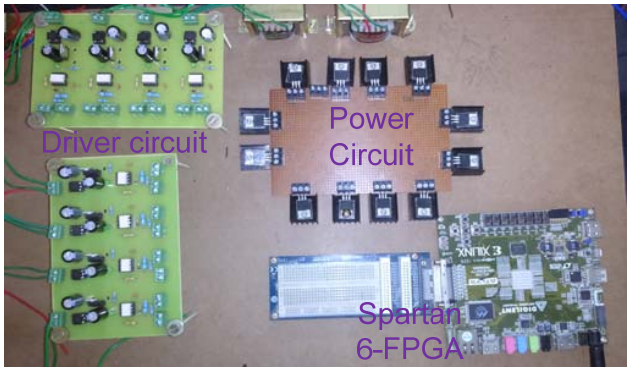


(a)

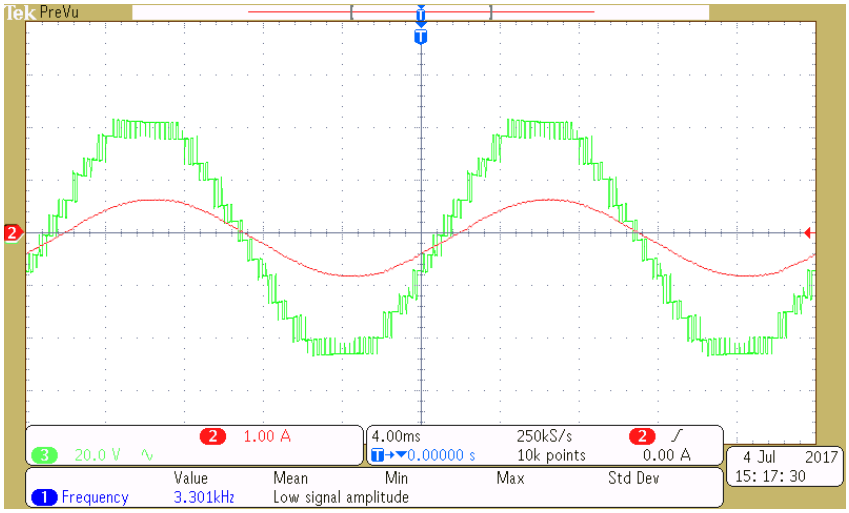


(b)

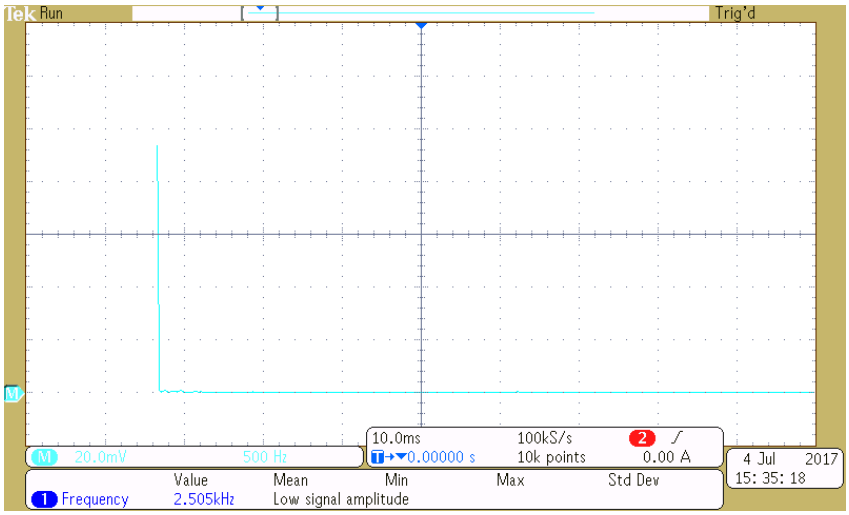
Fig. 9 %THD for output current waveform for (a) R=20 Ω and (b) R=20 Ω and L=10 mH



(a)



(b)



(c)

Fig. 10 (a) Experimental setup, (b) Experimental results of voltage and current waveforms and (c) % current THD

V. Conclusion

A thirteen-level asymmetrical single phase inverter has been presented. The proposed configuration is explored with neat diagrams for different mode of level generation. A comparison

is also made with conventional and other recent topologies. The simulation work is carried out in MATLAB software to verify the concept of the proposed topology. Finally extensive simulation results are presented for different loading conditions and the experimental results are also presented. The output voltage and current waveforms have good agreement with each other which validates the performance of the proposed topology.

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