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Investigation of Threshold Voltage Shift in Gamma Irradiated N-Channel and P-Channel MOS Transistors of CD4007

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Abstract**—**The ionizing radiations cause different kinds of damages in electronic components. MOSFETs, most common transistors in today's digital and analog circuits, are severely sensitive to TID damage. In this work, the threshold voltage shift of CD4007 device, which is an integrated circuit including P-channel and N-channel MOS transistors, was investigated for low dose gamma irradiation under different gate bias voltages. We used linear extrapolation method to extract threshold voltage from I_D-V_G characteristic curve. The results showed that the threshold voltage shift was approximately 27.5 mV/Gy for N-channel and 3.5 mV/Gy for P-channel transistors at the gate bias of |9 V| after irradiation by Co-60 gamma ray source. Although the sensitivity of the devices under test were strongly dependent to biasing condition and transistor type, the threshold voltage shifted linearly versus accumulated dose in all cases. The overall results show that the application of CD4007 as an electronic buffer in a radiation therapy system is limited by TID damage. However, this integrated circuit can be used as a cheap and sensitive radiation dosimeter for accumulated dose measurement in radiation therapy systems.

Keywords**—**Threshold voltage shift, MOS transistor, linear extrapolation, gamma irradiation.

I. Introduction

ELECTRONIC devices based on Metal-Oxide-Semiconductor (MOS) technologies are widely used in the environments with high level of ionizing radiation such as radiation therapy and radiology systems, space, accelerators, and nuclear power plants. Total ionizing dose (TID) affects such devices and leads to threshold voltage shifts, trans-conductance variations, and increase in leakage current [1]-[4]. In addition, these devices are commonly applied as dosimeters in radiation therapy applications [5], [6].

MOS devices are susceptible to be damaged by ionizing radiation resulting from charge buildup in gate, field and SOI buried oxides. As ionizing radiation passes through the gate oxide, energy is transferred from high energy photons and charged particles to generate electron-hole pairs. The amount of energy deposited by ionizing radiation is referred to as TID and is defined as the absorbed energy per unit mass of a material. The generated charges in the gate oxide will transport to the gate electrode and Si/SiO_2 interface. Following this process, some fractions will recombine and consequently reduce the initial density of the free charged carriers. A very short time window is available for the initial recombination processes to occur, since the electron mobility is considerably more than hole mobility in SiO_2. Therefore, it is quickly removed from the oxide layer [7].

The hole trapping that occurs at defect sites is generally associated with oxygen vacancies in SiO_2 creating oxide-trapped charge. In conventional gate oxides, the distribution of trapped holes is normally within a few nanometers of the Si/SiO_2 interface [8].

In this work, the radiation-induced degradation parameters for gamma irradiated N-channel and P-channel MOS transistors belonging to CD4007 device have been investigated. Since the gate bias affects the sensitivity of transistors, the results were obtained in three different gate biases. The drain current to gate voltage transfer characteristic in linear region was utilized to extract threshold voltage. In addition, the temperature dependence coefficient of transistors has been measured to compensate the temperature effect on threshold voltage shift. Although other works have examined the response of CD4007 device to ionizing radiation, the threshold voltage shift has not been studied with linear extrapolation method [9], [10].

II. Materials and Methods

Experimental data were attained from irradiation experiments performed on N-channel and P-channel MOS transistors belonging to CD4007 device. As shown in Fig. 1, CD4007 integrated circuit device includes three N-channel and three P-channel MOS transistors. This device is one of the most widely used components in the electronic applications. The gate oxide thickness of these transistors is approximately 120 nm which represents relatively thick oxide layer and increases the sensitivity of transistor to TID effect [11].

The devices under test were irradiated by a Co-60 gamma source at a dose rate of approximately 7.18 Gy/hr (in SiO_2). The threshold voltages were measured immediately after irradiation at several different total doses up to 28.72 Gy. The N-channel transistors were biased at three different gate voltages of Vg=0V, Vg=+3.3V, and Vg=+9V, while the P-channel transistors were biased at three different gate voltages Vg=0V, Vg=-3.3V, and Vg=-9V. The gate voltage was set by the HAMEG 4030 power supply. The results were obtained by averaging the parameters which were measured for nine transistors in each dose level and bias condition. Irradiation was carried out at temperatures between 17-18 °C.

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There are various methods to extract transistor threshold voltage in linear operating region such as ELR (linear extrapolation), GMLE (Trans-conductance extrapolation), SD (Second-derivative), RM (Ratio method) and so on. Drain current versus gate voltage transfer characteristics of device is necessary in these methods. Nonetheless, there are another methods to extract threshold voltage based on measuring a constant current [12].

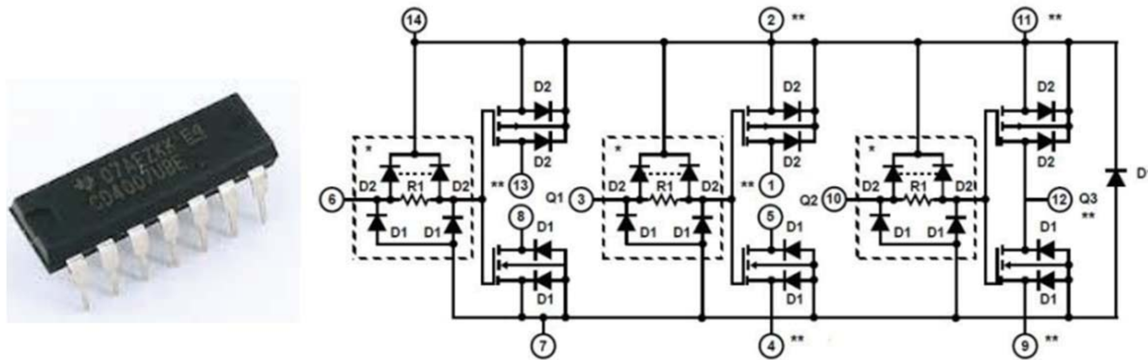


Fig. 1 The view of CD4007 integrated circuit and internal structure

In this work, extrapolation in the Linear Region method (ELR) was used as an accurate and promising method to extract transistor threshold voltage. The $I_D - V_G$ characteristic of the transistors was measured before and after irradiation at room temperature. The voltage of drain–source electrodes was set to 10 mV for measurement in linear operating region.

The relation between drain current and gate voltage for such a biasing condition can be expressed by (1) [13]:

$$I_D \cong \frac{\mu w C_{ox}}{L}(V_{GS} - V_{Th})V_{DS} \quad (1)$$

where μ, w, C_{ox}, L, V_{DS}, V_{GS}, V_{Th}, and I_D are mobility of carriers in channel, width of channel, capacitance of oxide layer per unit area, length of channel, voltage across drain and source terminals, voltage across gate and source terminals, threshold voltage, and drain current, respectively. The threshold voltage depends linearly on the temperature according to (2) [13]:

$$V_{Th}(T_2) = V_{Th}(T_1) - k(T_2 - T_1) \quad (2)$$

where T_2, T_1, and k are current temperature, initial temperature and temperature coefficient respectively. The two integrated circuits have been tested under different temperatures to measure temperature coefficient. Furthermore, the temperature of each component has been recorded with accuracy of 0.1 °C during I-V characteristic measurement.

III. Results and Discussion

The drain current as a function of gate voltage characteristic for N-channel transistor of CD4007 before irradiation is shown in Fig. 2. Since the threshold voltage is obtained by extrapolation in linear operating region, a line has been fitted to the $I_D - V_G$ curve at the maximum point of trans-conductance curve. Based on (1), the threshold voltage can be extracted by intersection point of fitted line with gate voltage axis.

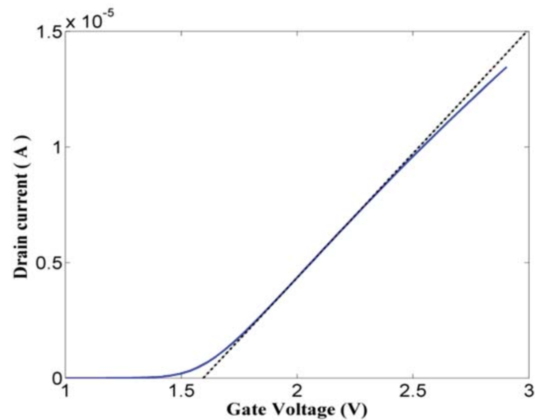


Fig. 2 Drain current versus gate voltage transfer characteristics of CD4007 N-channel transistor (solid line), and fitted curve based on (1) (dotted line)

The temperature dependency of threshold voltage for N-channel and P-channel transistors of CD4007 is shown in Fig. 3. The integrated circuit and transistors have been indicated by ICx and Tx, respectively. It can be seen that the threshold voltage linearly decreases with temperature. The measured temperature coefficients are 2±0.2 mV/°C and 3.5±0.3 mV/°C for P-channel and N-channel transistors, respectively.

Fig. 4 shows $I_D - V_G$ characteristic of N and P-channel transistors before and after different irradiation doses under +9 V and -9 V gate bias. As depicted, both of the N and P-channel transistor curves have been shifted to the left after irradiation. Since the threshold voltage is directly related to the amount of the flat band voltage, this voltage is useful to explain the behavior. Therefore, if there is no extra charge on the oxide layer, the flat band voltage will be equal to the difference between gate electrode and silicon substrate work functions. However, the trapped charge density in the oxide layer increases after irradiation. The trapped charges are positive which make the flat band voltage more negative in

both of N and P-channel transistors. The threshold voltage shifts are -792 mV and -99.9 mV for N and P-channel transistor respectively at total dose of 28.72 Gy.

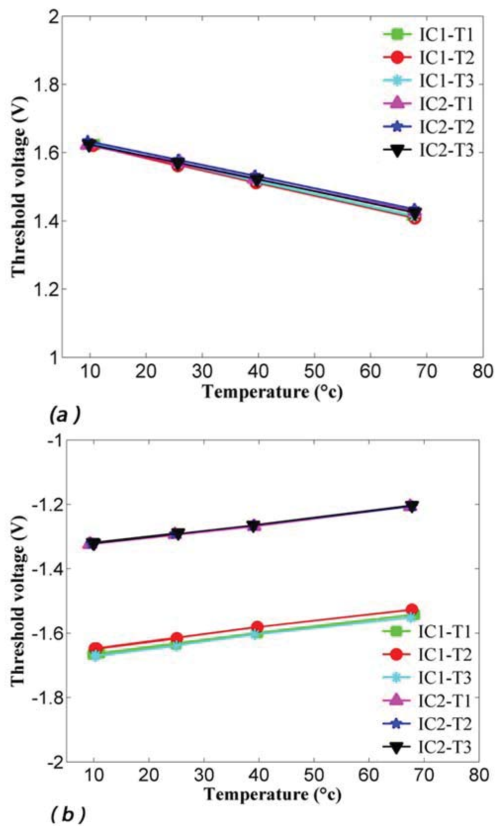


Fig. 3 Dependency of threshold voltage on temperature for (a) N-channel transistors, (b) P-channel transistors of CD4007

The trans-conductance versus gate voltage characteristic of transistors before and after irradiation under 9 V gate bias is shown in Fig. 5. It is noticeable that the maximum of trans-conductance curve has been decreased 8% for N-channel transistors, while this is about 1.5% for P-channels. This behavior is explained by accumulation of extra charges near Si/SiO_2 interface and creation of trapped energy levels and scattering centers after irradiation. Ionizing radiation can generate electron-hole in oxide layer and release protons from the precursor of the radiation-induced interface trap. The positive gate voltage causes to move the holes and protons toward Si/SiO_2 interface in N-channel transistors, while the negative gate voltage make them away from interface in P-channel transistors. Therefore, the density of accumulated holes near Si/SiO_2 interface for N-channel is higher than P-channel transistors.

The threshold voltage was extracted according to the described method (ELR) for N-channel and P-channel transistors biased at three different gate voltages during irradiation. As shown in Fig. 6, the positive biased N-channel transistors are approximately 7.9 times more sensitive than negative biased P-channel transistors. Moreover, the threshold voltage shift of positive biased N-channel transistor is about 69% more than zero bias condition, whereas applying negative bias causes to decrease the threshold voltage shift of P-channel transistor about 170%. Applying the positive bias increases N-channel threshold voltage shift as much as 69%, while negative bias on P-channel transistors reduces the sensitivity by a factor of 2.7.

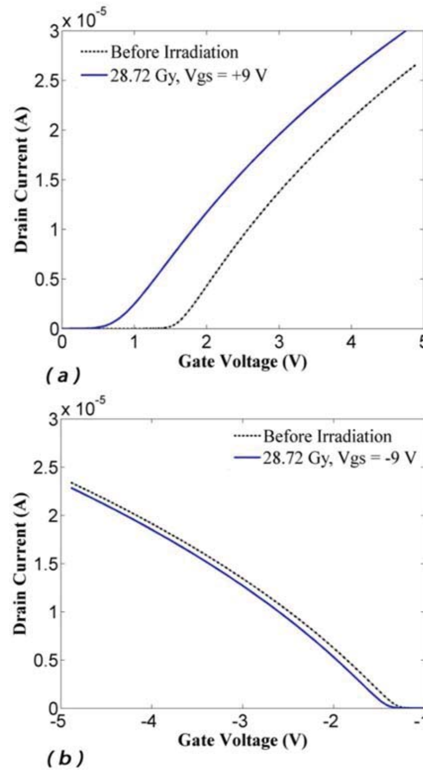
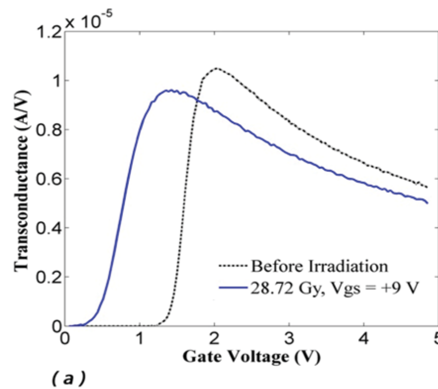


Fig. 4 Drain current versus gate voltage characteristic before and after irradiation dose of 28.72 Gy under 9 V gate bias, (a) for N-channel transistor, (b) for P-channel transistor



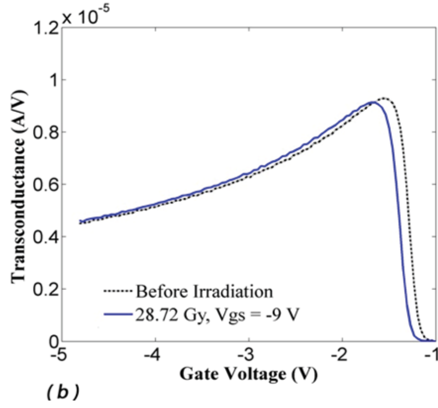


Fig. 5 Trans-conductance versus gate voltage characteristic before and after irradiation of 28.72 Gy and under 9 V gate bias, (a) for N-channel transistor, (b) for P-channel transistor

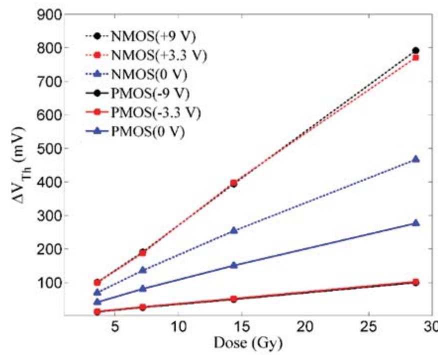


Fig. 6 The threshold voltage shift of transistors in different doses and biases

The detailed values of threshold voltage shift at different bias conditions during irradiation are summarized in Table I. The highest sensitivity of 27.57 mV/Gy was recorded for N-channel transistor with positive bias of 9 V. The lowest sensitivity of 3.5 mV/Gy was corresponding to the P-channel transistor under negative bias of - 9 V.

TABLE I
THE THRESHOLD VOLTAGE SHIFT CHARACTERISTIC FOR CD4007 TRANSISTORS DURING IRRADIATION

		Total Dose (Gy)			
		3.59	7.18	14.36	28.7
-ΔVT± SD (mV) For N-type Bias	9 V	101±1.1	191±1.2	394±1.3	792±3.1
	3.3 V	99.8±0.2	188±0.8	398±0.5	771±2.5
	0 V	69.8±0.5	136±1.1	254±1	467±3.7
-ΔVT± SD (mV) For P-type Bias	0 V	41.28±0.2	81.13±0.6	150.78±1	276.8±4
	-3.3 V	13.89±0.3	27.64±0.4	51.98±0.5	102.8±0.6
	-9 V	12.6±0.4	26.13±0.4	49.54±1.2	99.94±1

The relation between the distribution of the charges and threshold voltage shift in the oxide layer is given by (3) [14]:

$$\Delta V_{Th} = -\frac{q}{C_{ox}}\int_0^{d_{ox}} \frac{zN_t(z)}{d_{ox}}dz \quad (3)$$

where, z, d_{ox}, q, and $N_t(z)$ are distance from gate electrode, thickness of oxide layer, charge of electron and the density distribution of trapped holes along z axis, respectively. According to (3), the accumulated charges near Si/SiO_2 interface make a larger variation in threshold voltage than those accumulated near $Gate/SiO_2$ interface.

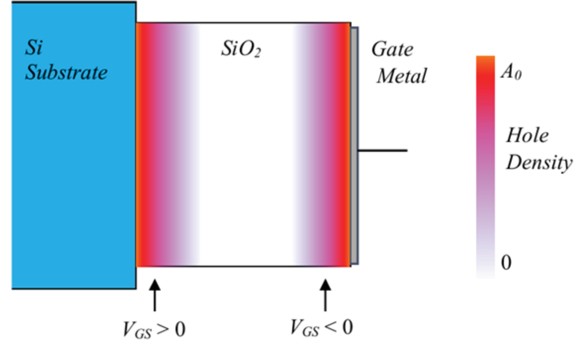


Fig. 7 The trapped charge distribution in oxide layer for positive and negative bias condition

The actual distribution of the holes depends on different factors such as bias condition, irradiation temperature, oxide intrinsic characteristics, and so on. Some of methods are used to obtain the hole distribution, and one of them is the etch-back method [15]-[18]. This method proposes an exponential function as an appropriate estimation for the trapped hole distribution. Fig. 7 schematically shows the density of trapped holes in the oxide layer under positive and negative gate biases. Since the positive charges move in the direction of the electric field, the holes are accumulated near Si/SiO_2 interface and the gate electrode for positive and negative bias conditions, respectively. Therefore, an exponential distribution has been applied for the buildup of radiation-induced oxide trapped charges as expressed in (4):

$$N_t(z) = A_0 \times \exp\left(-\frac{z}{\tau}\right) \quad \text{for } V_{GS} < 0 \quad (4A)$$

$$N_t(z) = A_0 \times \exp\left(-\frac{d_{ox} - z}{\tau}\right) \quad \text{for } V_{GS} > 0 \quad (4B)$$

where, A_0 is the maximum density of the holes, and τ is the distribution constant. In addition, the density of escaped holes from the initial recombination can be determined as (5):

$$Q\left(\frac{\#}{cm^3}\right) = \frac{D(Gy)\times \rho\left(\frac{kg}{cm^3}\right)\times \eta}{\varepsilon_{e-h}(eV)\times 1.6\times 10^{-19}\left(\frac{J}{eV}\right)} \quad (5)$$

where D, ρ, η, ε_{e-h} are absorbed dose in SiO_2, mass density of SiO_2 (~$2.27 \times 10^{-3}\ kg/cm^3$), the fraction of escaped holes and the energy required to generate an electron-hole pair in SiO_2, respectively. The fraction of escaped holes is strongly dependent on the magnitude of the oxide electric field acting upon the generated charge pairs [7], [19]-[21]. A higher field will tend to rapidly separate electrons and holes and therefore suppress recombination. At an applying bias of 9 V on 120 nm gate oxide, the fraction of escaped holes is around 70% for the

case of Co-60 irradiation. The average value of ε_{e-h} was determined by Ausman and McLean to be about 18 eV [22]. Therefore, the density of the holes is about $5.51 \times 10^{14}\ e-h/cm^3$ for the absorbed dose of 1 Gy.

The combination of (3)-(5) will obtain a correlation between the threshold voltage shift, the maximum density of holes and the distribution constant. These factors are shown in Fig. 8 for the absorbed dose of 1 Gy. Therefore, the illustrated factors have been calculated for the negative and positive gate bias as well as the maximum density of trapped holes. At the positive gate bias, an exponential hole distribution near the Si/SiO_2 interface with τ of 31 nm and A_0 of $2.13 \times 10^{15}\ hole/cm^3$ causes to shift of 27.5 mV in threshold voltage. Furthermore, the threshold voltage shift of 3.5 mV can be occurred at negative gate bias for an exponential hole distribution near the gate electrode with τ of 37 nm and A_0 of $1.8 \times 10^{15}\ hole/cm^3$.

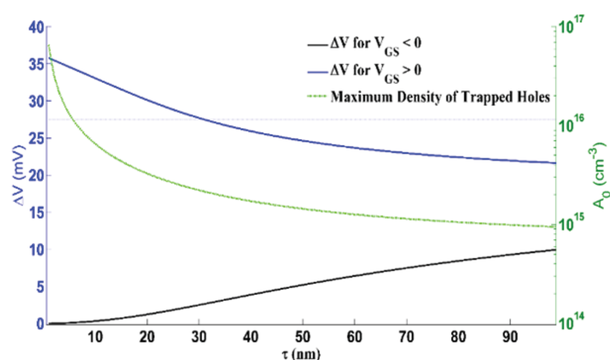


Fig. 8 The threshold voltage shift and maximum density of trapped hole attained from exponential distribution for 1 Gy dose

IV. Conclusion

The $I_D - V_G$ characteristics of CD4007 transistors have been measured in the linear operating region. These measurements were carried out before and after irradiation of Co-60 gamma source in different gate biases. The linear extrapolation method was utilized to extract the threshold voltage of transistors. Moreover, the measured temperature coefficients have been used for compensation of the threshold voltage dependency with temperature.

The threshold voltage shift for P-channel transistor was -99.9 mV, while it was -792 mV for N-channel transistors at total dose of 28.72 Gy. The results showed that the positive biased N-channel transistors are more sensitive to TID rather than P-channel MOS transistors. The obtained sensitivity was about 3.5 mV/Gy for P-channel and 27.5 mV/Gy for N-channel transistors at the gate bias of -9 V and 9V, respectively. This level of sensitivity limits the application of CD4007 in electronic circuits of radiation therapy systems. The threshold voltage shift for both of N-channel and P-channel revealed a linear relation respect to total ionization dose of 28.7 Gy. This feature nominates the CD4007 as an appropriate radiation dosimeter for low dose measurement.

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