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Rail-To-Rail Output Op-Amp Design with Negative Miller Capacitance Compensation

Muhaned Zaidi, Ian Grout, Abu Khari bin A'ain

***Abstract*—**In this paper, a two-stage op-amp design is considered using both Miller and negative Miller compensation techniques. The first op-amp design uses Miller compensation around the second amplification stage, whilst the second op-amp design uses negative Miller compensation around the first stage and Miller compensation around the second amplification stage. The aims of this work were to compare the gain and phase margins obtained using the different compensation techniques and identify the ability to choose either compensation technique based on a particular set of design requirements. The two op-amp designs created are based on the same two-stage rail-to-rail output CMOS op-amp architecture where the first stage of the op-amp consists of differential input and cascode circuits, and the second stage is a class AB amplifier. The op-amps have been designed using a 0.35μm CMOS fabrication process.

***Keywords*—**Op-amp, rail-to-rail output, Miller compensation, negative Miller capacitance.

I. Introduction

IN many electronic circuit designs, the operational amplifier (op-amp) is an important circuit building block. The op-amp is a differential input amplifier circuit that uses external feedback to create useful circuits such as buffers, comparators, oscillators, instrumentation amplifiers and filters. The move over the last number of years has been to operate the op-amp on lower power supply voltages and with single rail operation whilst utilizing lower geometry fabrication processes. However, reducing the supply voltage and transistor sizes has an effect on the design operation characteristics such as stability and frequency response. Various circuit architectures have considered these concerns in order to reduce performance related problems [1]-[4]. In general, Miller compensation is used to improve the stability and frequency response of the op-amp.

The Miller effect can be realized in two ways within a CMOS (complementary metal oxide semiconductor) analogue amplifier circuit using the metal oxide semiconductor field effect transistor (MOSFET); firstly, through the structure of the MOSFET as shown Fig. 1. The MOSFET has five capacitances between its drain (D), gate (G), source (S), and bulk (B) terminals. The overlap capacitance between the gate and the drain (Cgd) creates a feedback between the gate input and the drain output nodes. Although Cgd typically is a small capacitance value, it will however have an effect on the high-frequency response of the amplifier. The capacitance Cgd is called the Miller effect or Miller capacitance.

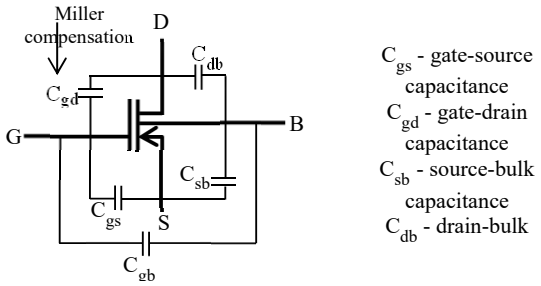


Fig. 1 Structure of the MOSFET

Secondly, it can be performed by adding an external capacitor (C_M) around the second stage of the conventional two-stage CMOS op-amp as shown in Fig. 2. In this figure, the external Miller capacitor (C_M) is connected to the second stage, although the capacitor could also be connected around the first stage or around the complete amplifier circuit.

In this paper, Miller compensation is considered by firstly using conventional Miller compensation and secondly by using a combination of Miller and negative Miller compensation. The target amplifier is a two-stage rail-to-rail output CMOS op-amp operating on a +3.3 V single rail power supply. The paper is organized as follows. Section II will introduce Miller theory and Miller compensation with its extension to negative Miller compensation. Section III will introduce the two-stage CMOS op-amp design with rail-to-rail output operation using the AMS 0.35 μm CMOS technology. Section IV will present the implementation of negative Miller capacitance and simulation of the op-amp using the Spectre simulator with typical transistor models.

Muhaned Zaidi is with the Department of Electronic and Computer Engineering, University of Limerick, Limerick, Ireland and University of Wasit, Wasit, Iraq. (phone: 00-353-61-202298, fax: 00-353-61-338176, e-mail: muhaned.zaidi@ul.ie).

Ian Grout is with the Department of Electronic and Computer Engineering, University of Limerick, Limerick, Ireland (e-mail: ian.grout@ul.ie).

Abu Khari A'ain is with the Faculty of Electrical Engineering, Universiti Teknologi Malaysia, Skudai, Malaysia (e-mail: abu@fke.utm.my).

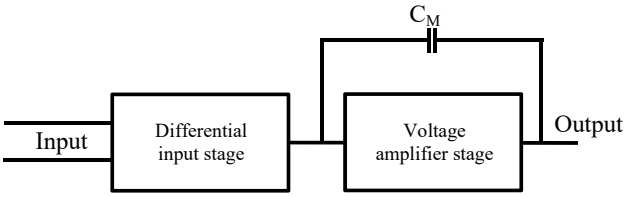


Fig. 2 Conceptual system block diagram with Miller compensation around the second voltage amplifier stage

II. Miller Theory

A. Miller Compensation

For a two-stage op-amp design, Miller compensation is typically accomplished by connecting an external Miller capacitor between the output of the second stage and output of first stage transistors as shown in Fig. 2. As identified in [2], the Miller capacitor can be modelled as an impedance connected from the output of the differential input stage to ground (GND) and a second impedance connected from the output stage to ground. This principle is shown in Fig. 3.

The capacitor on the input node has a capacitance value of C(1 + A) and the capacitor on the output has a capacitance value of C(1 + 1/A), where A is the voltage gain of the second stage. An advantage of this is that the dominant pole is shifted downwards to a lower frequency and the non-dominant pole is shifted upwards to a higher frequency [4], which leads to improved amplifier stability but with an associated reduction in the unity gain frequency.

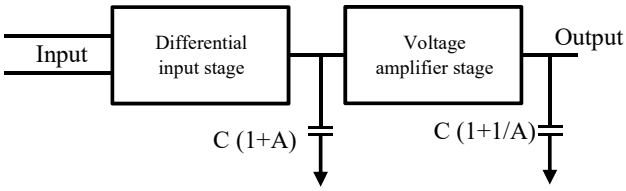


Fig. 3 Gain stage with Miller capacitance equivalent

B. Negative Miller Compensation

Within each MOSFET, parasitic capacitances are present which will limit the speed of operation of any circuit using the MOSFET [5]. Negative Miller compensation has been demonstrated to reduce this unwanted effect. Negative Miller compensation uses the idea of negative capacitance which has a unique property that its voltage falls when the capacitor charges [6]. Negative Miller compensation has been discussed widely in various text books and scientific articles including [1]-[3], [6]-[8].

A negative Miller capacitance (C_{NM}) is useful to cancel or remove the effect of any parasitic capacitances by using the advantage of the Miller effect. The Miller effect is one way to create the negative capacitance. Negative capacitance is created by connecting a regular capacitor across a non-inverting amplifier with a gain >> 1 [6]. In a fully differential amplifier, this is achieved by connecting capacitors between the non-inverting output to the negative input and inverting output to positive input [7]-[9]. Fig. 4 shows how this idea can be achieved in order to reduce the input capacitance of a differential stage. By adding the feedback capacitors of equal value (C_{NM}), the original input capacitance at each input node (with reference to GND) is reduced, and an improvement of op-amp unity gain frequency and phase margin is achieved [3].

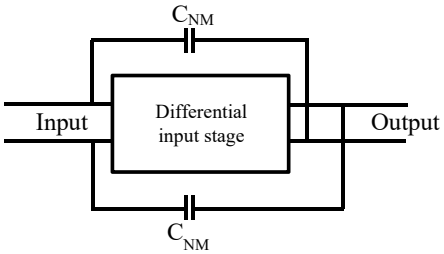


Fig. 4 Schematic of differential input with negative Miller capacitance

Fig. 5 shows the differential amplifier with a differential input (Vin(+) and Vin(-)) and a differential output (Vout(+) and Vout(-)). The capacitances C_{NM} are connected between Vout(+) with Vin(-) , and Vout(-) with Vin(+). If the feedback capacitance C_{NM} is much larger than amplifier input capacitance, the gain bandwidth improvement will be limited by the output load capacitance C_L. Cancelling the effect of a large capacitance will require a large feedback capacitor C_{NM}.

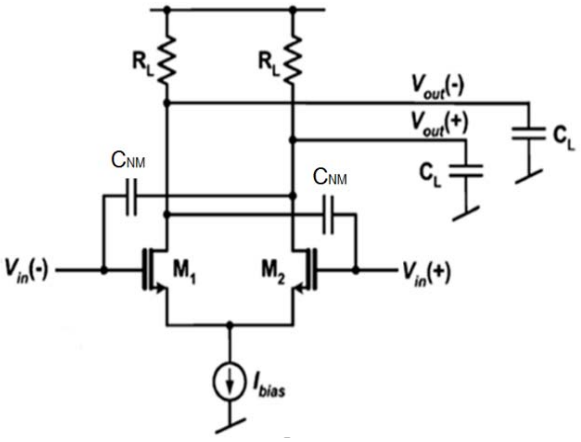


Fig. 5 Differential input stage with negative Miller compensation [7]

This means that a suitable differential amplifier performance (phase margin and unity gain frequency) can be achieved if load capacitance C_L is small. If a high voltage gain of the gain stage is created by a large op-amp output resistance, the bandwidth can be significantly improved with negative capacitance. The expression for the effective input capacitance for each input node, C_{eff}, without C_{NM} is given by:

$$C_{eff} = C_{gs} + C_{gd}(1 - A) \quad (1)$$

In (1), if the amplifier voltage gain A >> 1, the inclusion of negative Miller capacitance shows that the effective input capacitance is reduced [6]. To achieve a negative Miller capacitance, C_{NM} can be added between the amplifier inputs and outputs [10]. However, the charge on this additional capacitor is shared with the C_{gd} capacitance and:

$$C_{eff} = C_{gs} + C_{gd}(1 - A) + C_{NM}(1 - (-A)) \quad (2)$$

Assuming that C_{NM} is approximately equal to C_{gd} then:

$$C_{eff} \approx C_{gs} + 2C_{gd} \quad (3)$$

Thus, as long as the amplifier gain is much greater than 1, a reduction in the effective input capacitance is achieved.

III. Amplifier Structure

A. Cascode Circuit

In the previous section, Miller capacitance and negative Miller capacitance have been considered within an amplifier design of the form shown in Fig. 6. To obtain a high output voltage range using a CMOS technology, a cascode circuit can be employed. The cascode circuit has a transconductance (g_m) equal to that of one input transistor and the DC bias current. The mirror current connected transistors in the cascode circuits have the same currents as the differential stage input transistors; otherwise, the tail current is greater than the current of the input stage. A high g_m for the differential input stage provides a high unity gain frequency.

The unity gain frequency is given by:

$$f_{odB} = \frac{g_m}{C_c} \quad (4)$$

If the transconductance in (4) is a small value, the unity gain frequency will be high while the phase margin (PM) is decreased according to:

$$PM = 180° - \tan^{-1}\frac{f_{odB}}{Z} - \tan^{-1}\frac{f_{odB}}{P_1} - \tan^{-1}\frac{f_{odB}}{P_2} \quad (5)$$

where P_1, P_2 and Z are first pole, second pole, and zero pole values, respectively. However, the lower currents in the bottom set of current source transistors and upper mirror transistors allow these transistors to have a lower W/L ratio in strong inversion at the same saturation voltages [11].

The wide-swing cascade current mirror used in the cascade circuit produces a high output resistance [12] which is given by:

$$R_o = [g_{m6}r_{ds6}(r_{ds4}||r_{ds2})]||[g_{m8}r_{ds8}r_{ds10}] \quad (6)$$

The gain of the cascode circuit is given by:

$$A_{dc} = g_{m1}R_o \quad (7)$$

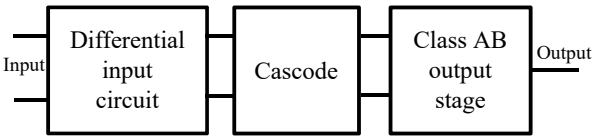


Fig. 6 Block diagram of the op-amp structure

B. Rail-To-Rail Output

The second stage is provided by feedforward class-AB control and is achieved using transistors M23 and M24, biased by two in phase signal currents from the cascade transistors M11 and M13. The gate voltages are kept at a constant value by the stacked diode connected transistors (M25-M26 and M27-M28). The floating current source transistors are M21 and M22, and their transistors are connected to the stacked diode with feed-forward class-AB control. The output stage with transistor coupled feedforward class AB control and floating current source is appropriate for designing a compact and power efficient op-amp [11].

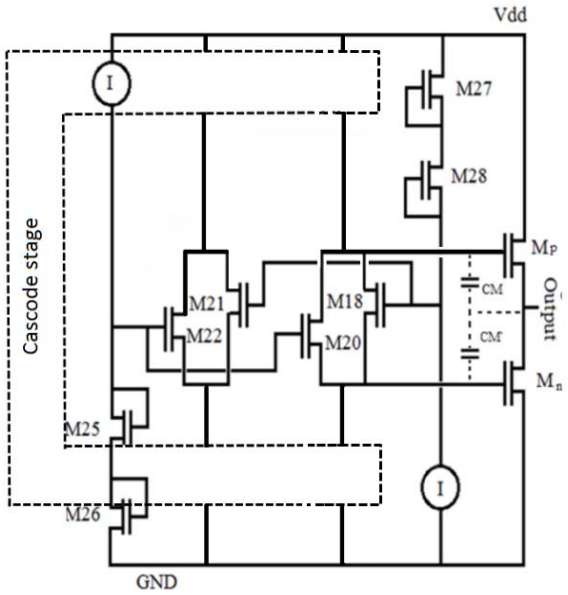


Fig. 7 Class AB stage structure with Miller capacitance

The class AB amplifier and floating current source control is implemented in the cascode circuit in order to decrease the noise and offset. The noise and offset of the amplifier are mainly determined by the input transistors and the summing circuit [13]. In addition, the minimum supply voltage for the class_AB stage transistor operation is equal to Vdd (min) = Vgs(M26) + Vgs(M25) + Vsat. Even if M25 and M26 operate in weak inversion, it means that Vdd (min) of this stage is quite often the value that limits the minimum power supply voltage for low voltage operation of the overall op-amp [14], [15]. Moreover, good high-frequency behaviour is achieved as the coupling between the gates is realized by a single transistor [16].

IV. Design Implementation and Results

Fig. 8 shows the second op-amp circuit with Miller and negative Miller capacitances. The negative Miller capacitance is connected around the first stage (C_{NM1} is connected between the negative input to the output of first stage and C_{NM2} is connected between the positive input to the output) and they must be matched values.

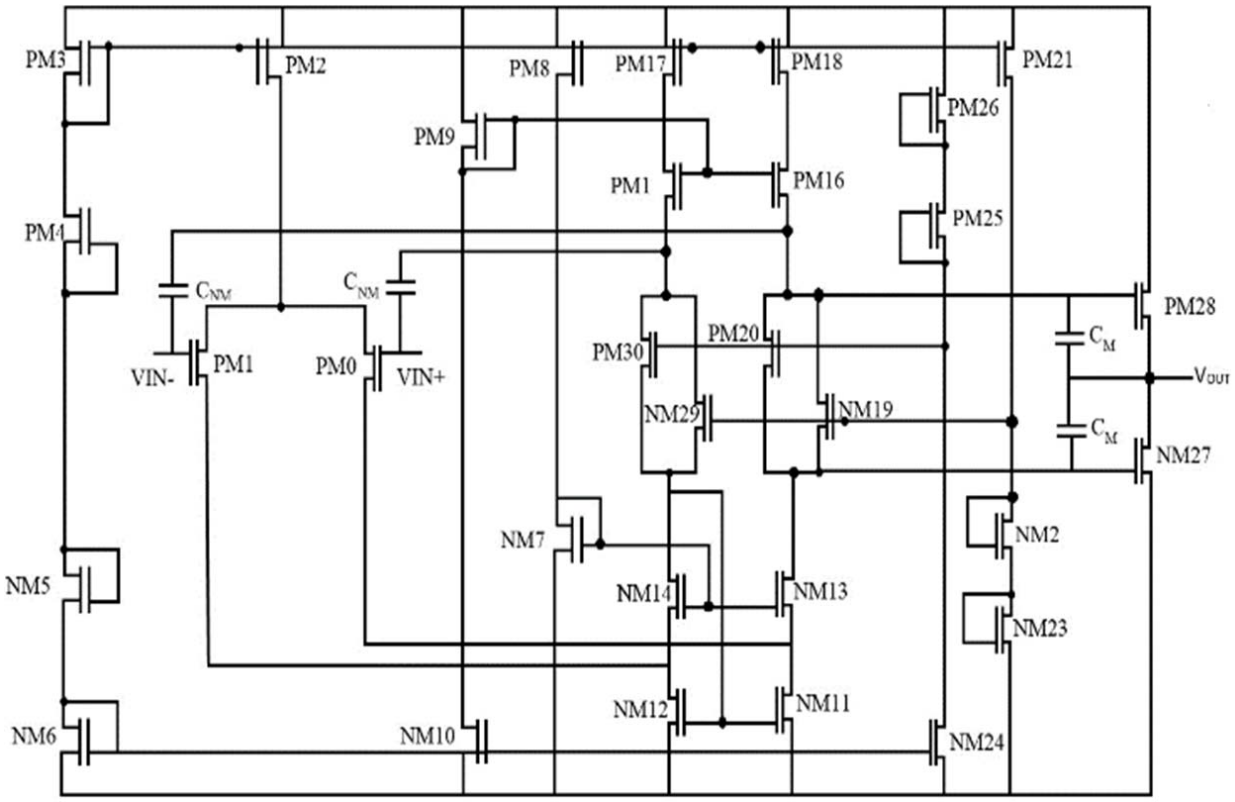


Fig. 8 Schematic of the second op-amp (negative Miller compensation and Miller compensation)

The op-amp was simulated with AMS 0.35 µm CMOS technology and simulated using the Cadence Spectre simulator. The threshold voltages of NMOS are around 0.5 V and PMOS transistors are in the around of 0.7 V.

The supply voltage Vdd is 3.3 V and the load capacitance is a 1 pF. Table I shows the results for the first op-amp design with different Miller capacitor values (i.e., no negative Miller capacitors included) and identifies that the phase margin has increased with increasing the Miller compensation (increasing the value of C_M), but the unity gain frequency has reduced. Fig. 9 shows the gain frequency and phase for different of the Miller capacitance values.

Table II shows the different values of the negative Miller capacitor with a fixed Miller capacitor value of 0.4 pF. The unity gain frequency increases and phase margin shows a reduction as the value of C_{NM} is increased. Fig.10 shows the gain frequency and phase with different of the negative Miller capacitance.

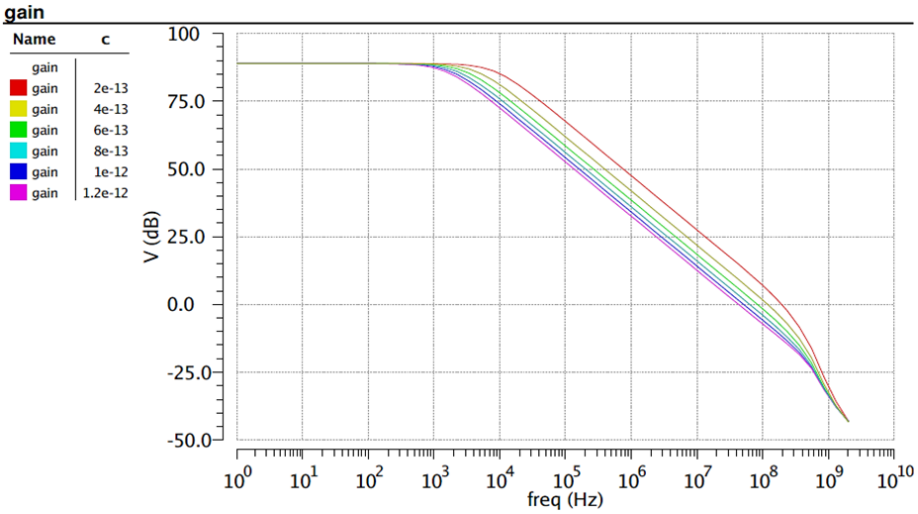
In Table III, a comparison between the two op-amp designs is provided. The DC gain, common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) have not changed since the input differential pair or current summing branches do not contribute to PSRR [17].

TABLE I
Different Miller Capacitor Values for the First OP-AMP Design

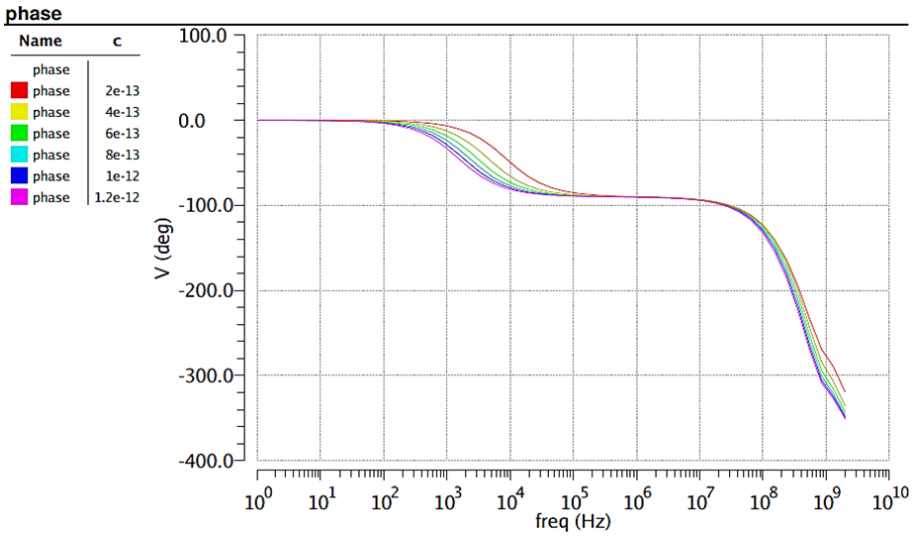
C_M pF	Phase margin degree	Unity gain frequency (MHz)
0.2	52.43	233.1
0.4	68.99	129.6
0.6	75.02	87.40
0.8	78.12	6380
1	79.87	53.05
1.2	81.14	42.32

TABLE II
Different Negative Miller Capacitor for the Second OP-AMP Design (Fixed Miller Capacitor Value)

C_{NM} pF	Phase margin degree	Unity gain frequency (MHz)
0.2	57.34	290.94
0.4	52.41	328.88
0.6	48.07	328
0.8	44.76	359.12
1	42.69	373.36
1.2	41.14	384.56

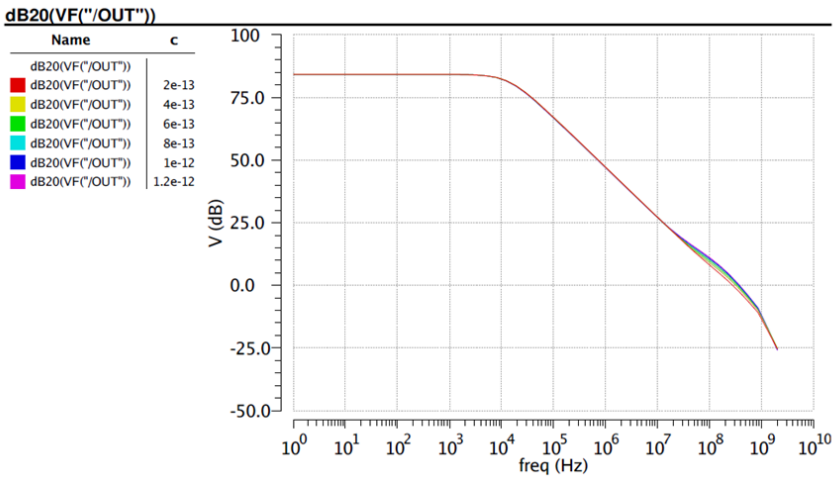


(a)

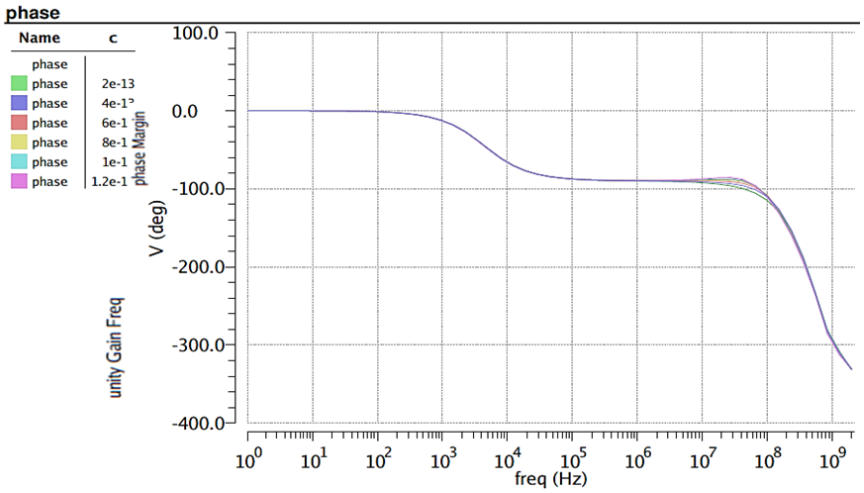


(b)

Fig. 9 Frequency response of the first op-amp (a)- gain and (b)- phase



(a)



(b)

Fig. 10 Frequency response of the second op-amp (a)- gain and (b)- phase

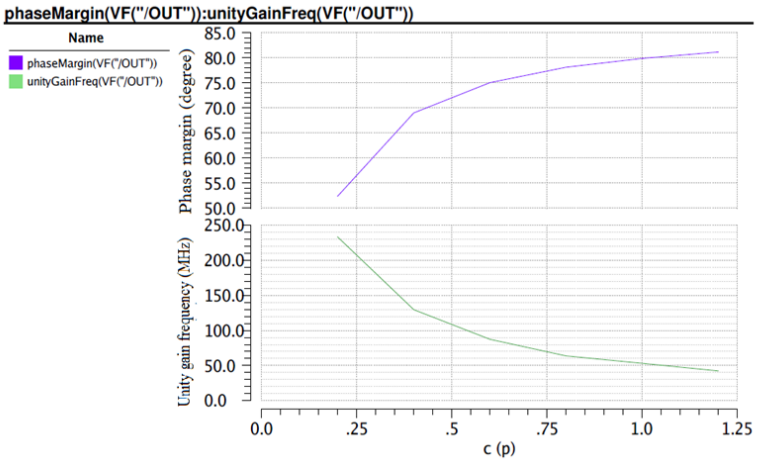


Fig. 11 Miller capacitance variation with unity gain and phase margin

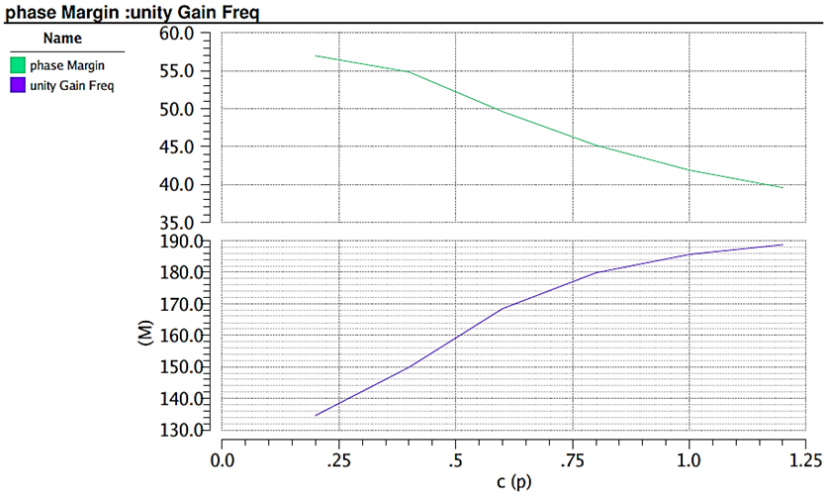


Fig. 12 Negative Miller capacitance variation with unity gain and phase margin

TABLE III
COMPARISON OF OP-AMP PERFORMANCE: MILLER CAPACITANCE ONLY AND COMBINED MILLER WITH NEGATIVE MILLER CAPACITANCE OP-AMP

Parameters	Miller capacitance only	Miller and negative Miller
Power supply (V)	3.3	3.3
DC gain (dB)	85.93	85.93
Phase margin (degree)	49.5	53.13
Unity gain frequency (MHz)	174.4	217.7
CMRR (dB)	100.4	100.4
PSRR (dB)	135.43	135.43
Slew rate (V/μs)	79.4	75.9
DC offset (mV)	1.53	1.53
Input Common Mode Voltage	0~2.45	0~2.45
Output Voltage Swing high (V)	3.28	3.28
Output Voltage Swing low(mV)	0.12	0.12
Settling Time (μs)	0.217	0.182

V. CONCLUSIONS

In the paper, two op-amp designs with different unity gain frequencies and phase margins have been discussed. A scheme using a combination of Miller and negative Miller compensation was presented. In this arrangement, the op-amp is compensated by connecting a Miller capacitor around the first stage and the second compensation using negative Miller around second stage of the op-amp. This configuration results in a significant improvement the unity gain frequency with suitable phase margin, presenting higher speed and appropriate stability. An op-amp was designed using a 0.35 μm CMOS fabrication process using the planned compensation scheme. The total unity gain frequency of the op-amp is increased when related to the Miller compensation techniques with a single power supply operation.

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