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Enhancing the Performance of Wireless Sensor Networks Using Low Power Design

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***Abstract*—**Wireless sensor networks (WSNs), are constantly in demand to process information more rapidly with less energy and area cost. Presently, processor based solutions have difficult to achieve high processing speed with low-power consumption. This paper presents a simple and accurate data processing scheme for low power wireless sensor node, based on reduced number of processing element (PE). The presented model provides a simple recursive structure (SRS) to process the sampled data in the wireless sensor environment and to reduce the power consumption in wireless sensor node. Based on this model, to process the incoming samples and produce a smaller amount of data sufficient to reconstruct the original signal. The ModelSim simulator used to simulate SRS structure. Functional simulation is carried out for the validation of the presented architecture. Xilinx Power Estimator (XPE) tool is used to measure the power consumption. The experimental results show the average power consumption of 91 mW; this is 42% improvement compared to the folded tree architecture.

***Keywords*—**Power consumption, energy efficiency, low power WSN node, recursive structure, sleep/wake scheduling.

I. Introduction

WSNs are the widely used platform to interact with physical world. Low power WSNs design are used in applications such as military, agriculture, biomedical, structural and environment monitoring. The major components of the wireless sensor nodes are the sensor, radio and microcontroller unit along with the power supply using battery. But the radio transmission consumes more energy and design nodes are consuming minimum power to extend the lifetime of the node. The sensor processors are compact and reliable which can combine sensing, computation, storage, power supplies and communication into small form factors. The sensor operation depends on power consumption as the sensors are inevitably used in remote areas which are difficult to reach. The limitations of the sensors like reduced lifetime and difficulty in replacement in remote areas have led to the development in this field. The future emphasis is to increase the lifespan of the sensor with minimal usage of resources in efficient way for all applications. [1]-[3]

Each sensor node operates by collecting the information from the surrounding and transfers them to the base station through wireless transmission. Since power required for the sensor node is more, battery is not sufficient due to its limited capacity. The wind and solar energy sources are not reliable to use although these sources are sufficient for WSN. Hence, the design of WSN should use the low power architecture [4], [5]. The basic design architecture of the sensor node consists of storage unit, power unit, transceiver, processing unit and sensing unit as shown in Fig. 1. The power generator is connected to the power unit to provide power for the sensor node to operate. The energy usage in sensor nodes can be reduced by reducing the duty cycle, dynamically changing the frequency, tuning the radio transceiver selectively. Xilinx and Altera are two major Field Programmable Gate Arrays (FPGA) in the semiconductor marketplace as they offer up to 28 nm CMOS technology. This development in semiconductor field leads to produce energy-efficient computing platforms. In some situations, selective operation is enabled by selectively turning on the specific functional modules. Recent FPGAs include energy-efficient arithmetic components such as adders and multipliers operating at high-speed with low power consumption.

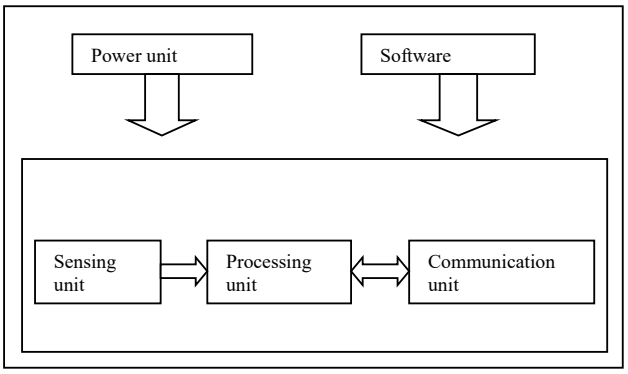

Fig. 1 Sensor Node Architecture

There are numerous circuit approaches available to reduce total system power consumption and each approach has its own architecture and performance implications from sub-threshold circuit design to asynchronous circuit to power gating. Power minimization is one of the most important design goals in modern nanometer integrated circuits design [13]. Especially for WSN, power minimization has become inevitable part in today VLSI design. Power minimization is not only to enhance the battery lifetime but also to reduce the overheating problem. WSN operates in four distinct modes of operation: Transmit, idle, receive and sleep. An important observation in the case of most radios is that operating in idle mode results in expressively high power consumption, almost equal to power consumed in the receive mode. By employing more appropriate PEs the power consumption in all the four

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modes of operation will reduce significantly. In the present VLSI technology, reducing power consumption is an important issue. Especially for WSN, due to their limited battery lifetime, the low power VLSI design has become inevitable for wireless communication. The goal of this paper is to design a low power systolic architecture for WSN nodes. The work presented in this paper focus on implementation of FPGA in WSN.

II. Literature Review

The configurability of FPGA can be generally classified into static and dynamic configurability. In static reconfiguration, the configuration only occurs between running of FPGA chip. Several research groups have exploited the usefulness and benefit of FPGA by developing ad-hoc reconfigurable devices. The flexibility of these systems is high, compared with ASIC, but only static reconfiguration has been explored in these works. Gao et al. developed a new architecture for sensory node controller (SNOC). This node uses dynamic voltage scaling (DVS) mechanism. DVS is used to minimize the energy essential for running a given task by dynamically changing the supply voltage and the clock speed of the processor permitting to the time constraints prescribed by each task [6]. Lu et al. introduced a new ASIC design of sensor network device in which the power is reduced by "Sleep – Event wake up" low power management mechanism [7].

Y. Li et al. designed a novel partial dynamic reconfiguration-based WSN node for less power consumption [8].Rafael Vicente Martinez-Catala developed the architecture to reduce the power consumption by designing a miniaturized 3D architecture using cubic structure [9]. Imran et al. introduced energy-efficient SRAM FPGA-based wireless vision sensor node (VSN). VSN is designed using static RAM (SRAM) based FPGA when compared to FLASH based FPGA. For conserving energy, the VSN can be switched to a low-power state, referred to as the sleep state, when the required vision tasks have been performed [10].

Hulzink et al. proposed design low power wireless sensor node for biomedical applications. This tracks the data driven operations and single instruction multiple data (SIMD) mechanism. The low power consumption is achieved by power optimization at altered abstraction layers comprising application optimization and mapping, system partitioning for effective duty cycling, multi-layer extensive clock gating, and circuit level optimization for operating at near threshold and low power on-chip clock generation [11]. Zhu et al. proposed low power reconfigurable processor utilizing variable dual VDD. To reduce the power by applying variable dual -VDD method [12].

TABLE I
Comparison of Literature Review

Ref.	METHODOLOGY	PROS	CONS
[6]	DVS	✓ Required power is one fourth of the fixed power supply.	❖ Increases the programming overhead.
[7]	Sleep –event wake up	✓ Security using un-resemble coder algorithm	❖ Applicable only for specific applications
[8]	Reconfiguring the hardware.	✓ Less area complexity	❖ Disconnection while programming.
[9]	Built-in battery in wireless sensor node	✓ No external battery requirement	❖ Needs a systematic approach to integrate the battery.
[10]	SRAM FPGA based WSN	✓ Life time is extended.	❖ Generic architecture supporting only duty cycling applications.
[11]	Data driven mechanism	✓ Very less power consumption	❖ Partitioning of the circuit.
[12]	Variable dual-VDD ethod.	✓ CMOS transistors are used.	❖ Requires reconfigurable processor

III. Folded Tree Architecture

Fold Tree Architecture with parallel Prefix Operation is used to reduce the total numbers of PEs in the VLSI design and also reduces the total area, by reducing the number of PEs. Area is proportional to power, so power consumption is also reduced. During processing and transmission of signals, the WSN nodes will consume more power. Especially for clock distribution, nearly 70% power is consumed. Merging technique is used to optimize the power during clock distribution, multi-bit flip-flop. A straightforward binary tree execution of Blelloch's loom costs a momentous quantity of area as n inputs need p = n - 1 PEs. To shrink area and power, pipelining can be traded for throughput. In a classic binary tree, layer of PEs finishes dispensation, to overtake the results and novel calculations can previously recommence autonomously.

The concept vacant here is to fold the tree back onto itself to maximally salvage the PEs. In burden so, p becomes comparative to n/2 and to cut the area in half. Area is proportional to power, so power is also cut in half and also reduces the interconnection. This tree topology is depicted in Fig. 2, which is functionally comparable to the binary tree on the left side. By using the Folded Tree Architecture power consumption, area and wire length are reduced considerably. Folded Tree Architecture (FTA) for on-the node data processing in WSNs, using parallel prefix operations and data locality in hardware reduces both area and power consumption. The FTA design is used to reuse the PE nodes. It is restraining the data set by preprocessing among parallel prefix operations. The combinations of data flow and control flow elements are to near a local distributed memory, which removes the memory bottleneck while retaining ample flexibility. Several PEs consume more power, so by using FTA, the PE can be reused and power is reduced. Sensor node is to perform the task whenever necessary. The power consumed is less when compared with the simple recursive architecture of the sensor node.

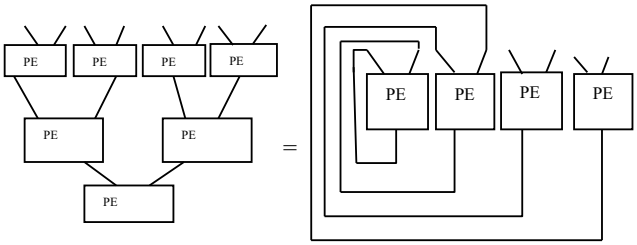

Fig. 2 Binary Tree and Equivalent Folded Tree

IV. Recursive Architecture

The recursive architecture is shown in Fig. 3, where single PE is used repeatedly to complete the reduction of collected sensor data. In the trunk phase to add the output data recursively with the input data. The iteration counter counts the process; after completing the process, the iteration counter initiates the memory/register to give the data output. In trunk phase, the average of all the sensed data along with the internal register content is transferred to the receiver. In the receiver, twig phase is to be carried out.

In the twig phase, we use the same setup as in the trunk phase, but instead of addition, subtraction process will be carried out in the PE. The Buffer is used to register the input data and output data. The use of single PE results in reduced area and reduced complexity which leads to reduced power consumption. The power can be reduced by introducing the sleep/wake mechanism in the proposed simple recursive architecture. The sleep mode is activated at the end of the task and the sensor node will be in wake mode while performing the task. The block diagram of the recursive structure of the sensor node with the sleep and wake scheduling is given in Fig. 4.

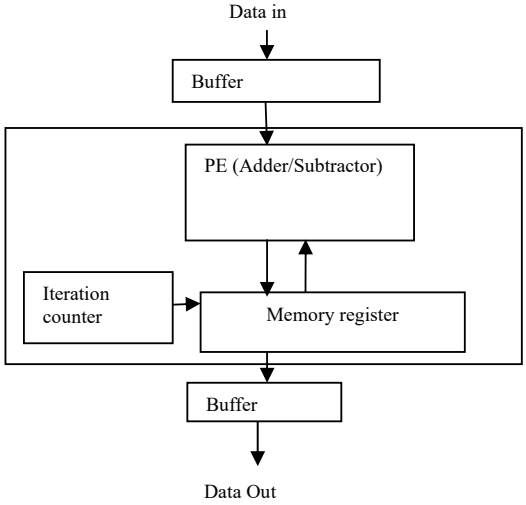

Fig. 3 Simple Recursive Architecture

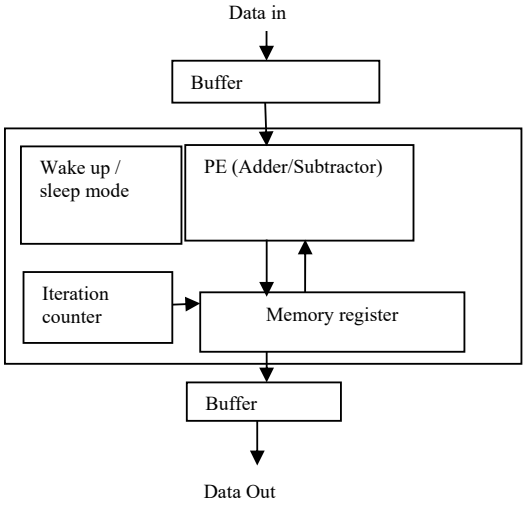

Fig. 4 Recursive Architecture with Sleep/Wake Scheduling

V. Experimental Results

ModelSim is a multi-language (HDL) simulation background by Mentor Graphics. It can be used separately, or in conjunction with Altera Quartus or Xilinx ISE. Simulation is performed with the GUI, or robotically using scripts. In this architecture, the collected sensor data are compressed using inter-stage accumulation process. The transmitter sends the processed intermediate results to memory/ register.

The simulation waveform shows the collected sensor data, intermediate processed results and the final accumulated value. The intermediate process takes 3-cycles to complete the task, and 1-cycle is required to buffer the final results. So totally the process needs 4-clock cycles to complete the entire process. In this process, total of 9-clock cycles are required to process the collected sensor data. Here, 8-clock cycles are required to process the intermediate accumulation and 1-clock cycle is required for buffer/registering purpose. Comparative study of folded tree structure and recursive structure reveals that the recursive structure takes more time to process the data when compared to folded tree structure. This is due to reduced resource allocation. In folded tree structure, the system requires 4-PEs to complete the task. But in recursive structure, the system needs 1-PE only. The processing speed is not a matter of fact because the wireless sensor application has more impact due to energy/power consumption. By considering this key point a single PE is used to process the complete work.

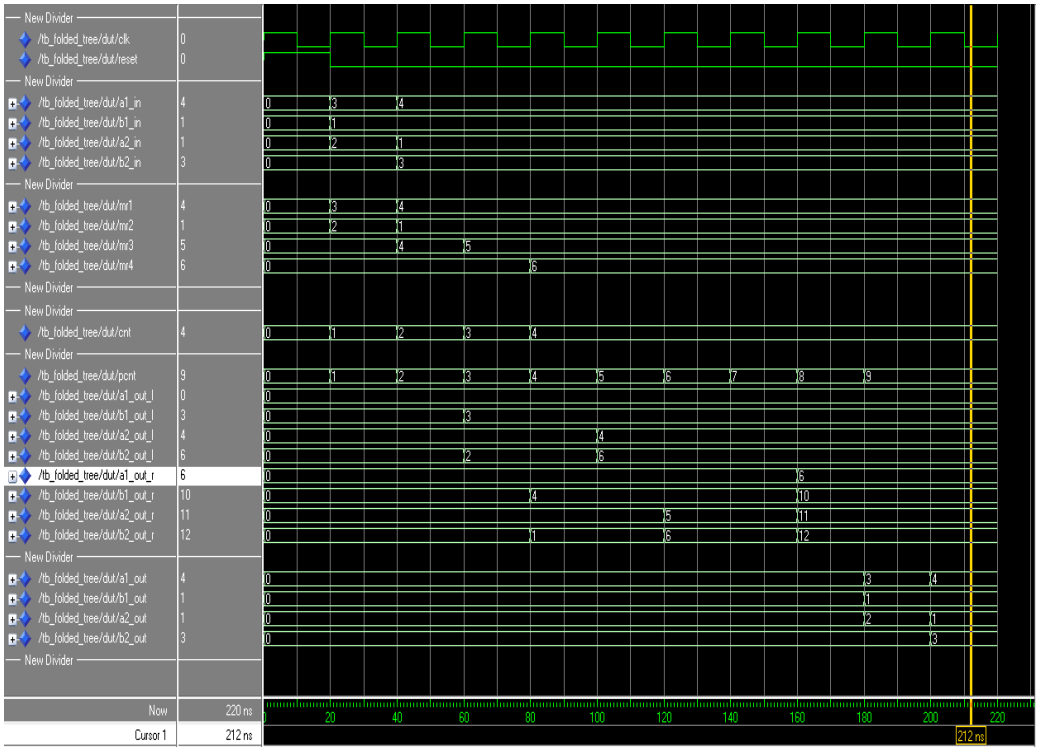

Fig. 5 Simulation Waveform of FTA

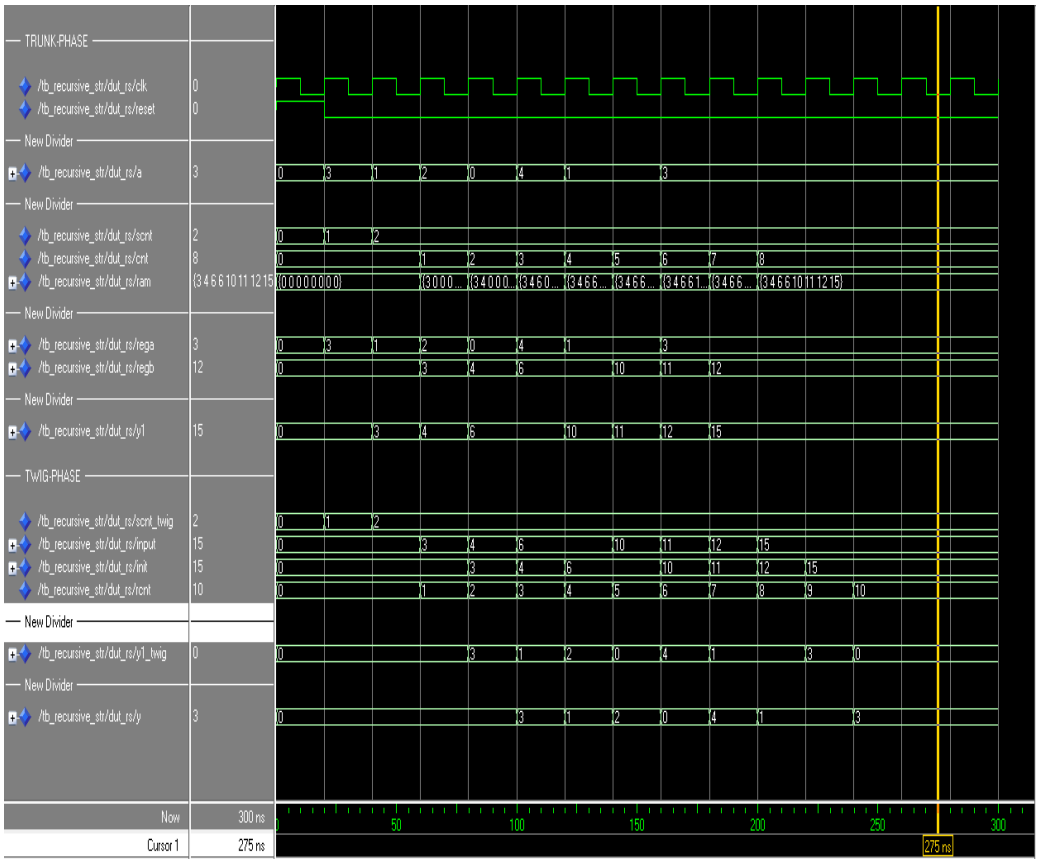

Fig. 6 Simulation Waveform of Recursive Architecture

VI. Power Report

TABLE II
POWER CONSUMPTION OF FTA

Clock Rate	FTA		
	Quiescent (mw)	Dynamic (mw)	Total (mw)
Default	56	50	106
100	60	41	101
200	60	78	138
300	61	114	175
400	61	151	212
500	61	187	248

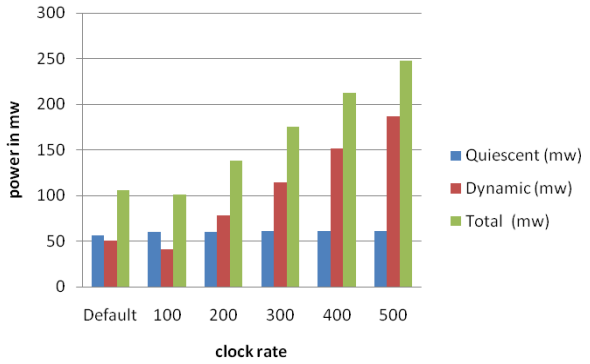

Fig. 7 Power Summary of FTA

TABLE III
POWER CONSUMPTION OF RECURSIVE ARCHITECTURE WITH SLEEP/WAKE SCHEDULING

Clock rate	Recursive Architecture with Sleep/Wake Scheduling		
	Quiescent (mw)	Dynamic (mw)	Total (mw)
Default	56	3	59
100	60	15	71
200	60	26	79
300	60	38	88
400	60	49	96
500	60	61	105

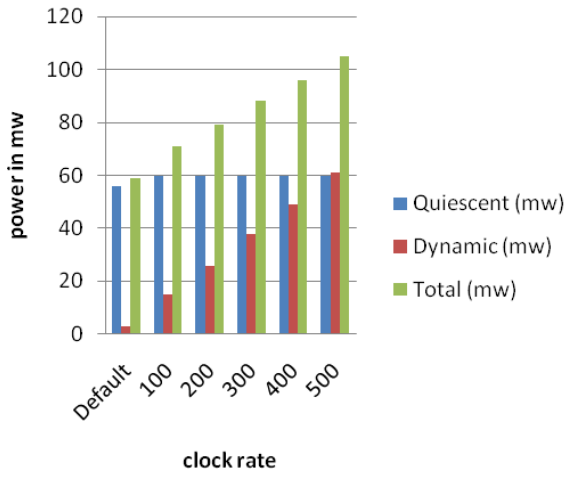

Fig. 8 Power Summary of Recursive Architecture with Sleep/Wake Scheduling

TABLE IV
TOTAL POWER COMPARISON

Clock rate	FTA (mw)	Simple Recursive Architecture (mw)	Recursive Architecture with Sleep/Wake Scheduling (mw)
Default	106	59	59
100	101	75	71
200	138	86	79
300	175	98	88
400	212	109	96
500	248	121	105

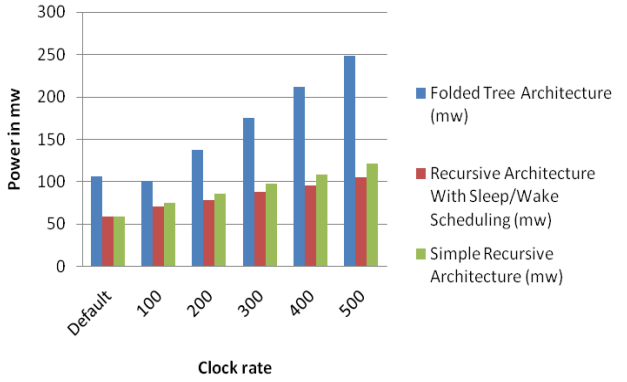

Fig. 9 Total Power Comparison

VII. Conclusion

Power consumption is the vital factor to be considered in recent years; many researches are concentrating on low power architectures. Power consumption influences the performance and the lifetime of the sensor nodes in WSN. This scheme is based on the resulting architecture in a Xilinx FPGA device for the proof of concept validation. The experimental result shows 42% on the average of less power consumption compared to the existing FTA. A speed of 143.431 MHz is achieved in the presented recursive architecture. These performance metrics shows the effectiveness of the presented SRS.

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